Timing Electronics @ SDHCAL

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On behalf of Shanghai-Omega-Lyon Group

CALICE Collaboration Meeting

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Contents

Brief motivation

- Purpose:
  - **Identify neutral and charged hadrons**
  - five dimension calorimeter
  - Position, Energy **and Timing**
- Adding MRPCs layers in the SDHCAL
- Front-end board for MRPC readout
  - Charge and timing measurement
  - **High resolution timing** measurement

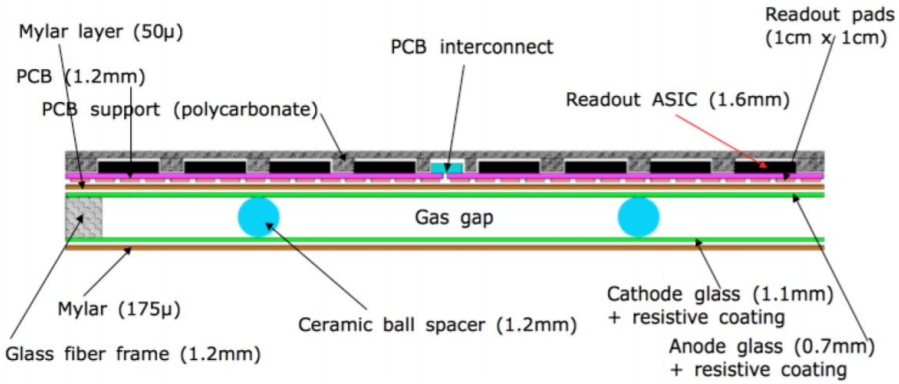


Fig 2. Resistive Plate Chamber(RPC) structure

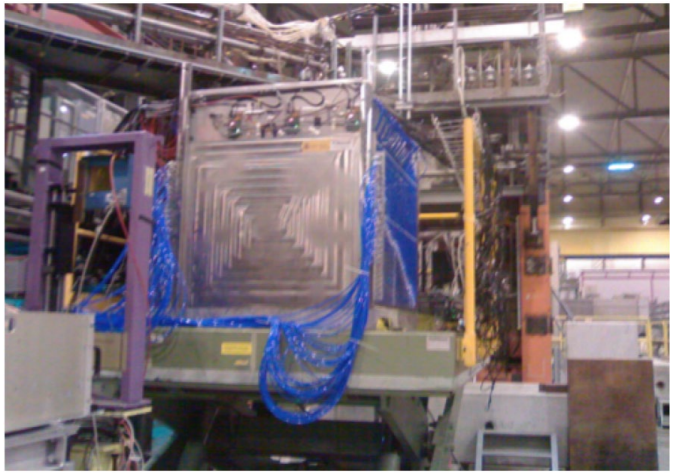


Fig 1. SDHCAL Prototype

First step:

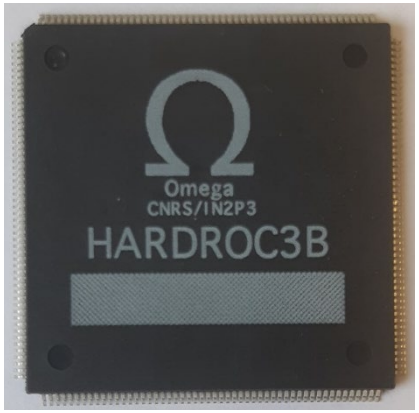
Design a front-end prototype board with four **petiroc2a**

Second step:

Build the 1m×1m **petiroc2a FEE**

HARDROC3B vs PETIROC2A

- Time resolution: **time stamping 200ns**
- Signal Polarity: negative
- 64 current inputs
- Sensitivity: Trigger on 10 fC with 100% efficiency
- Dynamic range: 30pC

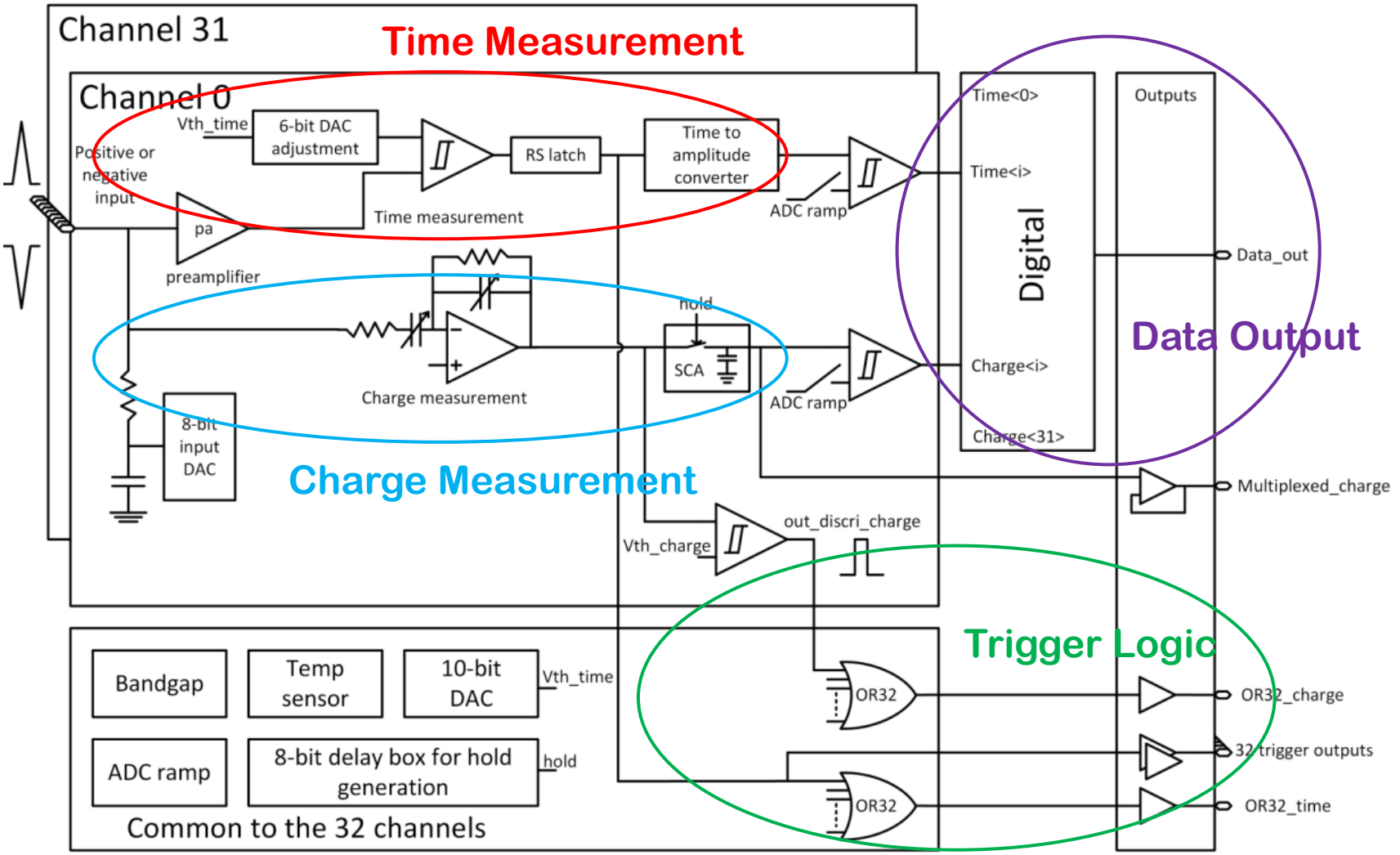


https://www.weeroc.com/products/other-read-out/hardroc-3b

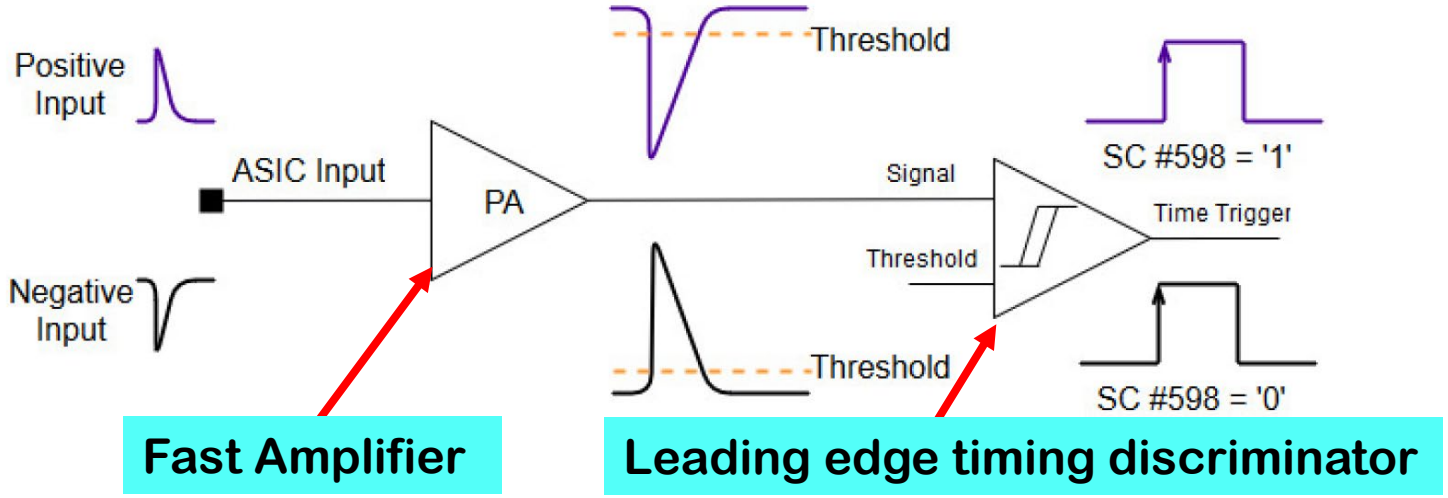
- Time resolution: **below 40ps**
- Negative or positive
- 32 voltage inputs
- Sensitivity: Trigger on first photo-electron
- 3000 photoelectrons (10^6 SIPM gain), Integral Non Linearity : 1% up to 2500 photoelectrons

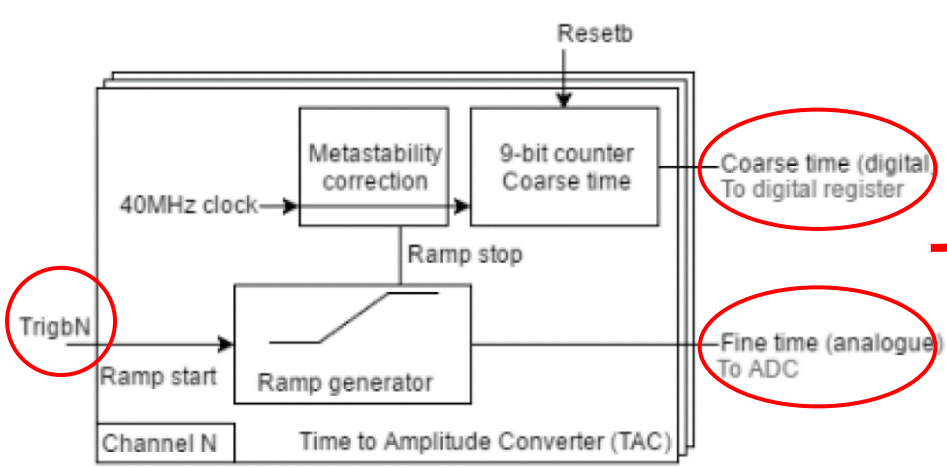
https://www.weeroc.com/products/sipm-read-out/petiroc-2a

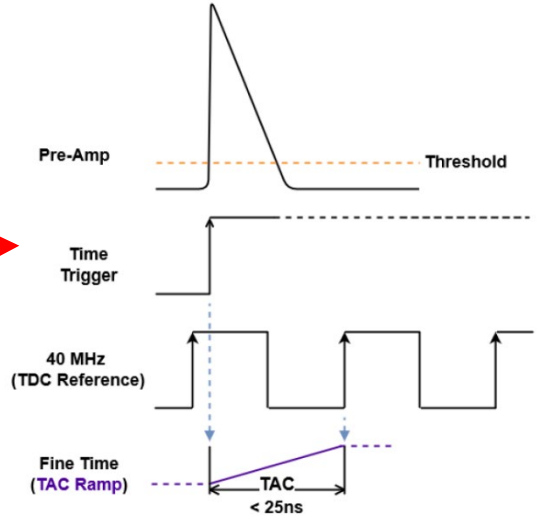
Block Diagram of PETIROC2A



Timing Measurement @ PETIROC2A







Block Diagram of Readout System

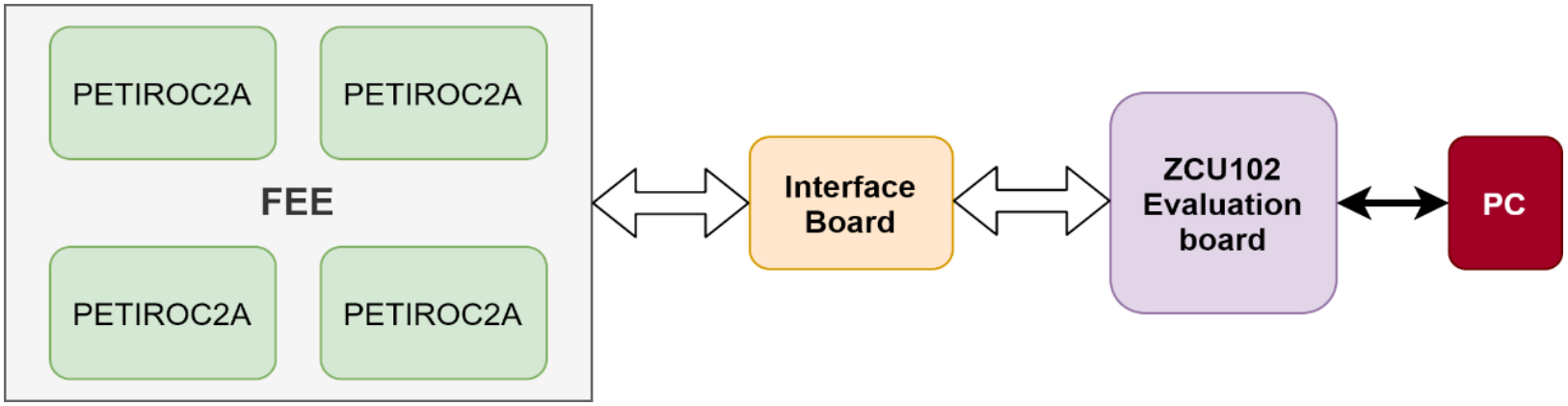


Fig 3. Block diagram of front-end electronics and data acquisition

- Front-End Board with four petiroc2a chips, Interface board and DAQ system
- A new-designed Detector Interface (DIF) card is in charge of the communication and data transfer with the FE electronics
- Design one DAQ system based on commercial FPGA (ZCU102)

Design of Front-End Board

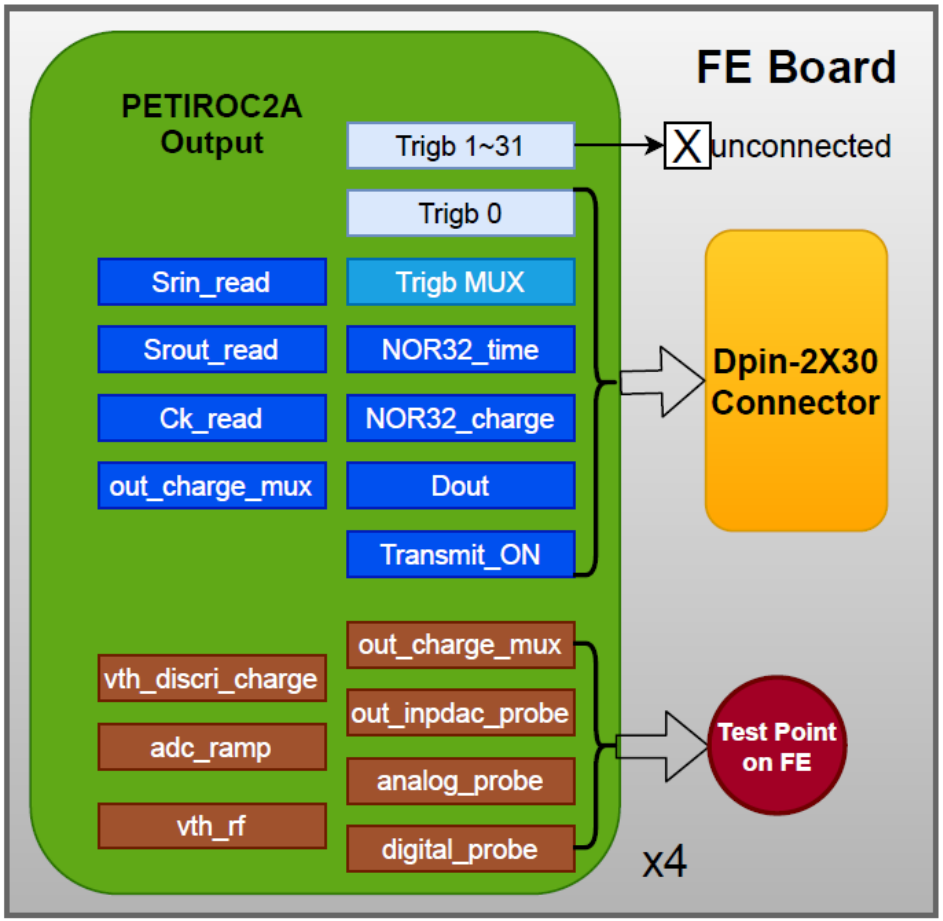


Fig 4. Block diagram of front-end electronics

- 32 trigger output
  - Only connect one to FPGA for test purpose
- Open collector buffer
  - 100 Ohm external resistors
  - Trigb_MUX, transmit_ON
- Dout
  - LVDS Differential signals
- Some signals are connected to onboard test points.

Design of Front-End Board

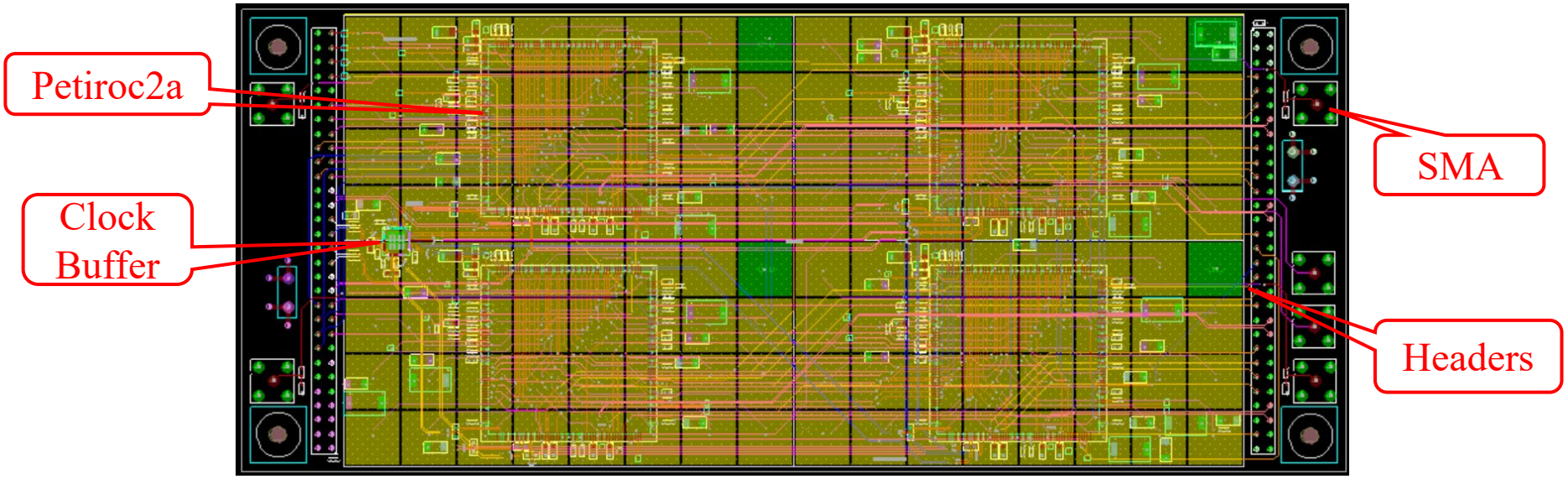


Fig 5. PCB layout of front-end electronics(prototype board)

- Components: four petiroc2a chips, clock buffer(2:8) for clock signal(40MHz and 160MHz)

  two headers for communication with DAQs and SMA for injection test.

- 128 pads(yellow square) , induction unit size: 1cm×1cm.

- The dimension:197mm*82mm, the blind/buried via technology.

Technology of Front-End Board

		SURFACE	AIR
2	TOP	CONDUCTOR	COPPER
3		DIELECTRIC	FR-4
4	GND1	CONDUCTOR	COPPER
5		DIELECTRIC	FR-4
6	SIG1	CONDUCTOR	COPPER
7		DIELECTRIC	FR-4
8	SIG2	CONDUCTOR	COPPER
9		DIELECTRIC	FR-4
10	GND2	PLANE	COPPER
11		DIELECTRIC	FR-4
12	VDDA	PLANE	COPPER
13		DIELECTRIC	FR-4
14	VDDD	PLANE	COPPER
15		DIELECTRIC	FR-4
16	GND3	PLANE	COPPER
17		DIELECTRIC	FR-4
18	SIG3	CONDUCTOR	COPPER
19		DIELECTRIC	FR-4
20	SIG4	CONDUCTOR	COPPER
21		DIELECTRIC	FR-4
22	GND4	CONDUCTOR	COPPER
23		DIELECTRIC	FR-4
24	BOTTOM	CONDUCTOR	COPPER
25		SURFACE	AIR

Fig 6. Stack-up information and via layer design

- 12 layers are designed.
- Many key induction units are at the bottom of the board.
- Via technology:
  - **Laser-drilled Via-in-pad Technology** (small size: ~0.1mm)
  - **Buried vias** with the size 0.3mm
  - **Through vias** located in two edges without induction pads

✓ **The manufacture of FEB is ongoing.**

Detector Interface card

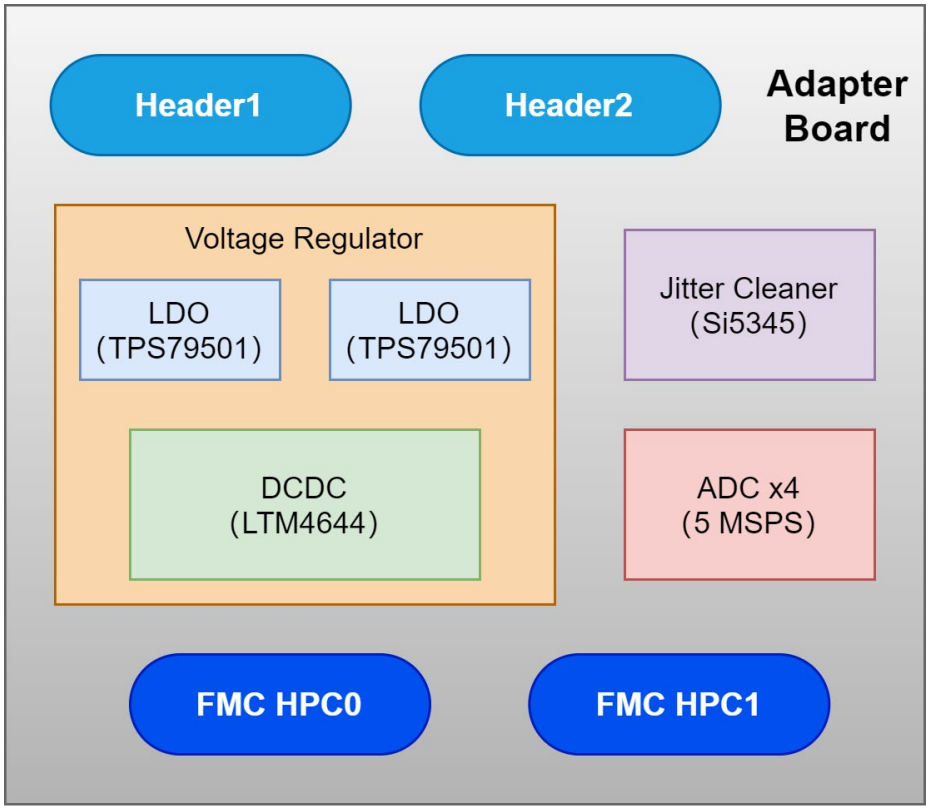


Fig 7. Block diagram of DIF card

- DIF card will be in charge of the **communication and data transfer** with the FE electronics(two headers) and ZCU102(two FMCs).
- Components: voltage regulator(DCDC/LDO), jitter cleaner(SI5345) and ADC(5MSPS).
- Analog and digital power are separated.

Design of DIF card

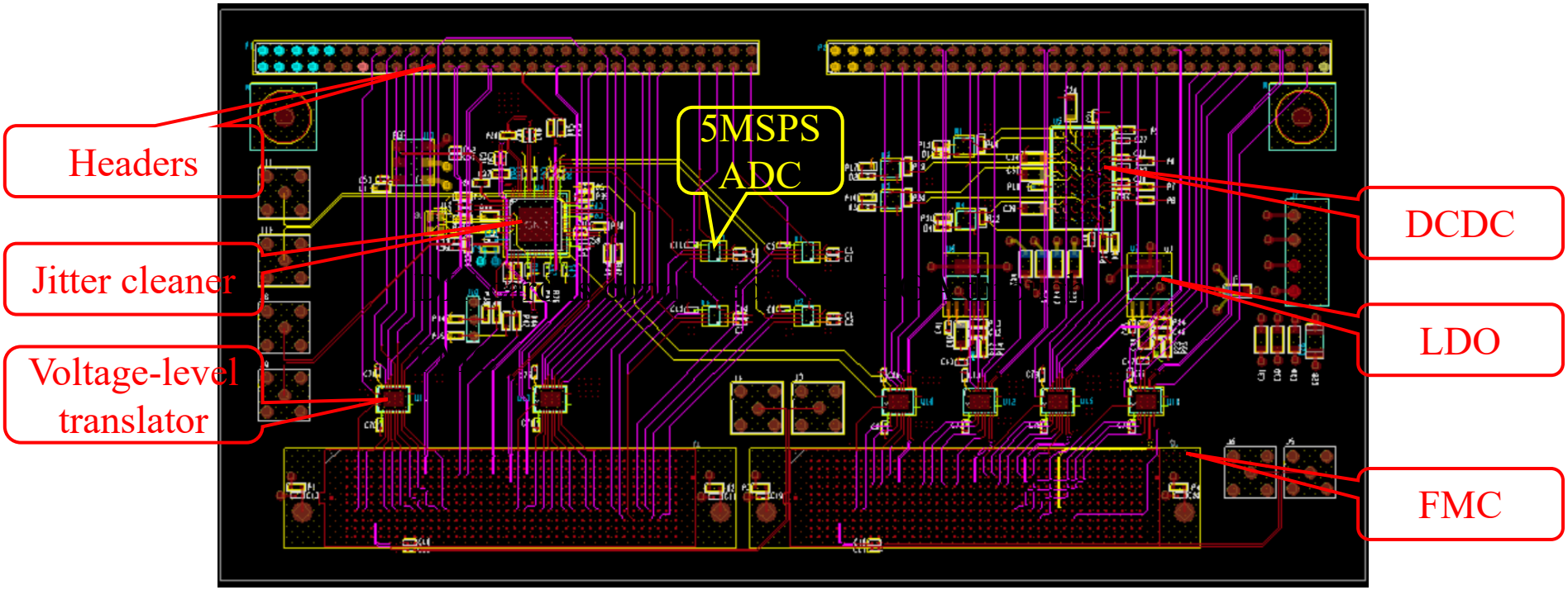


Fig 8. PCB layout of DIF card

- The stack-up of DIF card is 8 layers PCB board.
- Jitter cleaner(Si5345) to improve the clock quality.
- Voltage-level translator.
- DIF card connected with FPGA through FMC.

✓ **The manufacture is ongoing.**

Introduction of FPGA-ZCU102

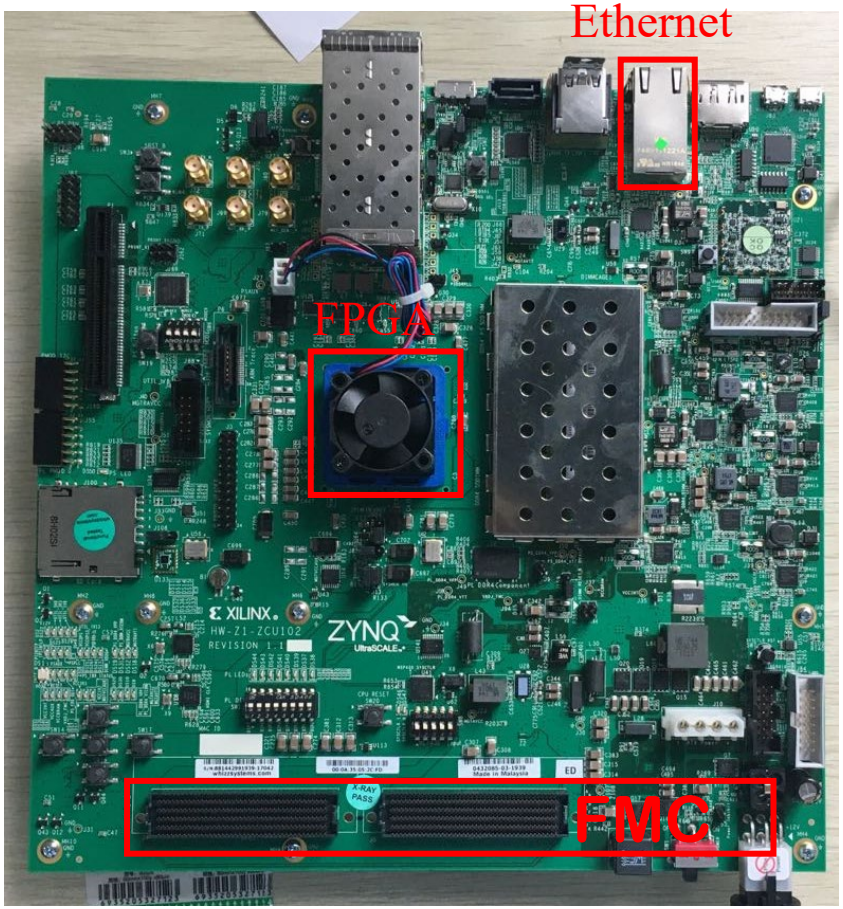


Fig 9. ZCU102 FPGA

- FPGA: ZYNQ UltraScale+ MPSoC
  - SFP, Ethernet, DDR4 etc.
- 2x FMC-HPC connectors
  - 16 GTH Transceivers. 400I/Os
  - 128 single-ended or 64 diff signals
  - 66 I/O used for four petiroc2a chips
- DAQ system will be developed on the basis of the Xilinx ZCU102.

https://www.xilinx.com/products/boards-and-kits/ek-u1-zcu102-g.html

Summary & Next plan

Completed the design of FEE and DIF card

- The prototype of front-end board has been manufacturing
- The production of DIF card is also ongoing

Next plan: Data Acquisition system

- The system will be developed on the basis of Xilinx ZCU102
- Slow-control and data transfer through the Ethernet

Next plan: Test the prototype board

- Test the performance through the signal injection
- Test time resolution applying the board to RPC with cosmic ray

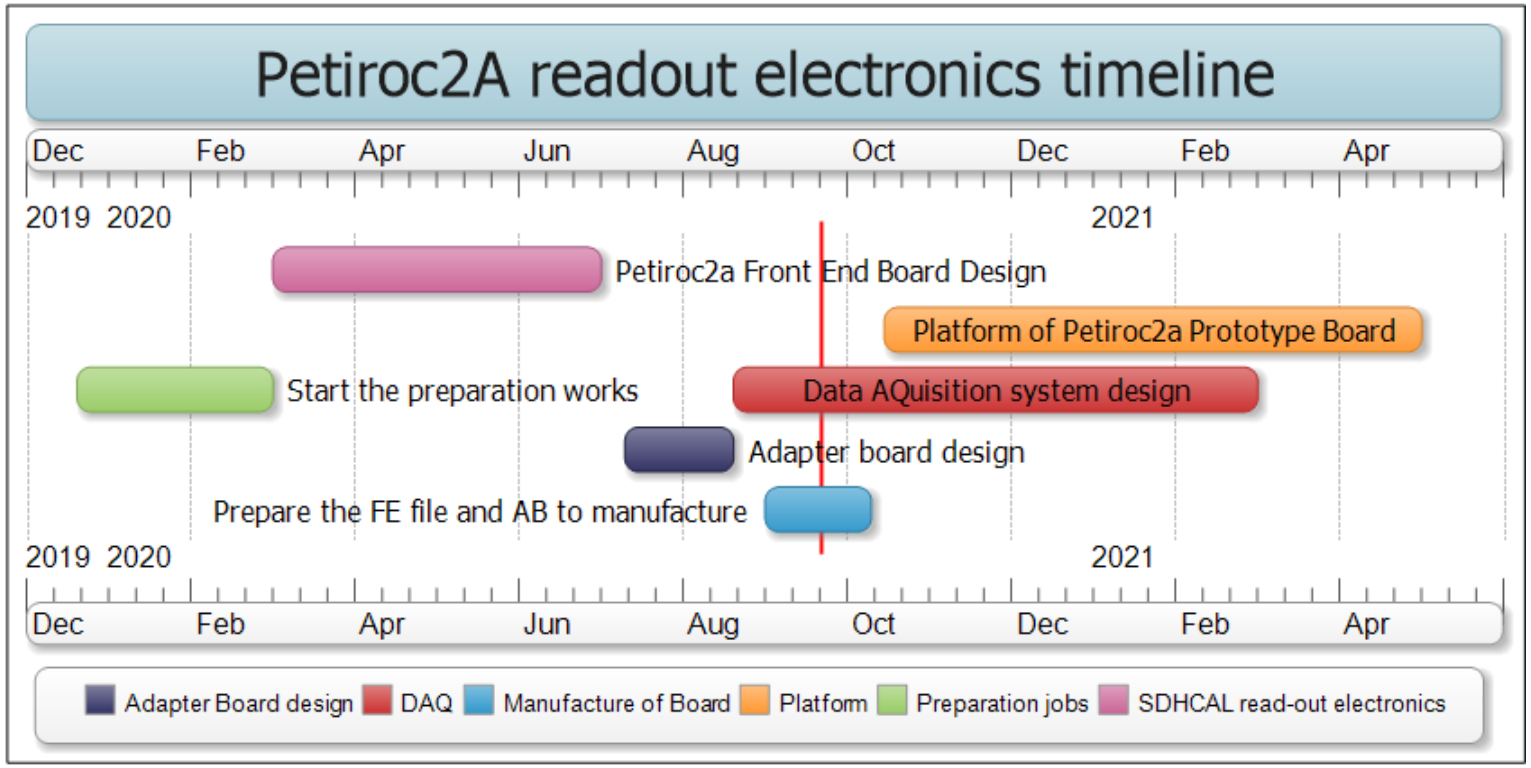
Thanks!

Introduction of PETIROC2A

- Time measurement with 10bits TDC interpolating 40MHz coarse time
- Charge measurement with 10bits DAC
- Voltage input amplifier, 200Ohm matching
- Petiroc2a parameters:
  - One chip with 32-channels and mixed analog/digital
  - The 32chs input connected with PAD(detector unit)
  - One channel split into two parts, respectively for charge and time measurement
  - Internal DAC for each channel to adjust the amplitude of the input signal
  - Lower power consumption(~6mW/channel)

https://www.weeroc.com/products/sipm-read-out/petiroc-2a

Plan & Current Status



- ✓ Petiroc2a front-end prototype board
- ✓ Detector Interface card

- ZCU102 will be used for DAQ system.
- Prepare the firmware for the slow-control and transfer through Ethernet.