Study of the retriggers on SiW-ECAL prototype

Y. Kato, T. Suehara[1], T. Mogi, T. Tanabe[2], S. Yamashita[3]

The University of Tokyo, Kyushu University[1], KEK[2], ICEPP[3]

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Study of the retriggers: Outline

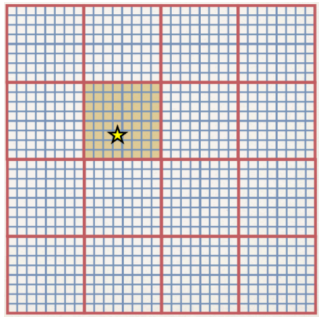
- This talk focus on FEV13: recent short slab of SiW-ECAL technological prototype.

FEV13 MIP run in TB2019	on beam	not on beam
Retrigger/Trigger	~30%	60-70%
Induced/Normal	~10%	30-40%

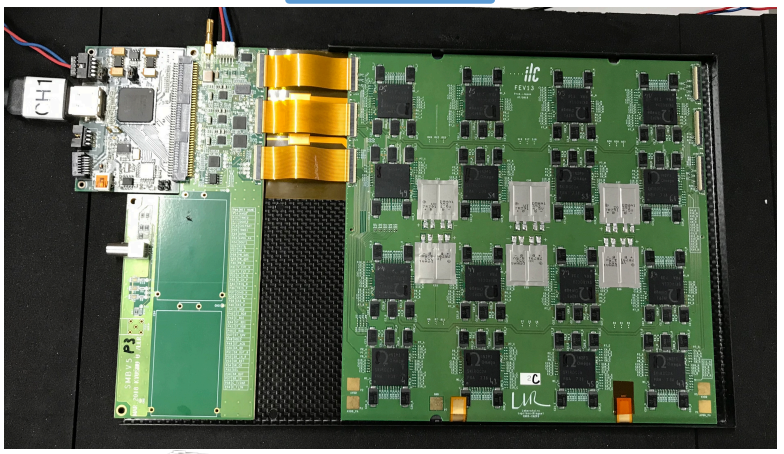
- **What is a retrigger?**
  - high rate of fake hits in the SiW-ECAL tech. prototype.
- **Investigation of retrigger pattern on FEV13**
  - **Pattern**: induced by normal hit(s) and all channels get triggered after few BCIDs
  - **Timing**: random for each ASIC
  - Retrigger rate and effect on ADC are also investigated. (see backup)
- **Investigation of the possible causes of the retriggers**
  - There is no significant correlation on the timing of retriggers between ASICs.
    → Not common within the slab, the cause should be around each ASIC.
  - Retrigger pattern & ADC pedestal shift
    → The cause affect baseline of ASIC.
- **Proposed plan to fix the retriggering problem**
  - Enhancement and optimization of decoupling capacitors around ASICs
- **Summary and prospects**
  - We have narrowed down the possible causes of the retriggers.
  - Evidence points to decoupling capacitors around ASICs
  - Expert opinions are needed to make further progress.

SiW-ECAL technological prototype: FEV

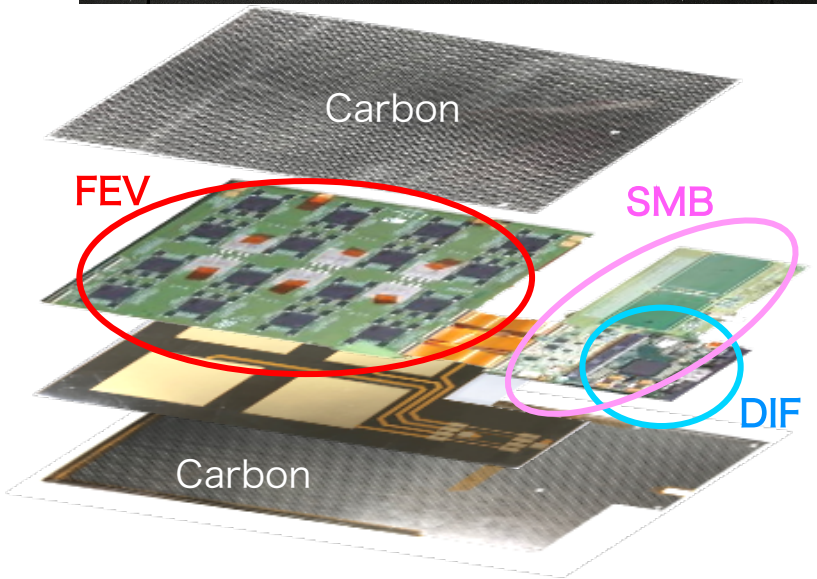
- FEV: frontend electronics of SiW-ECAL short slab
- **Geometrical structure**
  - Si pixel: 5.5 × 5.5 mm^2
  - 32 × 32 = 1024 ch / slab
    (4 Si wafers / slab)
  - 16 ASICs / slab



FEV13

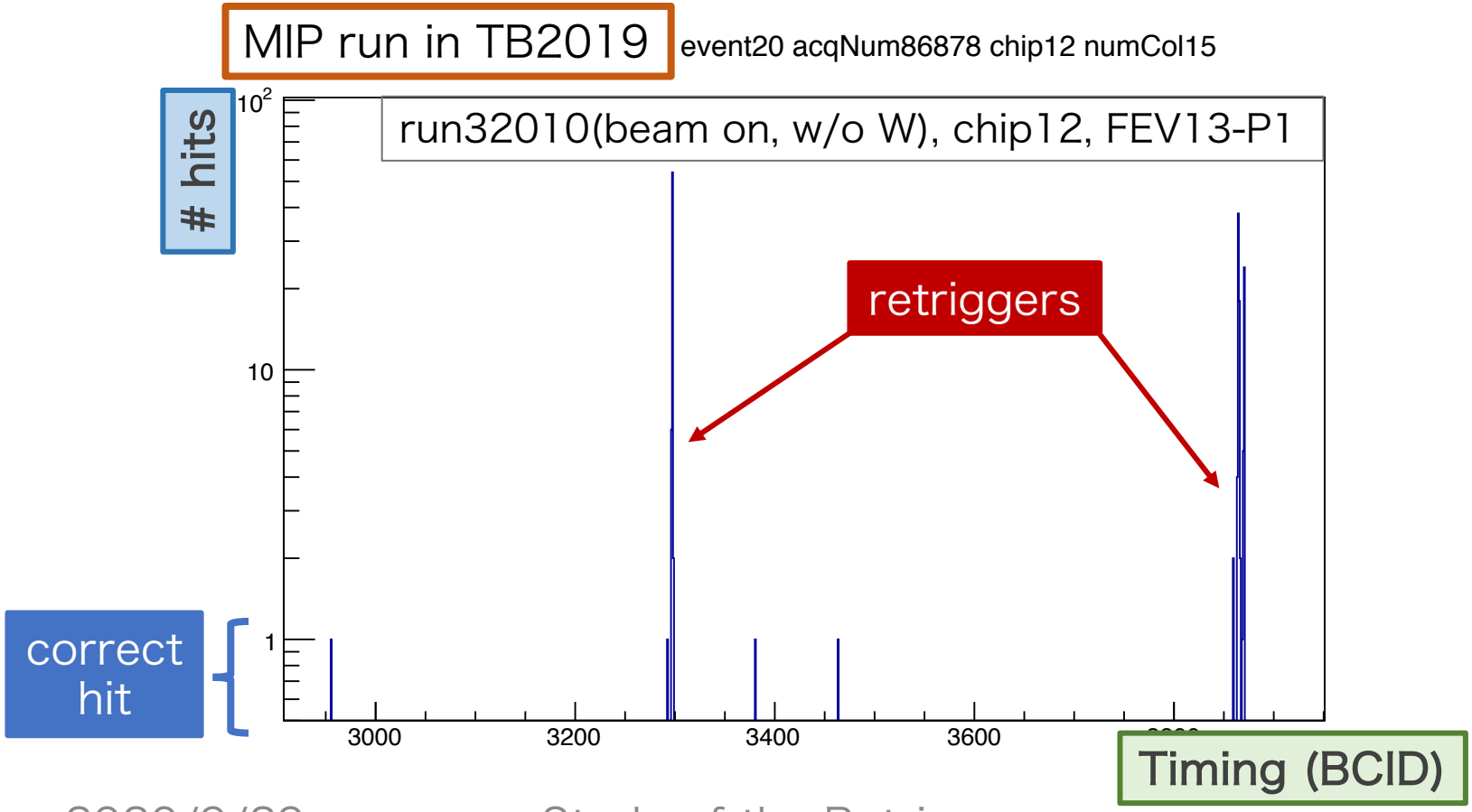


- **Readout information**
  - **Analog processing is performed independently in each ASIC: SKIROC**
  - Hit bit
    - self-triggered by each channel
  - Timing: Bunch Crossing ID (**BCID**)
    f = 5 MHz → Δt = 0.2 μs
  - Analog output
    - Charge/Fine timing
- **Power supply configuration**
  - Power Pulsing or Continuous Current



What is a retrigger?

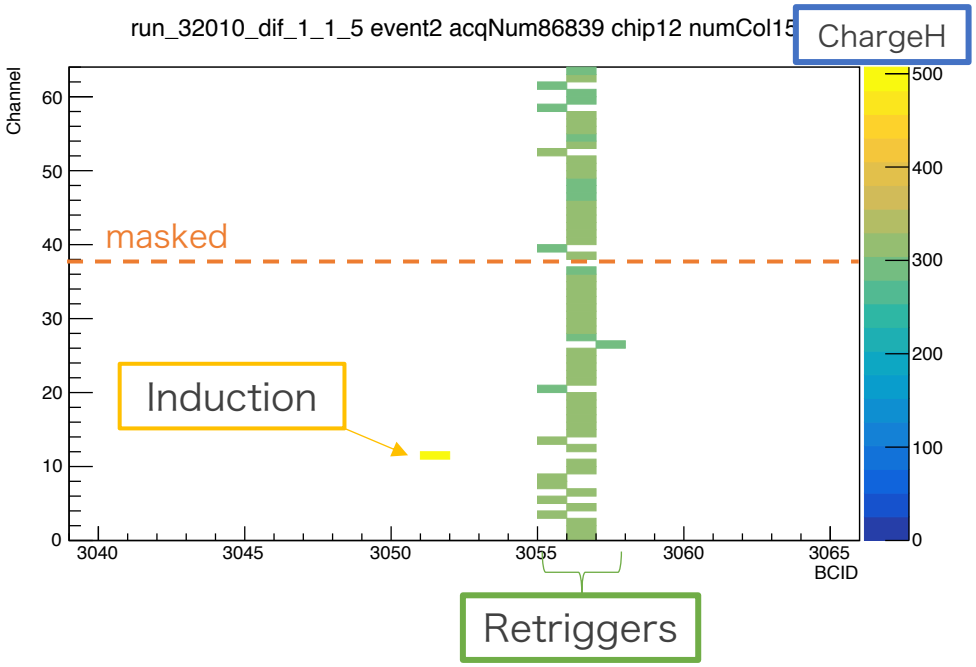
- A set of fake hits in the SiW-ECAL technological prototype.
- We have observed them since the beginning of the tech. prototype.
- In the basic analysis, retriggers are removed using the timing (BCID) features.
- We are investigating the details of their pattern and considering the cause.

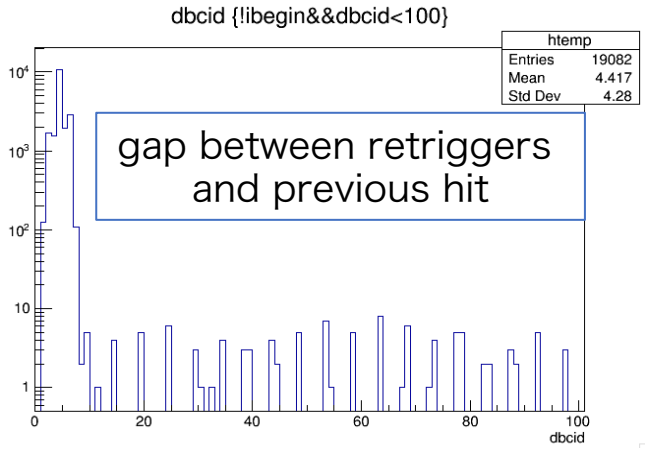


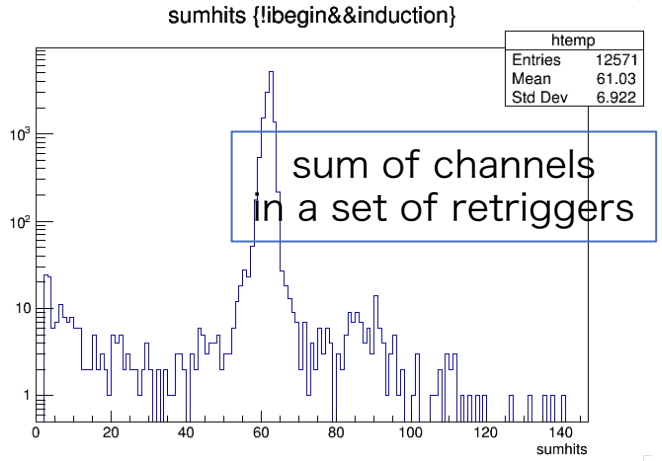
Investigation of retrigger pattern on FEV13

- Triggering pattern in MIP run
  - Almost all the channels are triggered in a set of consecutive BCIDs.
  - Retriggers appear after a few BCIDs from normal hits.

  -> Retriggers are induced by the previous normal hits.



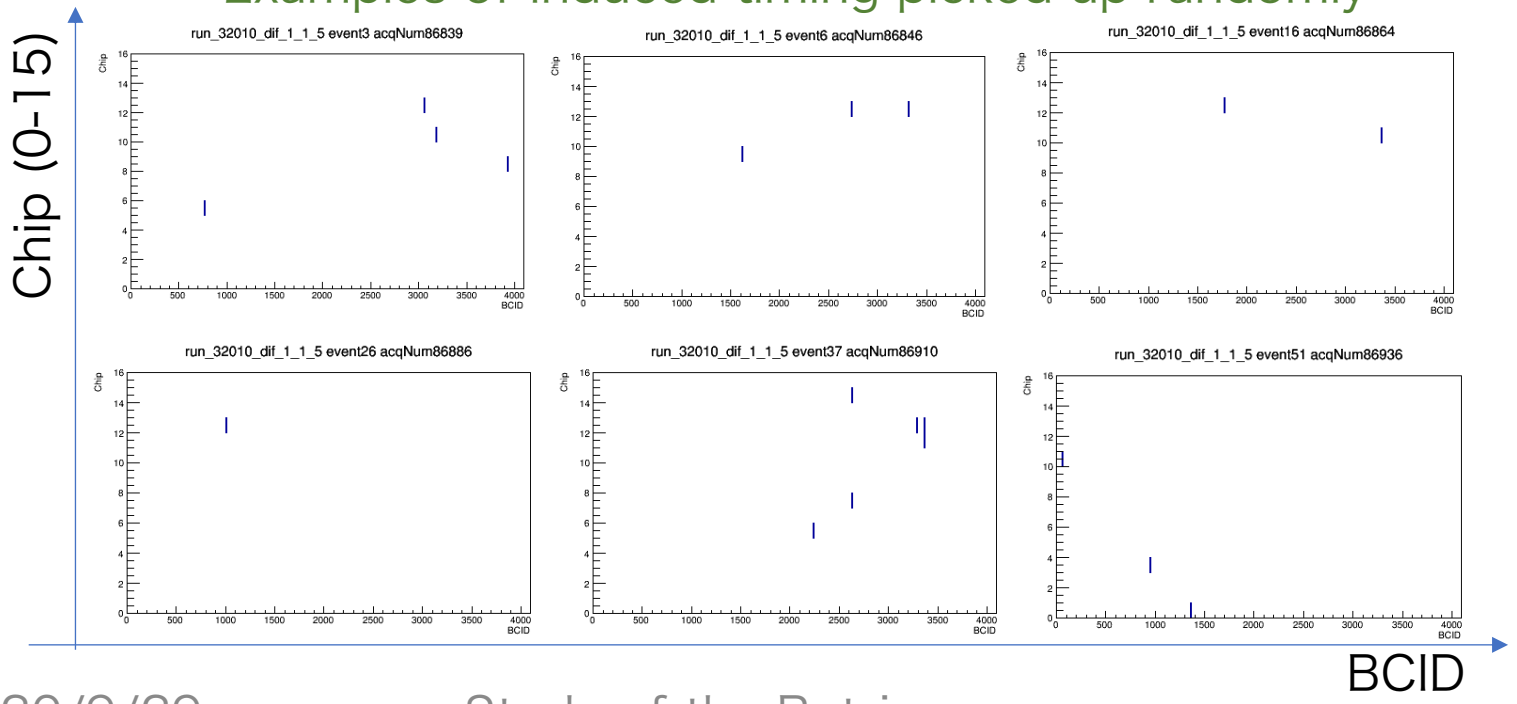




Investigation of retrigger pattern on FEV13

- Timing of retriggers
  - There is no significant correlation on the timing of retriggers between ASICs.
  - In the study about previous FEVs, some correlation between ASICs in terms of CHIPSAT signal was reported. (by A. Irles, see backup)
  - FEV13 might be improved because of the separation of low voltage power layers in the PCB.
    - But the amount of retriggers is not reduced significantly.

Examples of induced timing picked up randomly



Investigation of the possible causes of the retriggers

There is no significant correlation on the timing of retriggers between ASICs.

→ Not common within the slab, the cause should be around each ASIC.

Retrigger pattern & ADC pedestal shift

→ The cause affect baseline of ASIC.

Proposed plan to fix the retriggering problem

Enhancement and optimization of decoupling capacitors around ASICs

Actually it is reported that the retriggers are reduced on COB slabs by adding some decoupling capacitors at LV power line of SKIROC2A analog part. (by A. Irles, see backup)
However, the retriggers have not disappeared completely yet.

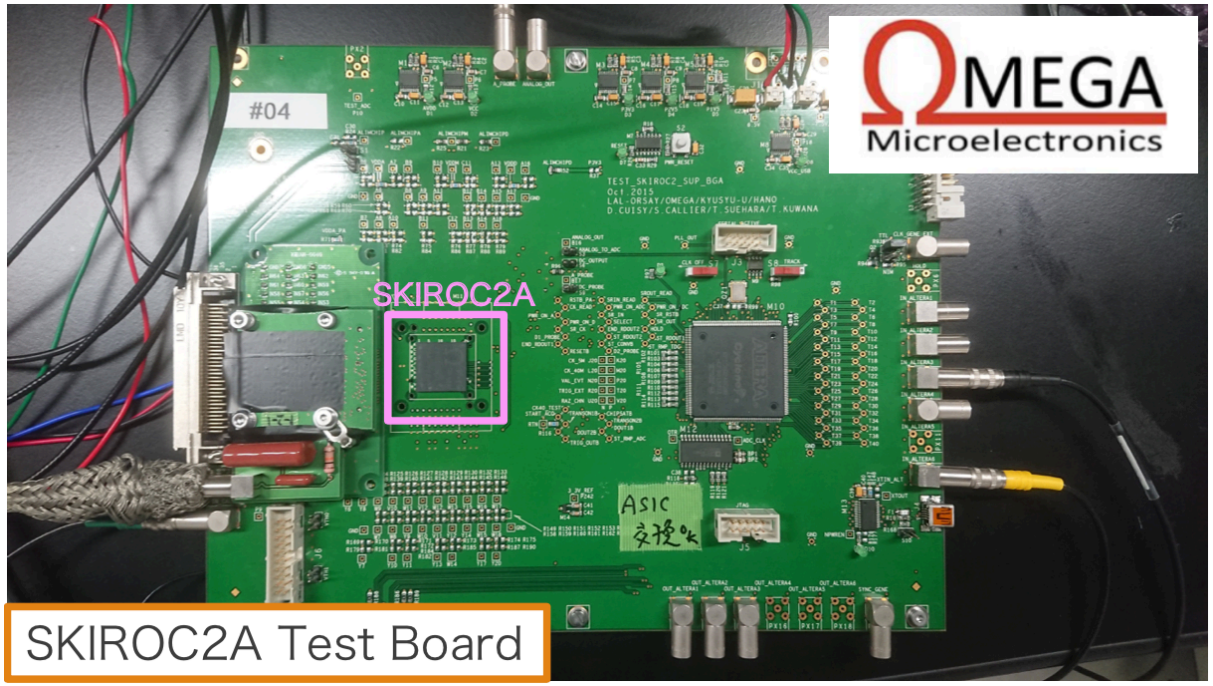
We are now conducting verification for the effect of decoupling capacitors using SKIROC test board.

Preliminary: Test with SKIROC test board

- We are investigating the situation of the retriggers on the SKIROC test board for comparison of the effect of DC capacitor.

SKIROC test board with test injection	w/o additional DC	w/ additional DC on AVDD_PA
Retrigger/Trigger	0.23%	0.25%
Induced/Normal	0.066%	0.035%

Preliminary



SKIROC2A Test Board

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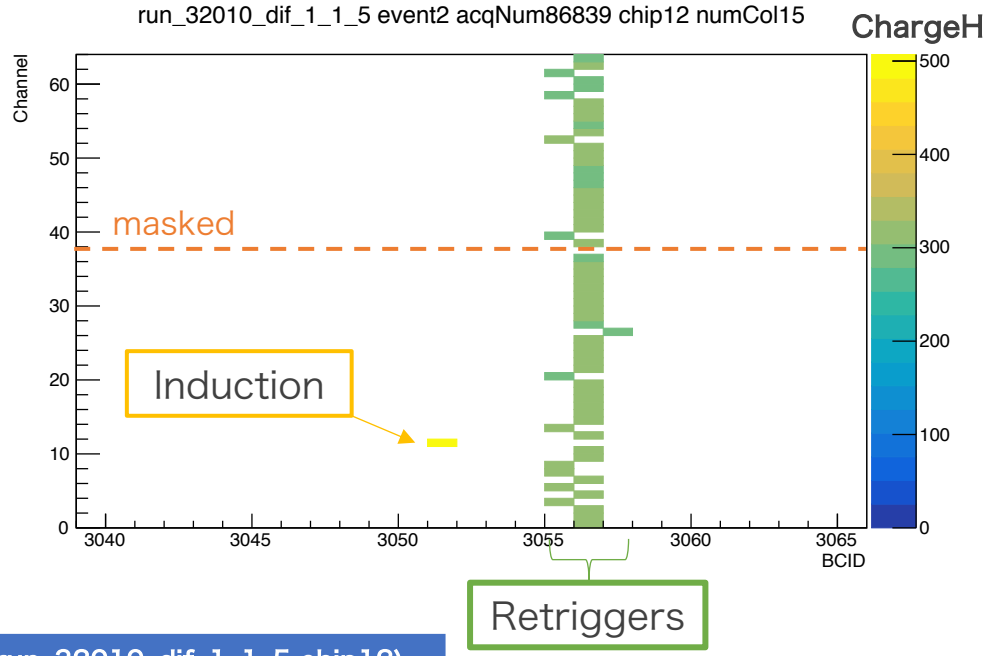
backup

MIP analysis on FEV13 with cosmic ray

- https://www.evernote.com/l/AWXkDz7HIZVGeq1oMv8NARKIAfOqEQBa7dQ

FEV13 in TB2019 at DESY

- MIP run: run32010, FEV13-K2
- Typical retrigger:



- Rate:

MIP run in TB2019 (run_32010_dif_1_1_5 chip12)	
Acq Recoded/Cycle	7068/14469
Triggered	61283
Normal / Empty / Retriggering	44960 / 2635 / 13688
Normal/Triggered	44960/61283 = 73.4%
Induction/Normal	3805/44960 = 8.5%

Triggered = Empty + Retriggers + Normal
Normal ⊃ Induction

Retrigger Rate

Triggered = Empty + Retriggers + Normal
Normal ⊃ Induction

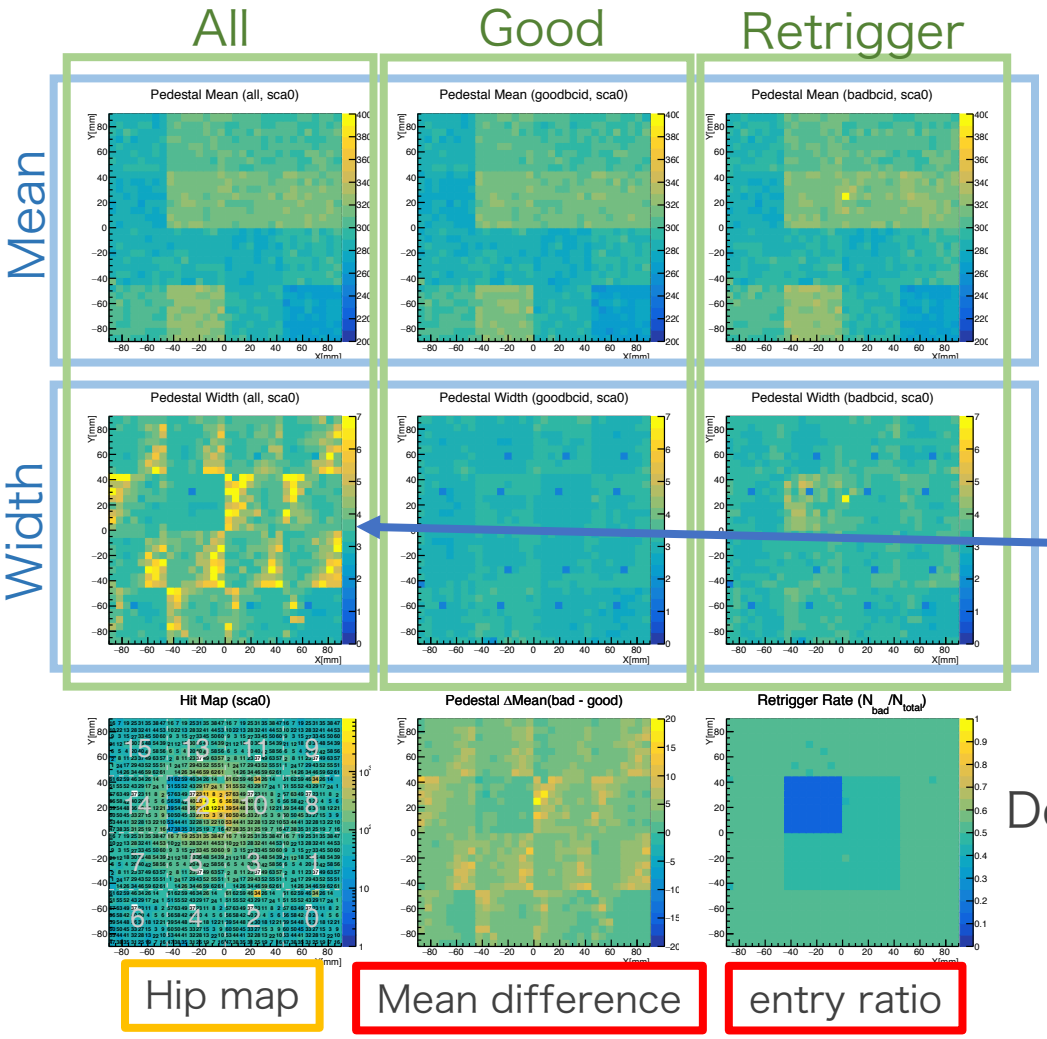
run_32010_dif_1_1_5_retrigger.txt
RESULT
Acq Cycle: 14469, Acq Recorded: 7068

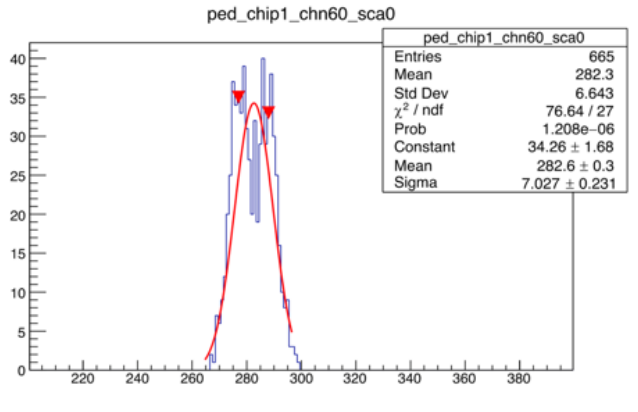
Chip	Triggered	Empty	Retriggers	Induction	Normal	FullSCA	Rate(Induction/Normal)
0	2819	70	1907	297	842	93	0.353
1	3225	59	2224	350	942	84	0.372
2	2928	66	2007	322	855	77	0.377
3	5421	154	3567	653	1700	104	0.384
4	2855	73	1984	305	798	76	0.382
5	5288	175	3230	667	1883	83	0.354
6	2439	76	1661	238	702	80	0.339
7	3319	87	2274	374	958	89	0.390
8	3763	361	2249	425	1153	87	0.369
9	2905	83	1938	286	884	87	0.324
10	18520	788	10149	1895	7583	196	0.250
11	4809	123	3215	521	1471	107	0.354
12	61283	2635	13688	3805	44960	1769	0.085
13	5280	172	3288	635	1820	93	0.349
14	4116	96	2778	488	1242	74	0.393
15	2642	86	1666	309	890	78	0.347

- Many retriggers are occurred in the irradiated chips.
  - The electron tracks should induce the retriggers.
- The rate of induction/normal seems to be higher in chips far from beam spot.
  - Is there any causes other than the tracks?

Retriggers: Double Pedestal

- Pedestal map (run 32004-32010, FEV13-P1, SCA-0)



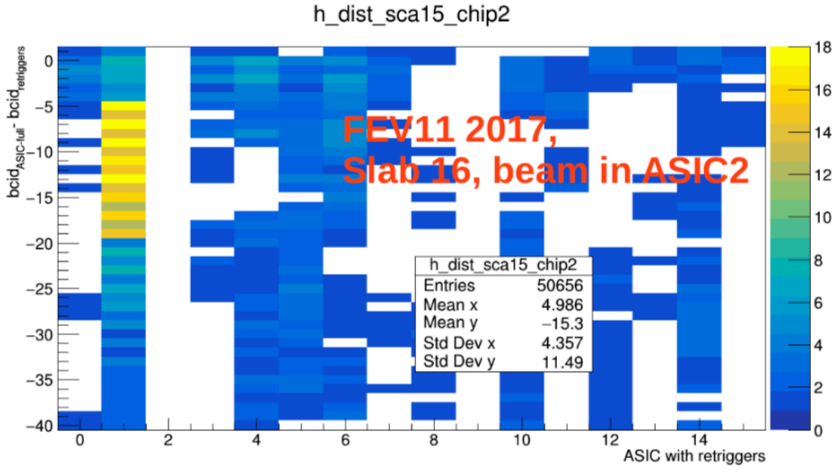


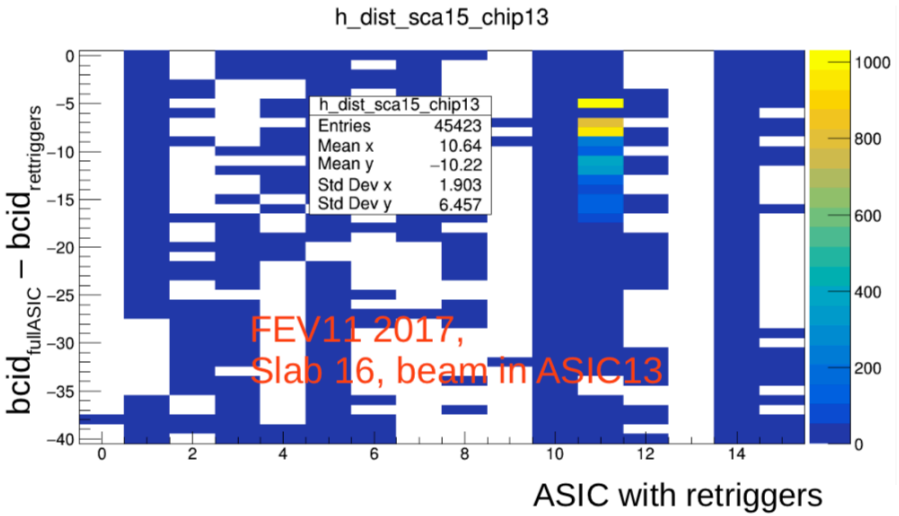
Double pedestal by retrigger

Double pedestal depends on channel position in ASIC.

Study of the retriggers. CHIPSAT in FEV11

- Chipsat signal as a source of retriggers.
- If the ASIC in which the beam is directed is full… I check the correlation with the bcid of all retriggers in other ASICs



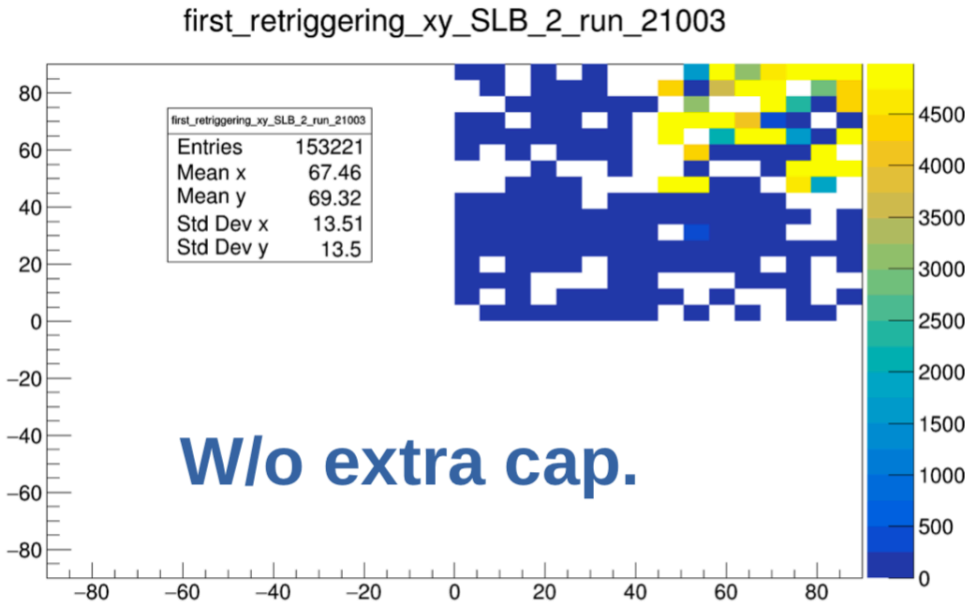


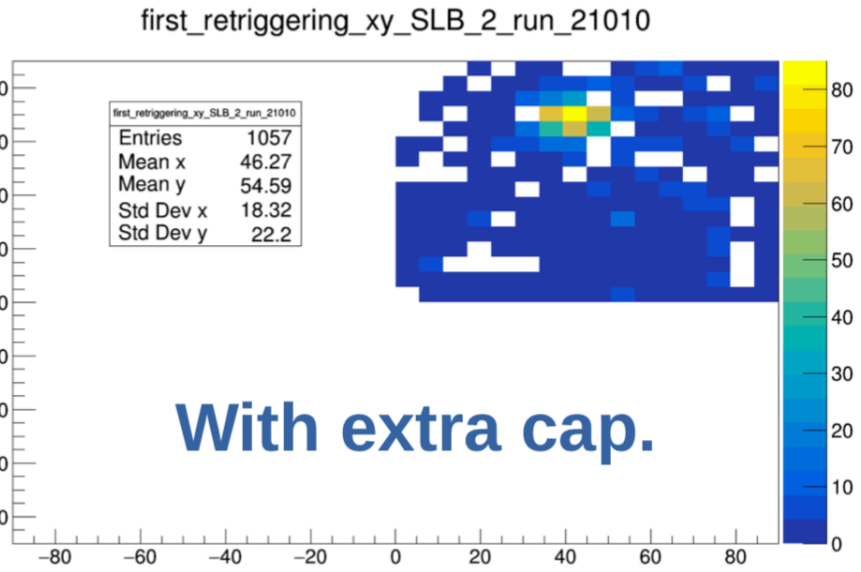
- FEV11 TB2017.
  - Correlation of about 5-10 bcids

A. Irles, in SiW-ECAL Meeting

COB-a: with and without extra capacitances

- ***RE*- TRIGGERS:**
- Before adding the capas. Lots of retriggers in the nearby of the SLBoard !!
- After adding the capas, we have a maximum of 80 rettrigers trains over 3500 good hits, in the beam spot ! So they may not even be retriggers, just overfiltered signals.





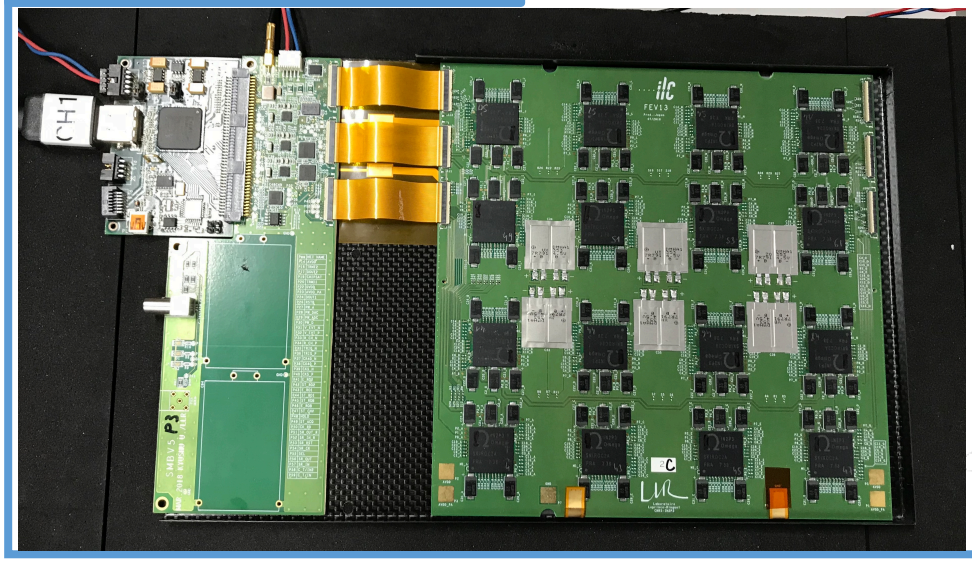
A. Irles, in SiW-ECAL Meeting

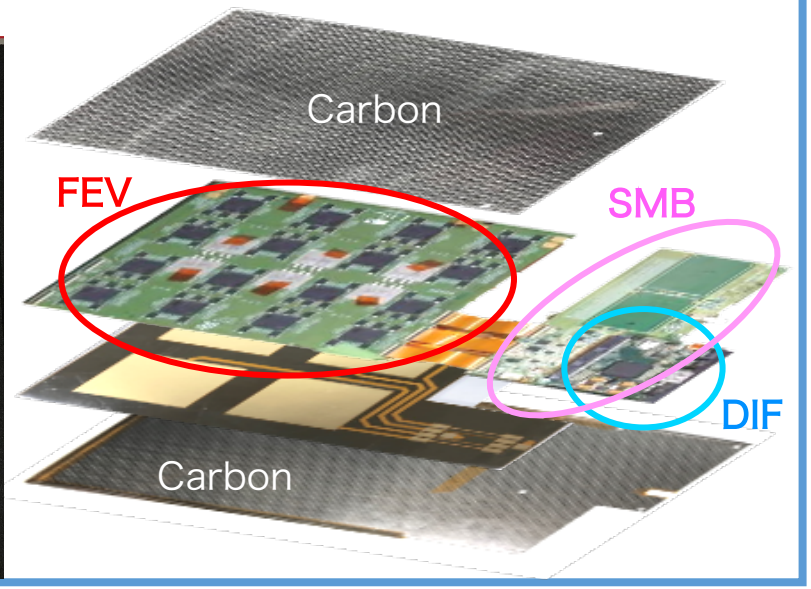
Latest Prototype: FEV13 & SMBv5

Major update from last version

- ASIC: SKIROC2 → 2A
  - individual threshold control
  - improvement on TDC resolution
- Separation of power layers
  - power supply for analogue and digital
  - improvement on noise level
- Capacitor for Power Pulsing
  - 0.4 mm thickness, 40 mF x 6
- Smaller SMB footprint
- New frame/cover
  - made of carbon fiber

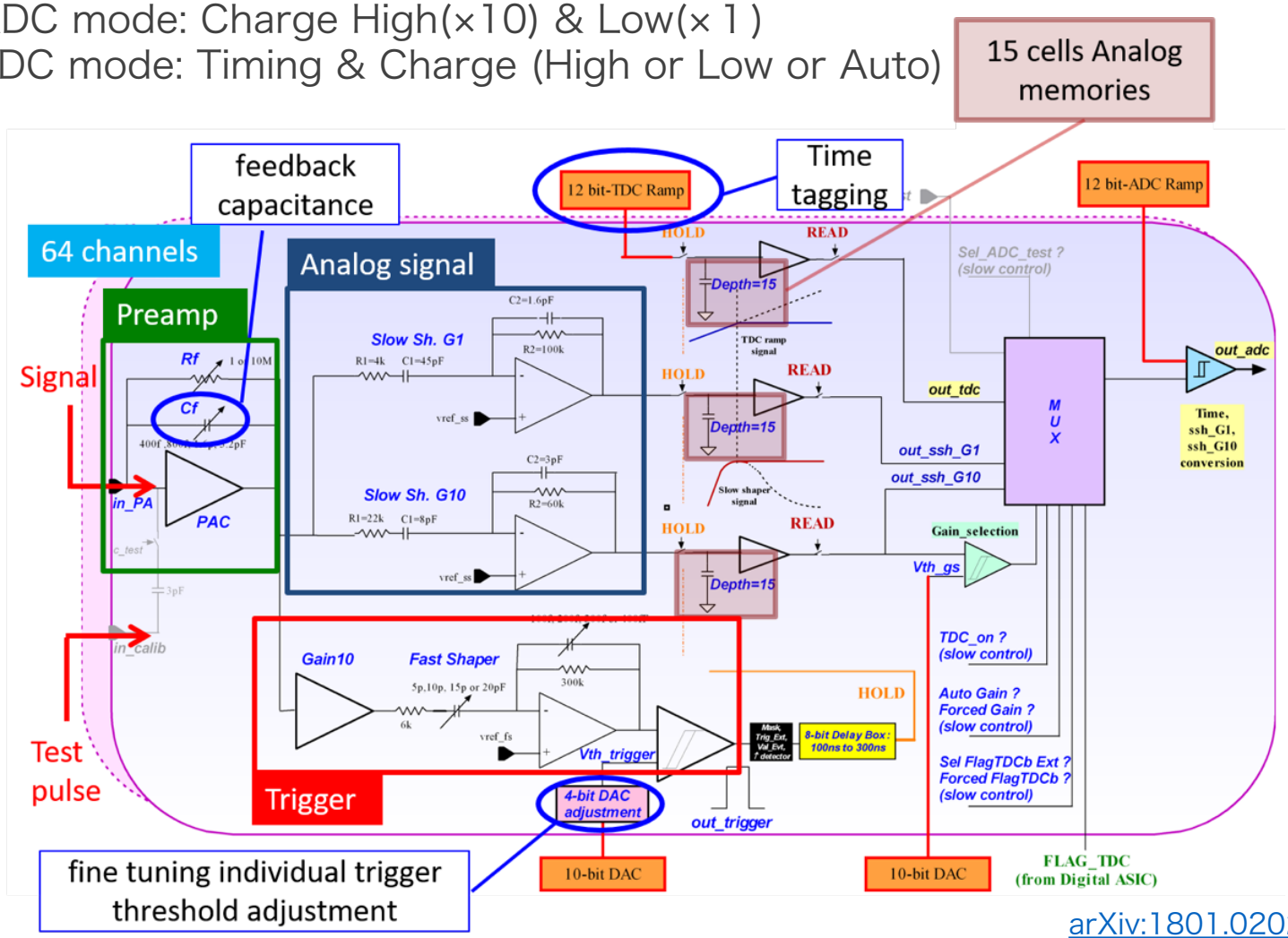
FEV13-Jp





SKIROC2A: Analogue core

- Outputs
  - ADC mode: Charge High(×10) & Low(×1)
  - TDC mode: Timing & Charge (High or Low or Auto)

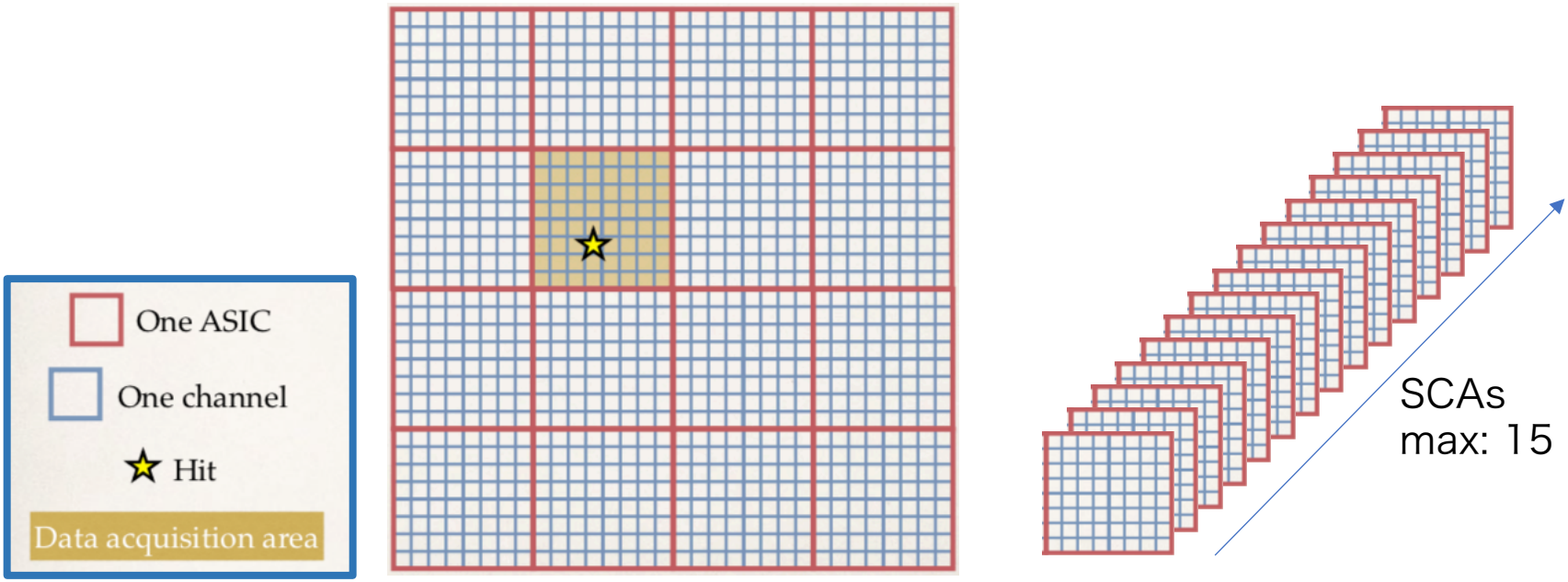


arXiv:1801.02024

Data acquisition mechanism of FEVs

- **Readout mechanism**
  - independently on each ASIC

1. Some tracks are triggered within one BCID interval (0.2 μs)
2. Analog outputs from all channels are stored in memory cells (15 SCAs)
3. After the acquisition phase, all stored data is read out and memory cells are reset.



Discrimination Method

- Example:
  - The variables are saved in each time consecutive bcids are found.