# Extension of the e-Long Slab

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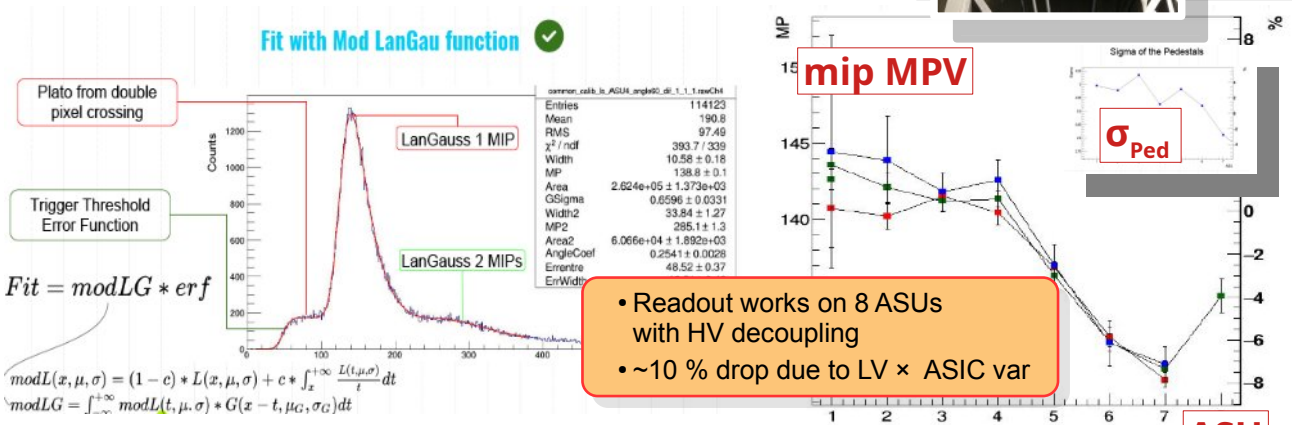
***CALICE Meeting***
***"everywhere"***
***28/09/2020***

# 1st ‘electric long slab’ (2018)

## Support of interface boards + 12 ASUs (DBD)

- 2+6+4 ASUs = ~3.2 m
- Rotatably along long axis (for beam test)

  Rigidity : ≤ ~1 mm per ASU
- Total access to upper and lower parts
  - 320µm Baby wafers (4×4 pixels) on the bottom







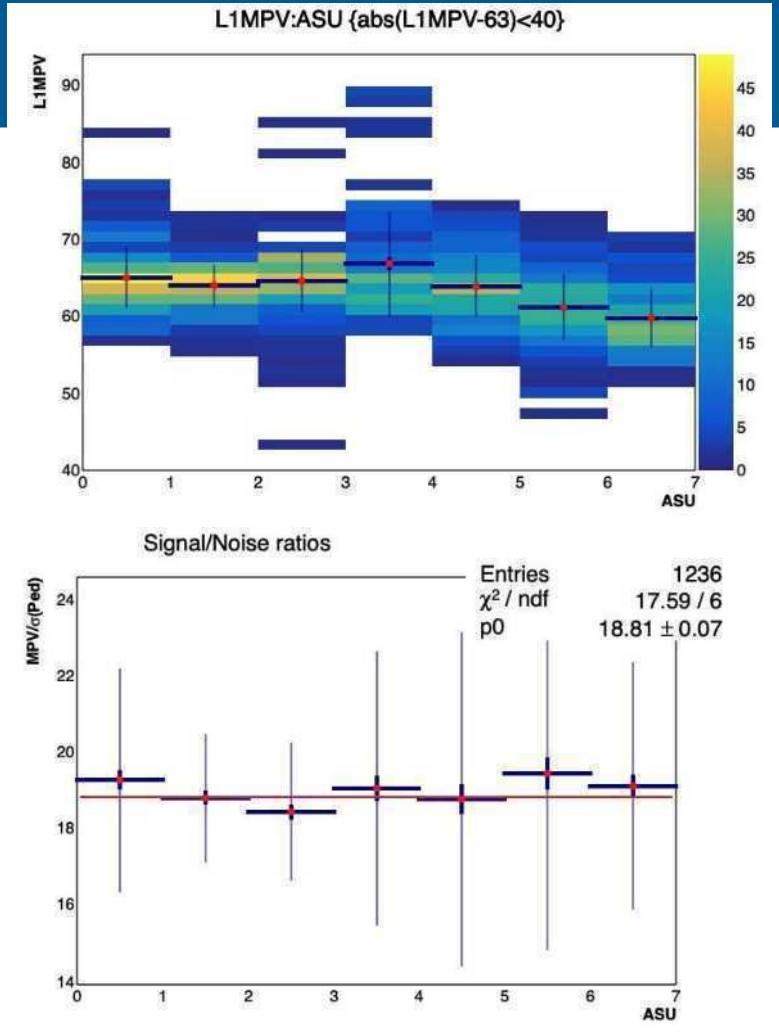
- Readout works on 8 ASUs with HV decoupling
- ~10 % drop due to LV × ASIC var

# Signal over Noise ratios

**The signal-to-noise ratio is defined as the most-probable-value (mpv) of a mip* divided by the pedestal width.**

- in highly granular (self-triggering) calorimeters, a noise cut above 5–6 σ is mandatory, while a cut at ½ mip will ensure a good efficiency, resulting in S/N>10–12.
- A constant S/N ~ 19 is observed in the readout branch unaffected by the variations of the gain along the slab.

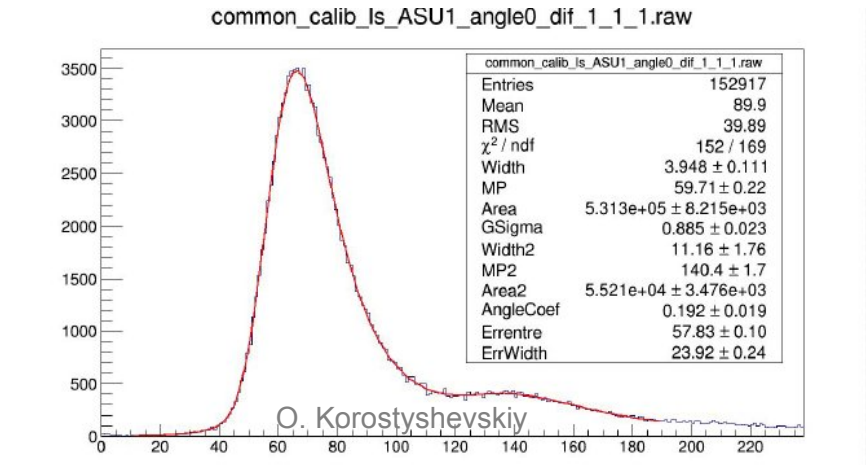
**mip* = [punch-through electron]**

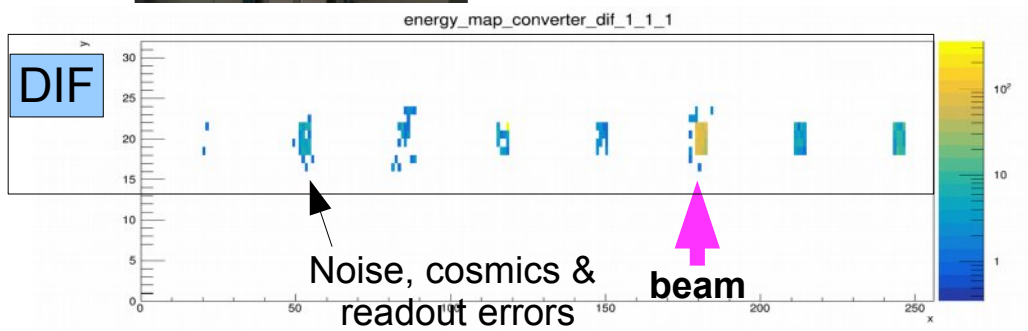


# DESY-2018 beam test

**2 weeks beg of July: full test of all prototypes:**

- Electric long slab: **8 FEV11** + baby-wafers
- Very clean response to “mip” (punch through e-)
- 1/2h beam on each ASU @ 0, 45, 60°



# Electronics adjustments

## Path length induced reflexions on clock line

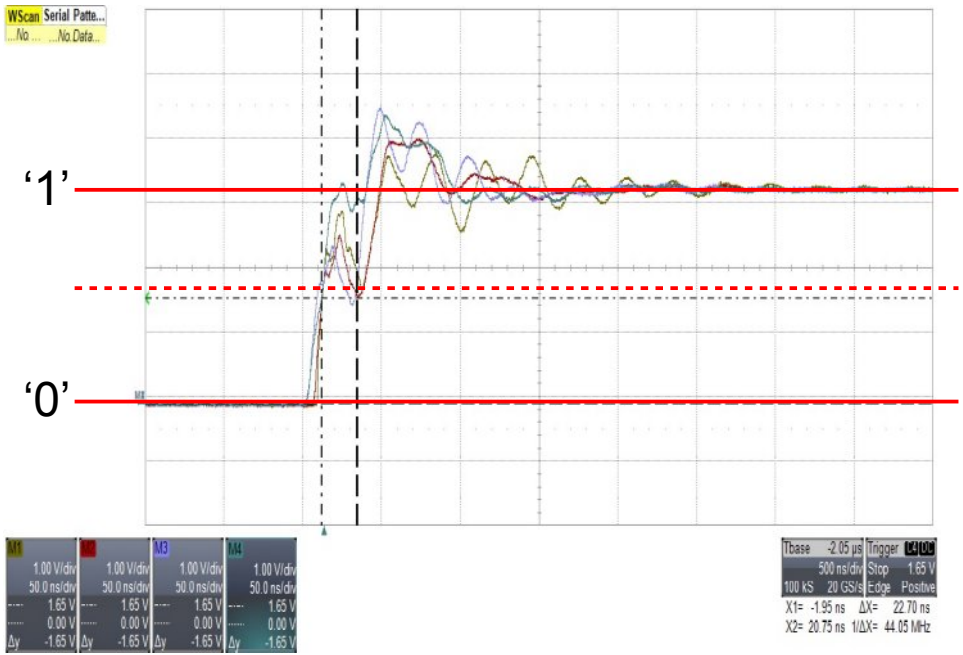
- Fluctuation over logical level
- Extra clock tick ⟶ bad ASIC configuration
- RC filter adaptation (Sigrity simulation)

## Impedance adaptation required depending on length

- **Limited to 8 FEV12** + baby-wafers

## Noise in the signal

- High frequency perturbation in the HV line
- Solved by RC filters on the HV line
  - Possible back-propagation of ASICs noisy channel through HV ?

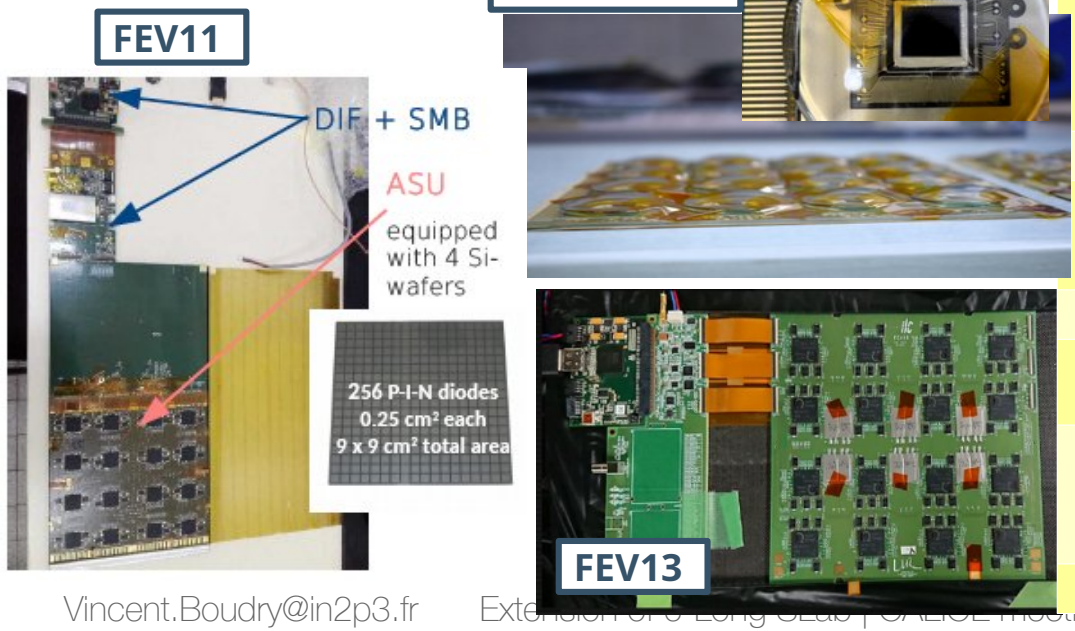



Also issues on the data routing...

# ASU: 11 years of R&D

## Most complex element: electro-mechanical integration

- Distrib / Collect signals from VFE (ASICs), Analog & Digital with dyn. range ≥ 7500
- Mechanical placer & holder for Wafers → precision
- Thickness constraints



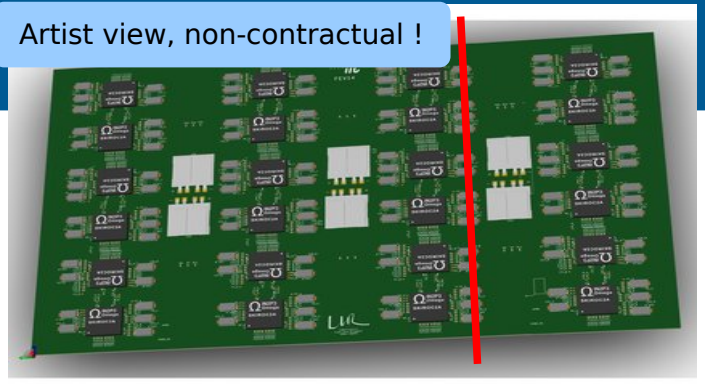

| Milestone | Date | Object | Details | REM |
|---|---|---|---|---|
| 1st ASIC proto | **2007** | SK1 on FEV4 | 36 ch, 5 SCA | proto, lim @ 2000 mips |
| 1st ASIC | 2009 | SK2 | 64ch, 15 SCA | 3000 mips |
| 1st prototype of a PCB | **2010** | FEV7 | 8 SK2 | COB |
| 1st working PCB | 2011 | FEV8 | 16 SK2 (1024 ch) | CIP (QGFP) |
| 1st working ASU in BT | **2012** | FEV8 | 4 SK2 readout (256ch) | best S/N ~ 14 (HG), no PP retriggers 50–75% |
| 1st run in PP | 2013 | FEV8-CIP | | BGA, PP |
| 1st full ASU | **2015** | FEV10 | 4 units on test board 1024 channel | S/N ~ 17–18 (High Gain) retrigger ~ 50% |
| 1st SLABs | 2016 | FEV11 | 7 units | |
| pre-calo | **2017** | FEV 11 | 7 units | S/N ~ 20 $(12)_{Trig,}$ 6–8 % masked |
| 1st technological ECAL | 2018 | SLABvFEV11 & FEV13 SK2a+ Compact stack Long Slab | SK2 & SK2a (⊃timing)<br>8 ASUs | Improved S/N Timing... |
| 1st working COB | 2019 | FEV-COB | 2×1/4 ASUs | |

# Potential FEV14 (2021 ?)

FEV13b?

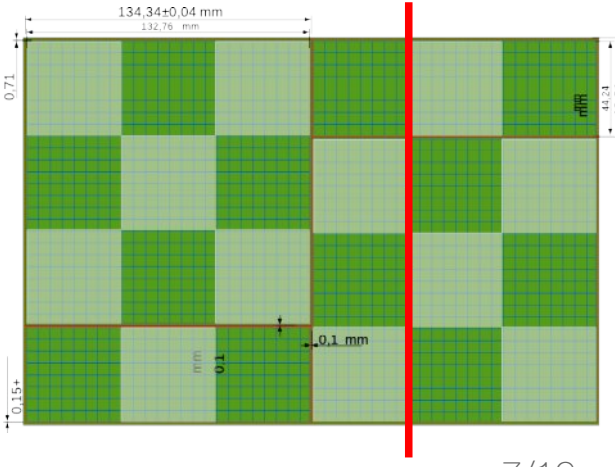
HPK « No 8" wafer bef. end 2021 »

Artist view, non-contractual !



## FEV14: Design PCB *just started*

- Compatible 8" et 6" wafers ; → dimensions×1.5 (18×27 cm²)
  - 6 Matrices 6" OR 2 × 1,5 Matrices 8"
- 24 ASICs vs 16 ASICs
  - Less cards ⇒ Less connections
- Improved scalability & maintenance
  - 1 HV per card ⇒ independent test, exchangeability
  - Bloc diagrams ⇔ Sharing BGA / COP ?
- LV Regulation on board with LDO ?
  - + monitoring ? T°, V, ID (⇔ DB)
- Corrected data & clock distributions
  - Must be OK for 2,1 m (EndCaps) = 8 FEV14 (12 FEV12)
  - Timing ≤ 0,1 ns ? → for SK3 ?
- Compatibility new DAQ (≠ FEV13)

# A Long Slab with “FEV13b”

**Adaptative design wrt FEV12**

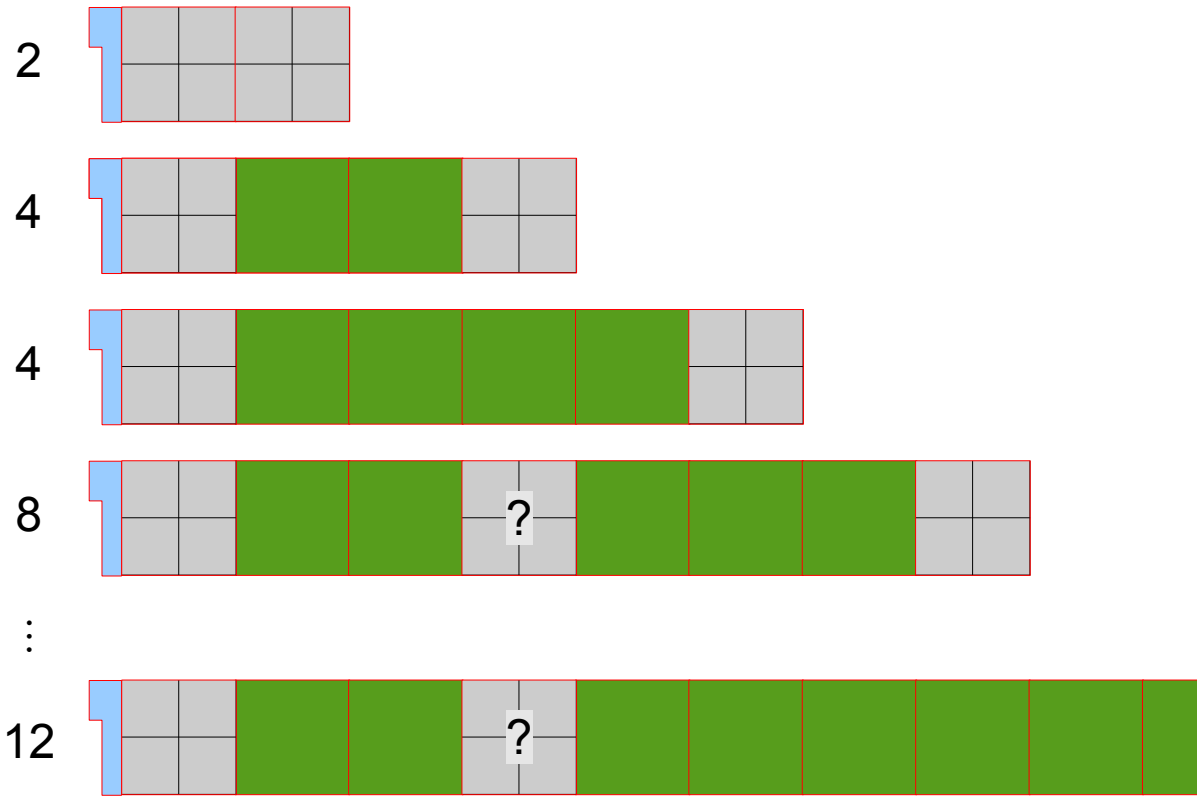
- Integration of new DAQ with Power Scheme
  - (see Jihane presentation)
- Possibility to include FEV13b-COBs in LS

**Modular design :**

- Incremental length

**Full equipped ends of SLAB**

- 1st and Last ASU
- Regulators / Decoupling on each ASU
  - Shower response at end of SLAB
- Possible integration new ASU’s in stack



# First steps (2020):

**Test LDO's scheme in situation**

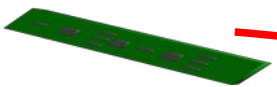
- Several implementation on small insert mezzanine between ASU's
- Measure stability and behaviour in PP

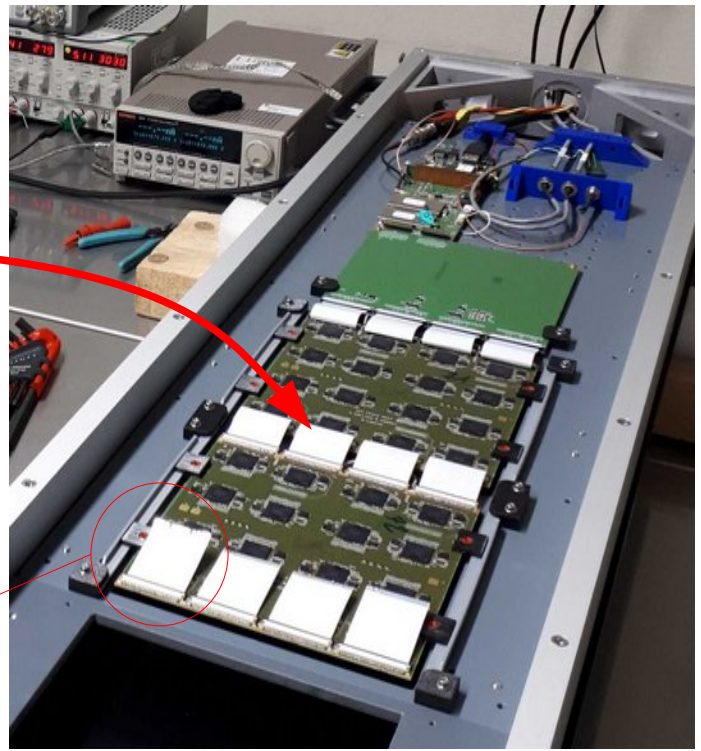
**Implement the interface with SLBoard (v2)**

- for Power Pulsing testing
  - remove / raise current limitations

**Package additionnal SK2a's**

- Test them





Compatible
with GradConn

# Implication of HL schemes

## Higher $\mathscr{L} \Rightarrow$

- Occupation / bunch train ↗
  - More memory for events
    - But large margins

## Higher repetition rates × longer bunch

- Power = $f_{rep} \times \sum P_{ASIC\_part} \times \tau_{spill\_part}$
  - $\tau_{spill} = \tau_{Ramp\text{-}up} + \tau_{Train} + \tau_{Conv}$
    $= \mathcal{O}(\mu s) + \{ \ldots \} + \mathcal{O}(100\text{'s } \mu s)$
    - $\tau_{Train} = \Delta T_{bunches} \times N_{bunches}$
    - $\tau_{Conv} \propto$ (occupancy + Noise ≥ thr.)

**Critical also for Power budget**

**⇒ Full ZERO suppr. needed**

## HL-ILC:

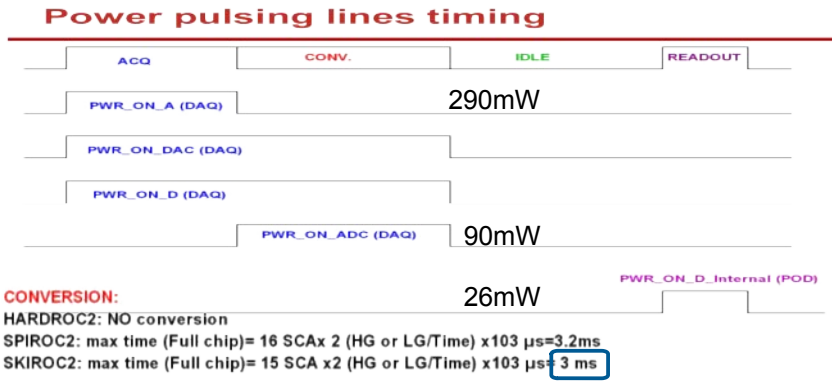
- $\mathscr{L}$ × 4 (6)
- $N_{bunches}$ × 2 : $\tau_{Train}$ : 1 → 2 ms
- $f_{rep}$ ×2 (3): 5 → 15 Hz

**Dominated by ACQ time:**
**P(~25µW/ch) × 6**

## HL-CLIC:

- $\mathscr{L}$ × 2
- $N_{bunches}$ → : $\tau_{Train}$ : 176 ns
- $f_{rep}$ ×2 : 50 → 100 Hz

**Dominated by Set-up & Conversion time: P (~82µW/ch) ×2**




**SK2 chips**

64 ch full conversion

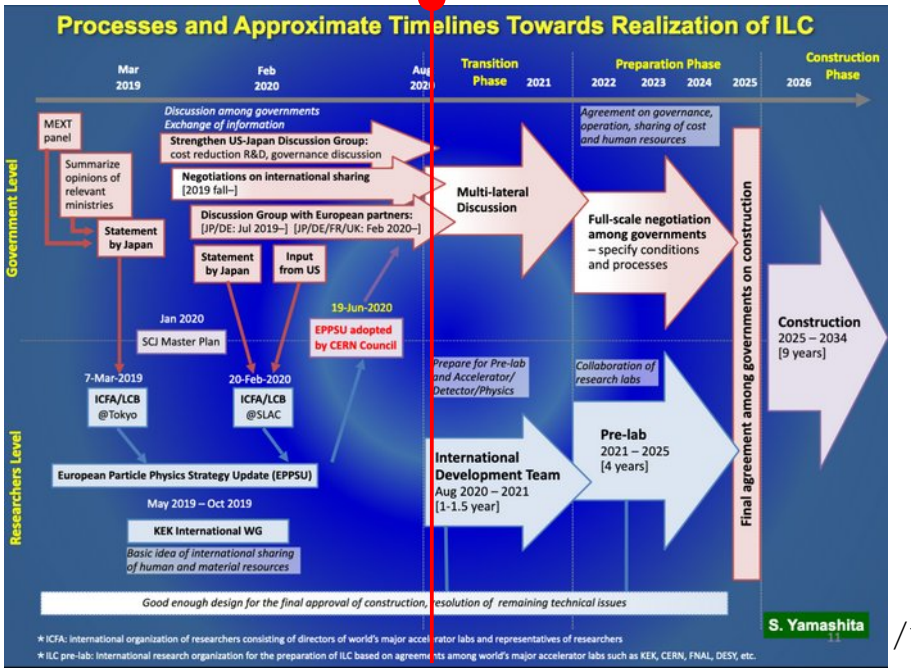
# Perspertive: Just In Time ?

Start of production of calorimeters in 2026 ?
- ➥ Preparation of production in 2025
  - ➥ Pilote ECAL Module in 2024
    - ➥ Pilote of SLABs in 2023
      - ➥ 1st SLAB in 2022
        - ➥ 1st ASU in 2021

⇐ achievable with LHC φ2 ?

⊃ all mechanical constraints

We are standing here



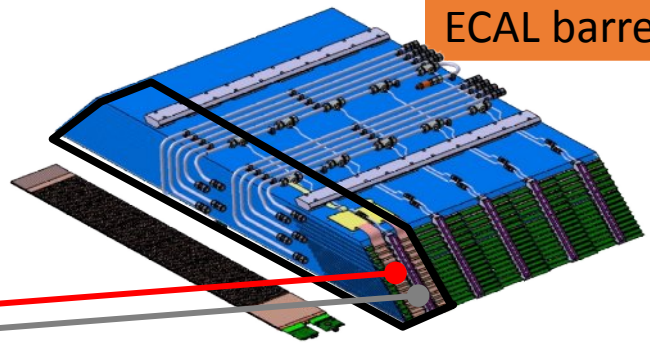

Power & Thermal simulation to be reviewed
- HL scheme

Final ASIC ≥ 2022
- Consumption & Timing

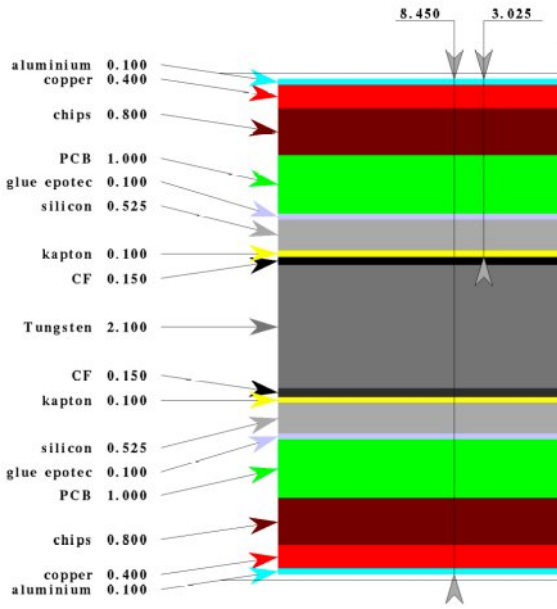
# Back-up

# Passive cooling


ECAL barrel

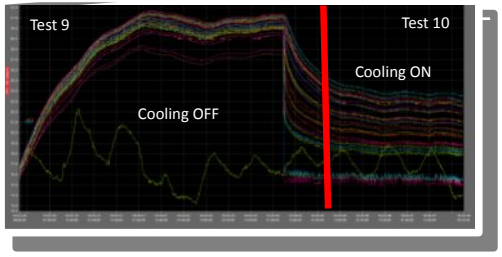


3.0mm Det
+ 2.1mm W



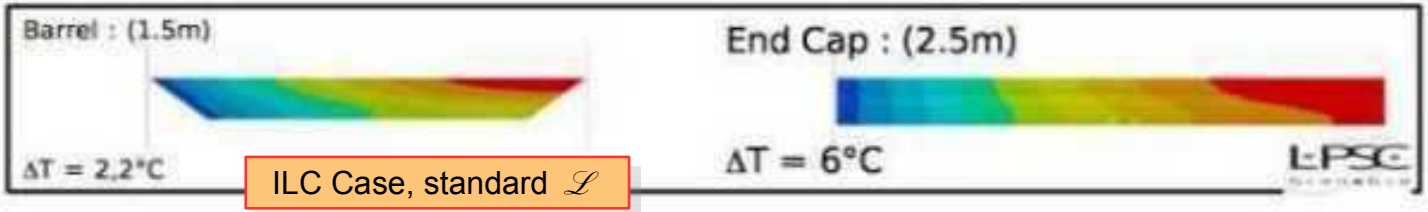


EUDET module (carbon structure) equipped with it's heat exchanger 15 slab in EUDET module




ECAL end cap

First tests results in line with simulations

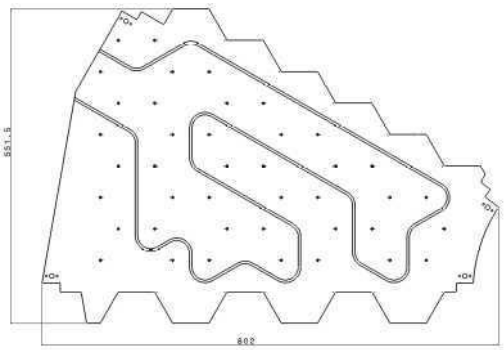



ILC Case, standard $\mathscr{L}$

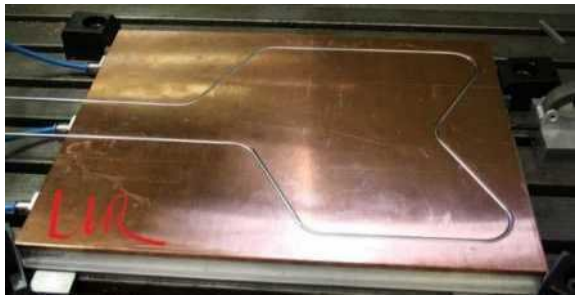
AIDA report 08/18
http://cds.cern.ch/record/2624680

# Active cooling → 'Continuous colliders'

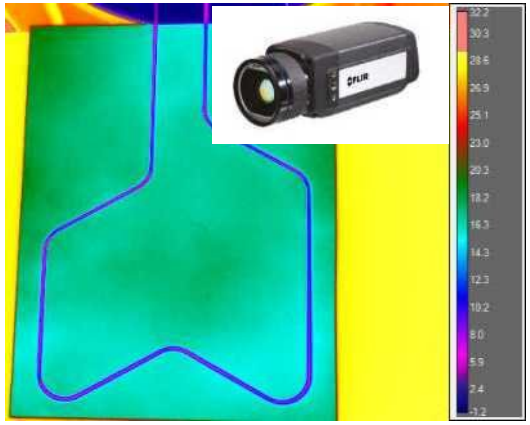
*R&D using CMS studies (Courtesy of Th. Pierre-Emile from CMS-LLR group)*

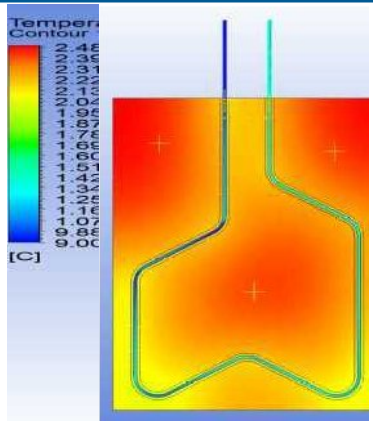


*Copper plate prototype dimensions information*



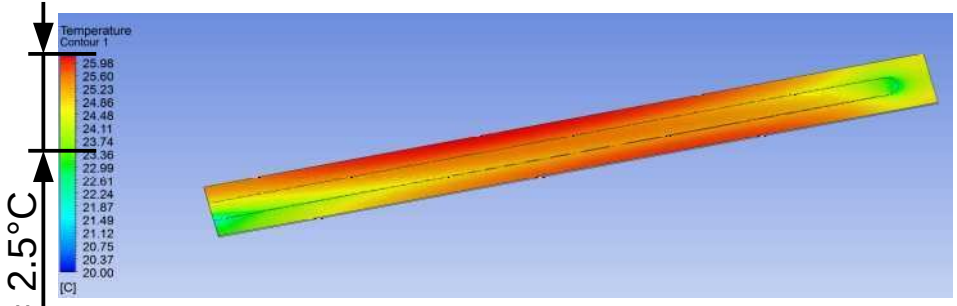
*Pipe insertion on a cooling prototype for FEA correlation*



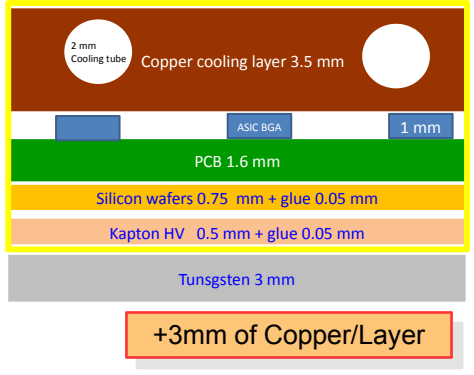


*Pipe insertion on a cooling prototype*

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling




*Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe*




**= 2× cont. operation of a SLAB**

# MIP fluctuation

**2 systematic effects has been identified**

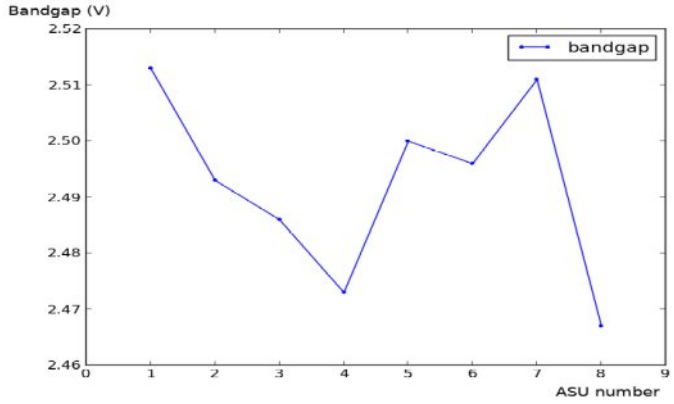
- Bandgap discrepancy (over 128 ASICs).
  - σ=19.2 mV peak to peak=200mV
- Voltage linear decrease over slab length

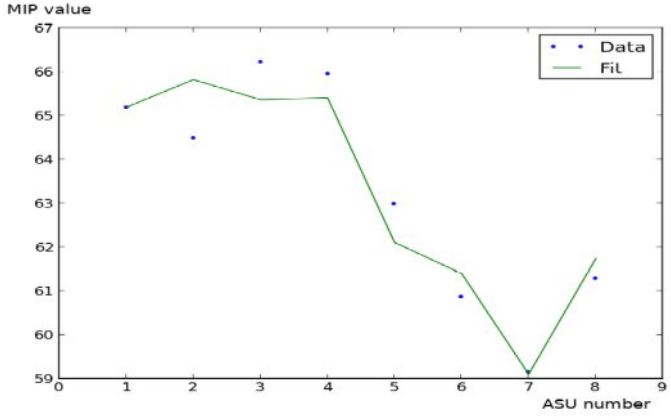
**Curve shape can be fitted by weighted sum of these two effects**

$$MIP(\mathrm{ASU}) = a * \mathrm{ASU} + b - c * \mathrm{bandgap}(\mathrm{ASU})$$

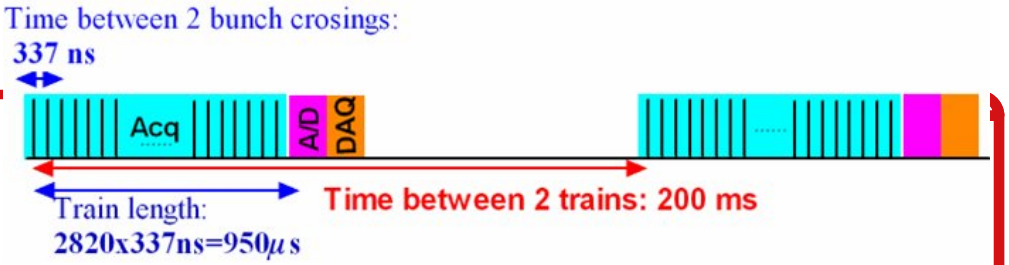
**Solutions**

- Reduce bandgap in ASIC design (already reduced in Skiroc2a version)
- Compensate bandgap by software
- Select ASICs to mitigate fluctuation
- Use fixed length power supply to avoid discrepancy

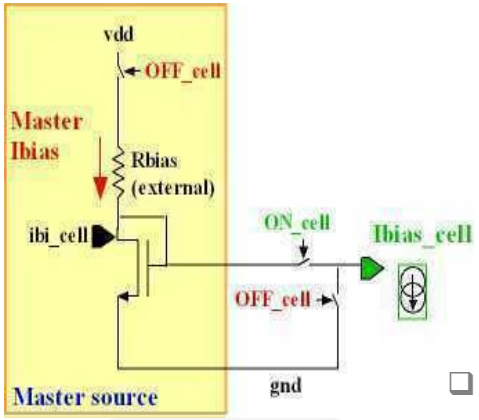


# POWER PULSING in SK2




- **Requirement:**
  - **25 µW/ch with 0.5% duty cycle**
  - **500 µA for the entire chip**




- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **SK2 power consumption measurement:**
  - 123 mA x 3.3V ≈ 40 mW => **0.6 mW/ch**
- **4 Power pulsing lines** : analog, conversion, dac, digital
- Each chip can be forced **on/off by slow control**

| Measurements | | |
|---|---|---|
| **Acquisition** | 88 mA , 290 mW | Duty Cycle =0.5%, 1.45 mW |
| **Conversion** | 27.3 mA, 90 mW | Duty Cycle =0.25%, 0.225 mW |
| **Readout** | 8.0 mA, 26.4 mW | Duty Cycle =0.25%, 0.066 mW |

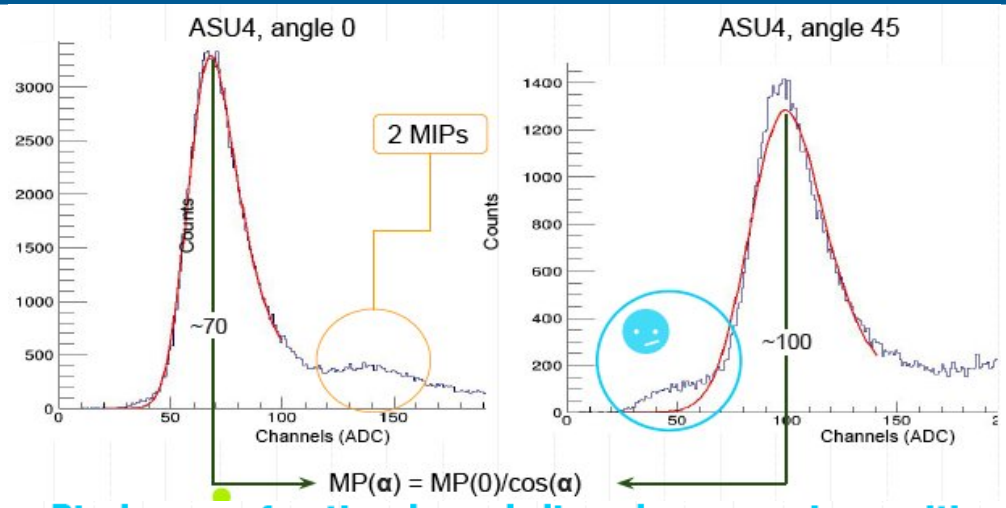
**Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 µW/ch**

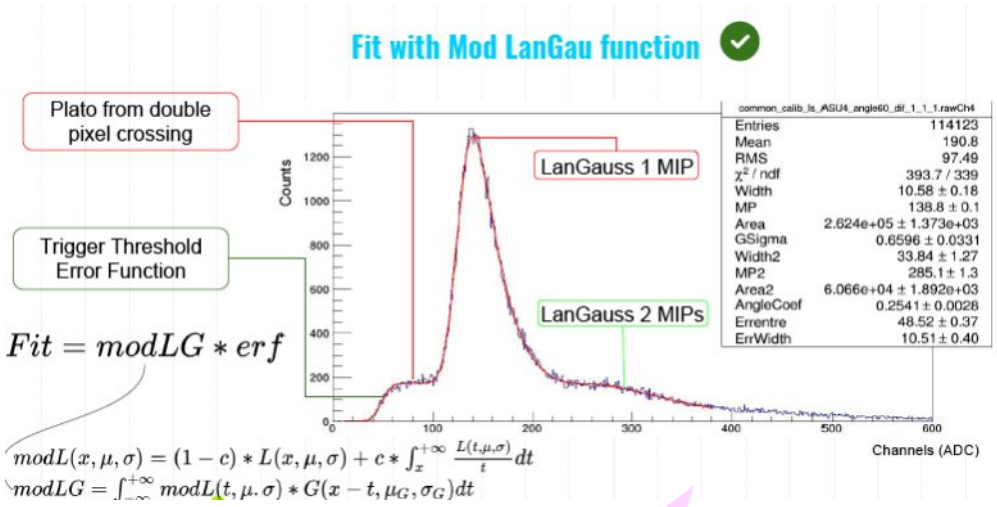
# Power estimations

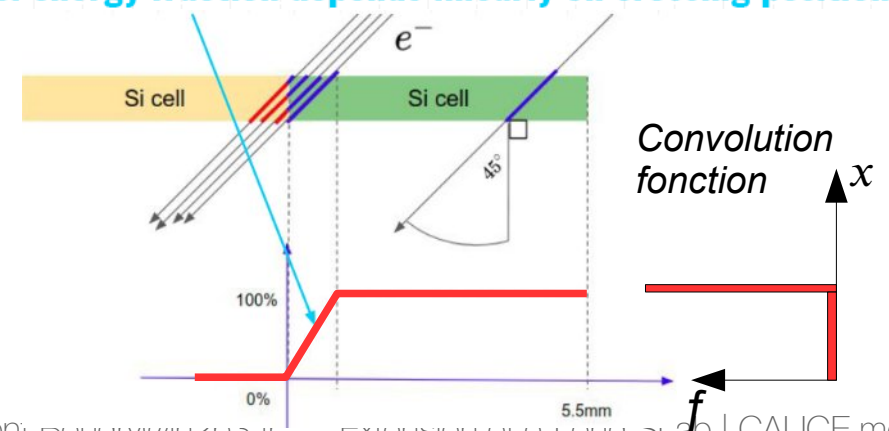
| | mW |
|---|---|
| P_ACQ | 290 |
| P_CONV | 90 |
| P_RO | 26 |

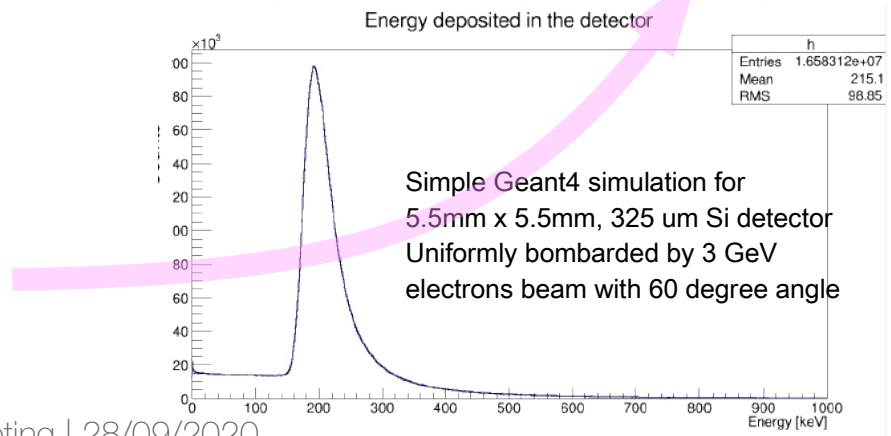
| | TAU_PO/ms | E_PO/µJ | **Tau_SPILL/ms** | E_ACQ/µJ | τau_CONV/ms | E_CONV/µJ | E_SPILL/µJ | f_rep/Hz | P_TOT/µW | P_TOT/µW/ch | Ratio HL/Lumi |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **ILC** | 0,005 | 1,450 | 1,000 | 290,000 | 0,10 | 9 | 300,45 | 5 | 1502,25 | 23,47 | |
| HL-ILC | 0,005 | 1,450 | 2,000 | 580,000 | 0,20 | 18 | 599,45 | 15 | 8991,75 | 140,5 | 5,99 |
| CLIC | 0,005 | 1,450 | 0,176 | 51,040 | 0,02 | 1,58 | 54,07 | 50 | 2703,7 | 42,25 | |
| HL-CLIC | 0,005 | 1,450 | 0,176 | 51,040 | 0,02 | 1,58 | 54,07 | 100 | 5407,4 | 84,49 | 2 |

# Mip analysis



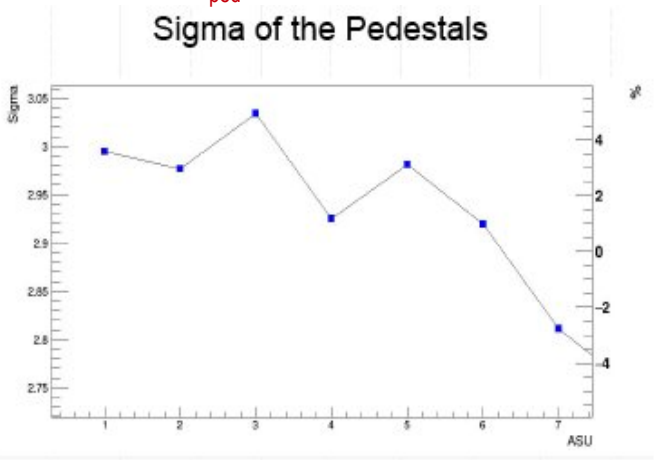



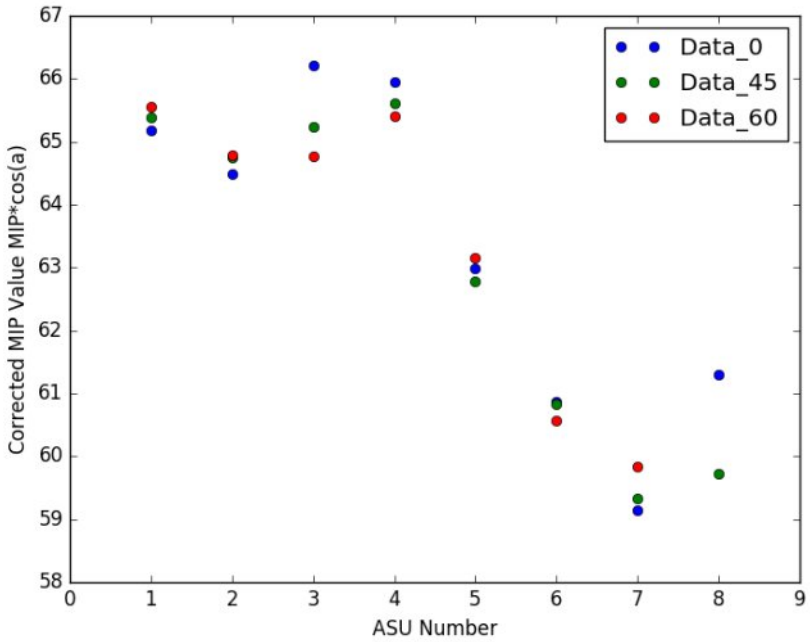



# MIP response vs position

**mip MPV *cos(θ) vs ASU#**

- OK for 4 1st ASU's
- Small drop ~of signal ~2%/ASU for ≥ ASU#5
- Also hints similar drop on $\sigma_{ped}$




**⇒ Voltage & Gain drop ?**

Power pulsed mode with ballast et end of slab
(or just random build-up effect from chip variability ?)