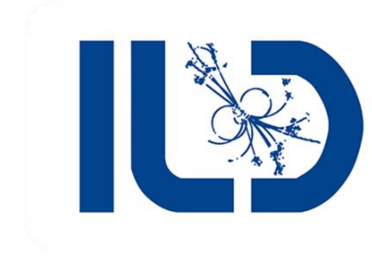
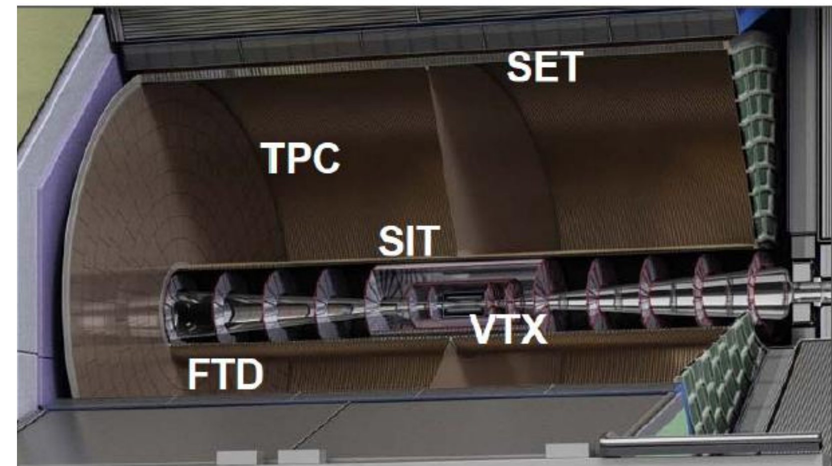


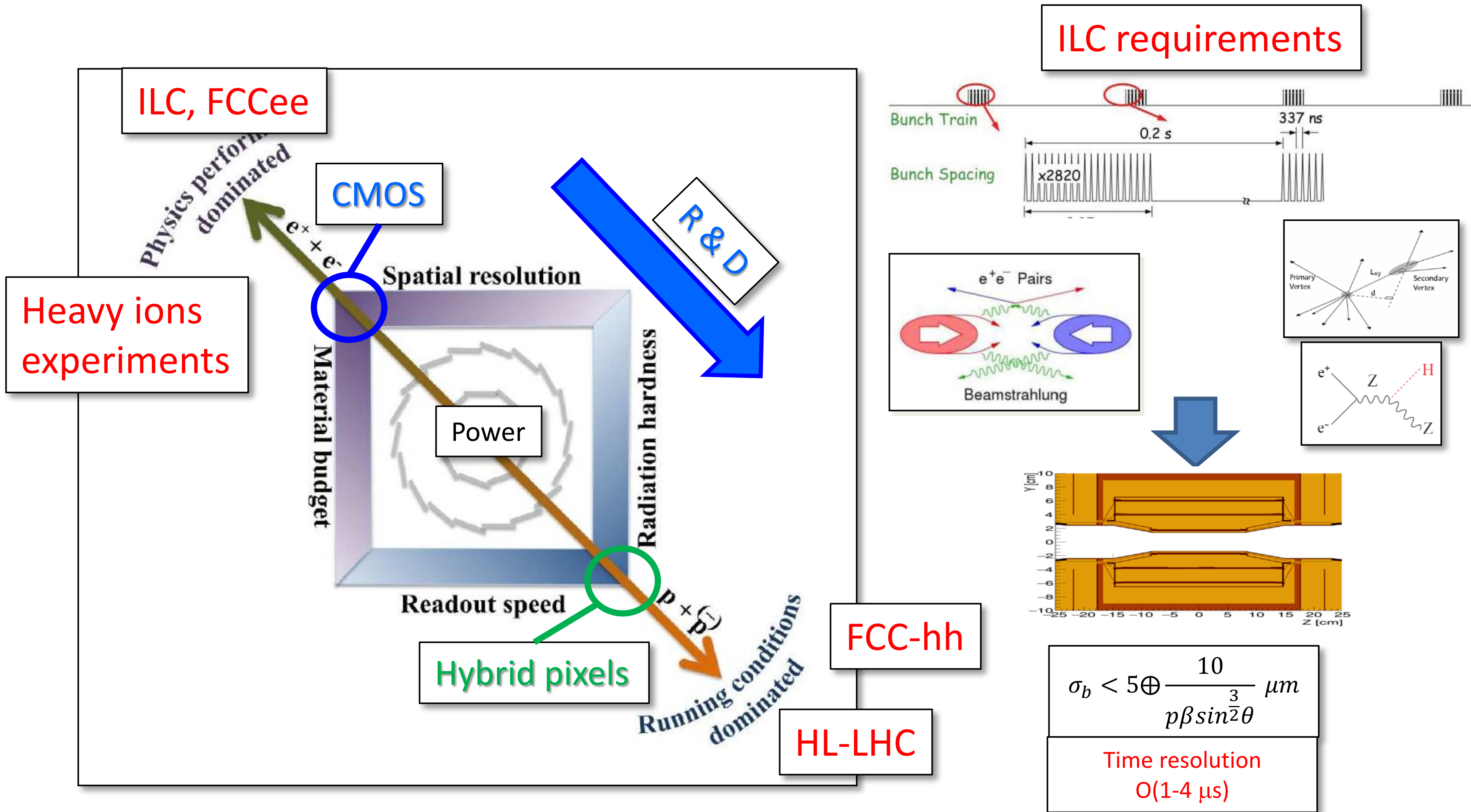
Vertex detector R&D status

Akimasa Ishikawa, Marcel Vos, Auguste Besson
(and thanks to Marc Winter, Yasuhiro Sugimoto)

- Vertex detector reminder
- Technologies
  - CCDs
  - DEPFET
  - SOI
  - CMOS
- Summary

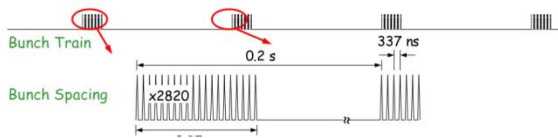


Vertex detector technology figure of merit

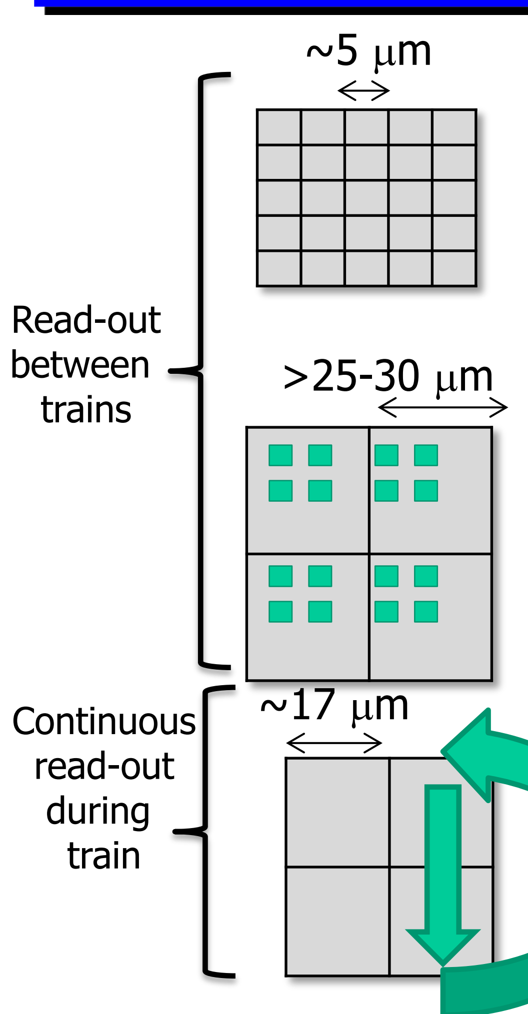


➩Keep excellent spatial resolution and push towards better time resolution

➩Strong synergy between Higgs factories and Heavy ion experiments



Read-out strategies and technologies



Power	Time resolution	Spatial resolution	Advantages	Caveats
Fine pixels (e.g. FPCCD)				
Low	1 complete train	~ 1 μm	Spatial Resolution Hit separation Beam background tagging capabilities ? (cluster shapes)	⇨x16 #pixels to read-out in 200ms ⇨No time stamping ⇨Occupancy issues ?
In pixel circuitry to store hits with time stamping (e.g. chronopixels, SOI)				
Low	Single or few bunches (>~ 0.5 μs)	>~ 5 μm	Hit time stamping Well suited to outer layers	⇨BX time stamping storage in conflict with granularity
Continuous read-out during train (e.g. DEPFET, CMOS): rolling shutter or priority encoding.				
High	Few to 10s bunches (1-50 μs)	~ 3 μm	Time & spatial resolution compromise	Power cycling mandatory ? ⇨F(Lorentz) ~ 10^s grams ⇨Distribute 100s Amps shortly before train ⇨heat cycles the ladders.

Technology	FPCCD	DEPFET	SOI	CMOS	iLGAD
Added value (example)	Very granular	Low material budget	2 tier process (high density μcircuits)	Industry evolution	PID

Requirements revisited ?

- Requirement ~ TDR (2012)
- Interim Design Report (IDR) update

Barrel system						
System	r_{in}	r_{out} [mm]	z_{max}	technology	comments	
VTX	16	60	125	silicon pixel sensors	3 double layers at $\sigma_{r\phi,z} = 3.0$ μm $\sigma_t =$ 2-4 μs	$r_0 =$ 16, 37, 58 mm (layers 1-6)
SIT	153	303	644	silicon pixel sensors	2 double layers at $\sigma_{r\phi,z} = 5.0$ μm $\sigma_t =$ 0.5-1 μs	$r =$ 155, 301 mm (layers 1-4)
TPC	329	1770 *1427*[s]	2350	MPGD readout	220 (*163*[s]) layers 1×6 mm^2 pads	$\sigma_{r\phi} \approx$ 60-100 μm
SET	1773 *1430*[s]	1776 *1433*[s]	2300	silicon strip sensors	1 double layer at $\sigma_{r\phi} = 7.0$ μm	$r = 1774$ mm $\phi_{stereo} = 7°$

End cap system							
System	z_{min}	z_{max} [mm]	r_{in}	r_{out}	technology	comments	
FTD	220 645	371 2212		153 300	silicon pixel sensors silicon strip sensors	2 discs 5 double discs	$\sigma_{r\phi,z} = 3.0$ μm $\sigma_{r\phi} = 7.0$ μm $\phi_{stereo} = 7°$

- New beambackground studies
  - ✓ (@ √s = 250 GeV)

ILD_l5_v05	hits/BX mean ± RMS	hits/BX/cm^2 mean ± RMS
VXD 1	914 ± 364	6.64 ± 2.65
VXD 2	545 ± 207	3.96 ± 1.51
VXD 3	129 ± 60	0.213 ± 0.100
VXD 4	107 ± 53	0.177 ± 0.088
VXD 5	40 ± 26	0.043 ± 0.029
VXD 6	34 ± 24	0.037 ± 0.026

Daniel Jeans, Akiya Miyamoto

- Possible Luminosity upgrades

			Z-Pole [4]		Higgs [2,5]			500GeV [1*]		TeV [1*]
			Baseline	Lum. Up	Baseline	Lum. Up	L Up.10Hz	Baseline	Lum. Up	case B
Center-of-Mass Energy	E_{CM}	GeV	91.2	91.2	250	250	250	500	500	1000
Number of bunches	n_b		1312	2625	1312	2625	2625	1312	2625	2450
Bunch population	N	10^{10}	2	2	2	2	2	2	2	1.737
Bunch separation	Δt_b	ns	554	554	554	366	366	554	366	366
Luminosity	L	10^{34}/cm^2/s	0.205	0.410	1.35	2.70	5.40	1.79	3.60	5.11
Luminosity enhancement factor	H_D		2.16	2.16	2.55	2.55	2.55	2.38	2.39	1.93

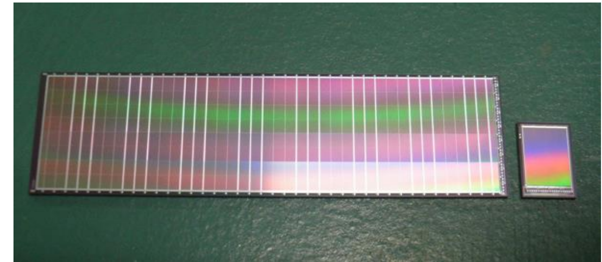
⇨ motivations to push towards better time resolution

FPCCD

FPCCD: Status of sensor R&D

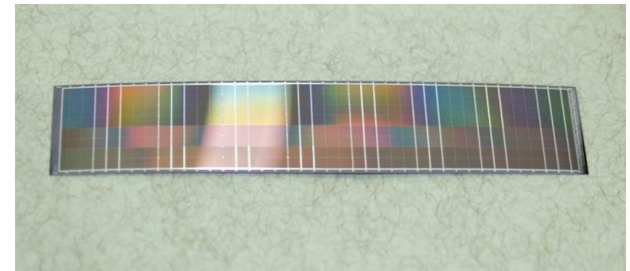
Yasuhiro Sugimoto

- Small prototypes
  - 6μm pixels, 6mm square sensor size
  - 4 readout ports/sensor, with different horizontal register size
  - Standard and thin (50 μm) wafers
  - Neutron radiation damage test has been done → More improvement of charge transfer inefficiency (CTI) is desirable



Large (left) and small (right) prototype

- Large prototypes
  - 62x12 mm^2 sensor size (active area)
  - 8 readout ports/sensor, with 3 pixel sizes (6, 8, 12 μm)
  - Standard and thin (50μm) wafers
  - With and without notch channel



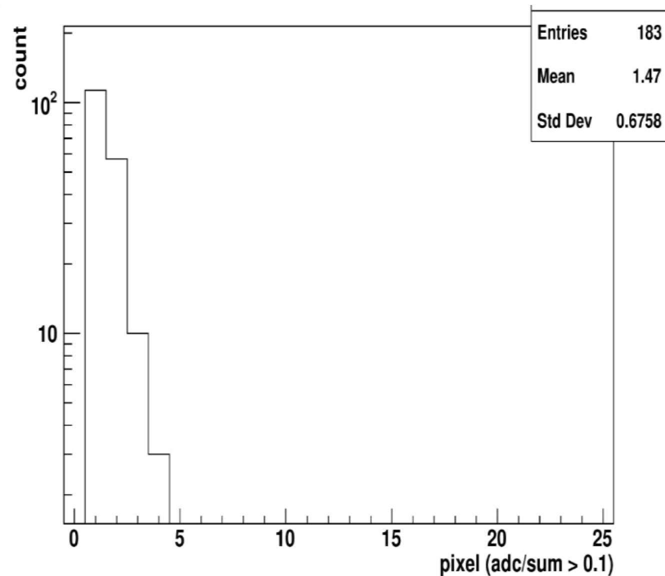
Thinned (50μm) large prototype

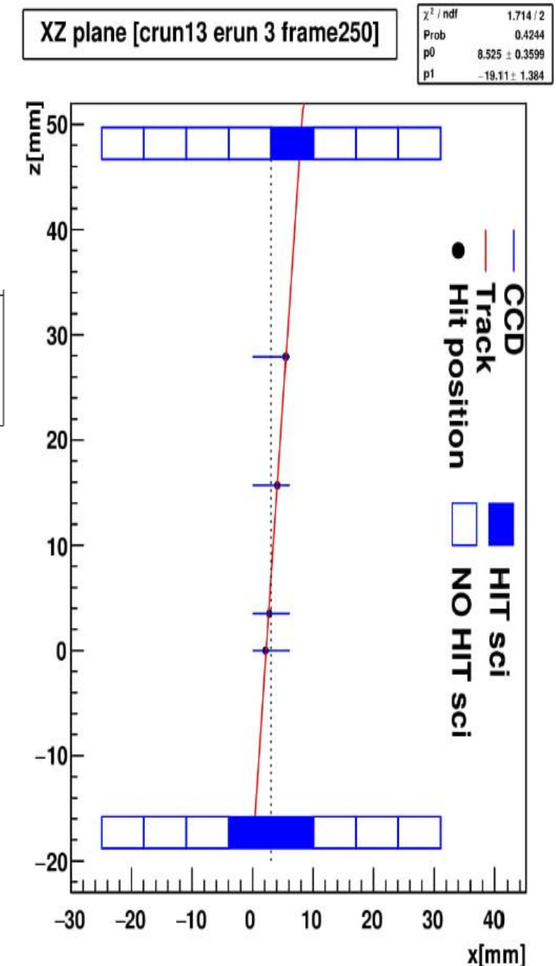
- No new prototypes recent few years

Recent studies

- Cosmic ray test of FPCCD sensors
  - Small (6mmx6mm) prototype sensors with 6 μm pixels
  - ~3 weeks data acquisition
  - Charge spread of the signal has been studied
    - For ~normal incident (<10 degrees) charged particles, the maximum number of the hit pixels was 4

Number of pixels in the cluster for normal incident particles





This result implies an excellent 2-particle separation capability of FPCCD sensors

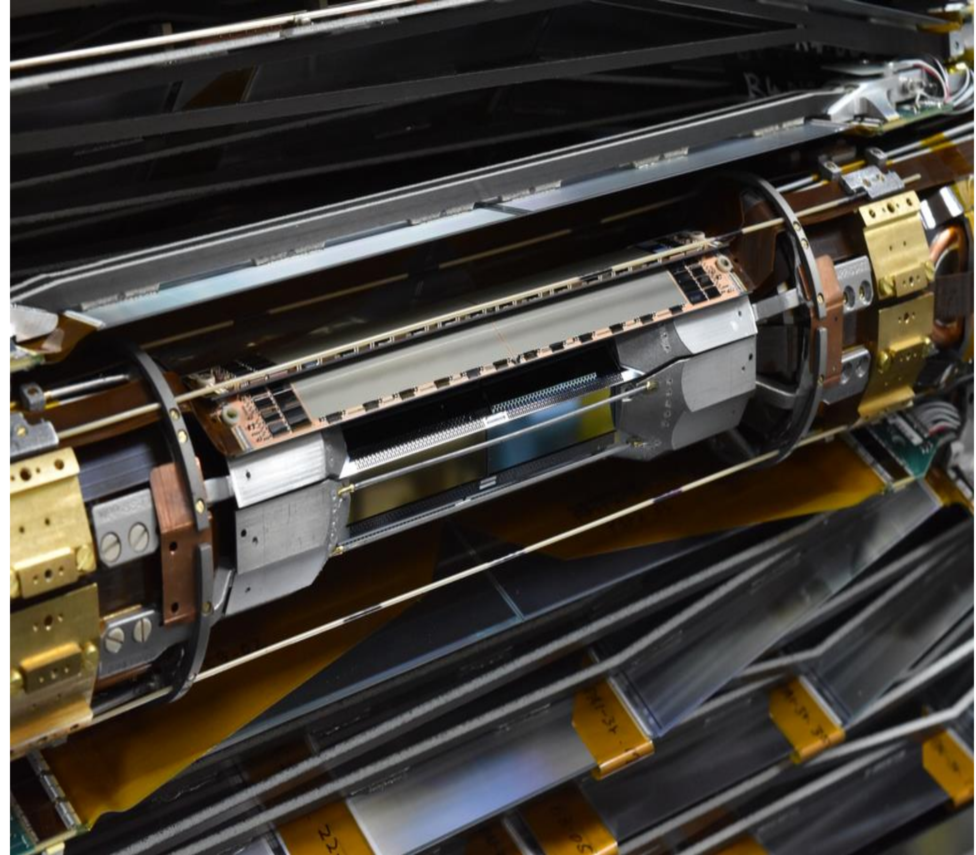
DEPFET

AIDA 2020

DEPFET/BELLE II

- DEPFET pixel detector
- has continued to take data
- in Belle II
- Performance adequate,
- if operation is not without
- problems

- Upgrade plans becoming
- more concrete



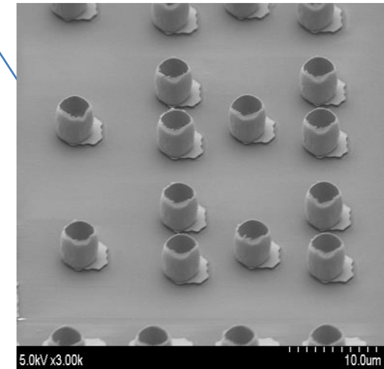
AIDA 2020

SOI and double tier

Development team: KEK- U Tsukuba-TMCIT- Tohoku U- Hokkaido U- Tohoku MicroTec

SOFIST, an SOI based pixel sensor for the ILC

SOFIST: SOI Fine measurement of Space and Time

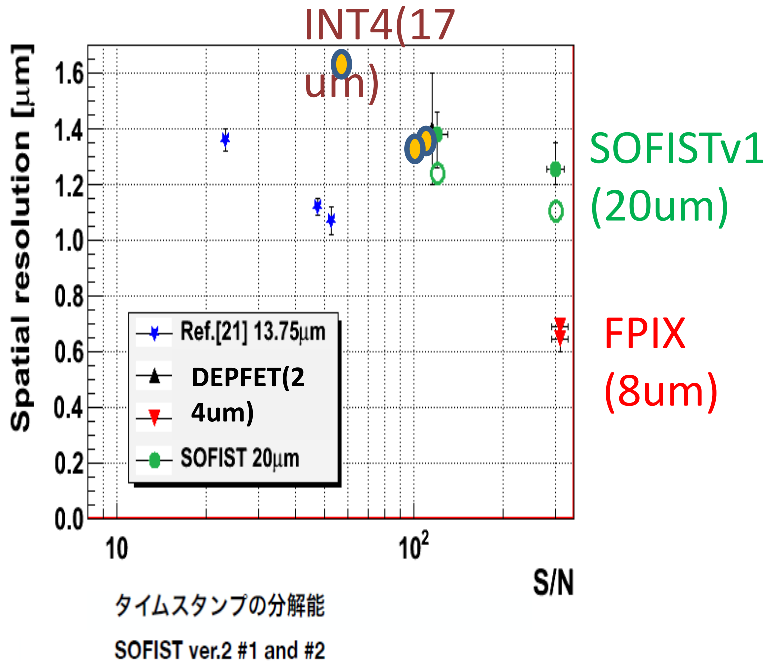


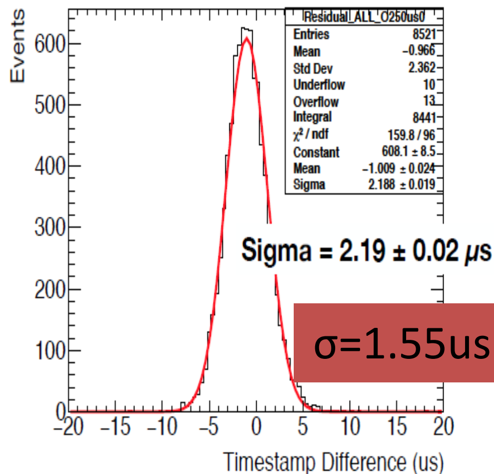
3D stacking using Au micro bumps to implement all features

Features:

- Multiple memories (3/pixel): dead-time less data store possible
- Timestamp data: distinguish hits associating to individual events – σ_t~1.6 us achieved
- 20x20 um pixel size (+ excellent SOI low noise): spatial resolution σ_x~1.2 um achieved
- Readout all memory data (charge and time) in a column by one ADC

Development status





Intrinsic resolution: 2.19/√2 ~ 1.55 μs

- Excellent performance has been demonstrated on the spatial and timestamp resolutions
- 3-deep memory cells deadtime-less readout, 8-bit column ADCs, zero-suppression logic implemented.
- sensor thinning to 50 μm has been verified.
- 3D stacking allows to keep the pixel size small (20x20 μm). SOI is in very good compatibility to the 3D stacking.

However, to adopt SOFIST to the ILC vertex

- Power consumption needs to be lowered. As the demonstrated detector performance is well within the requirements, compromise of the preamplifier speed (hence power) is foreseen.
- have a full size chip (3D stack sensor SOFIST4 is 4.5mm square)
- Periphery circuits: analog power-off in between trains, digitized data transfer, including cooling need to develop

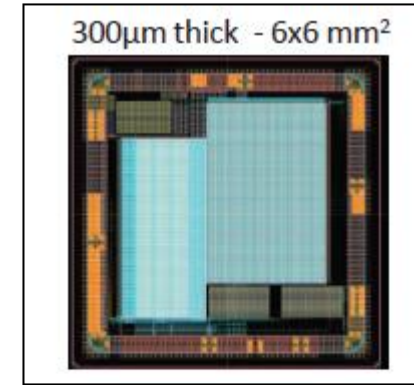
Collaboration with related groups should enhance the development

SOI development at IPHC

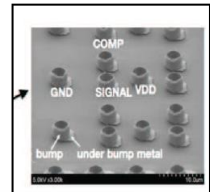
SOIPIX Silicon-On-Insulator Pixel Detector Project

KEK

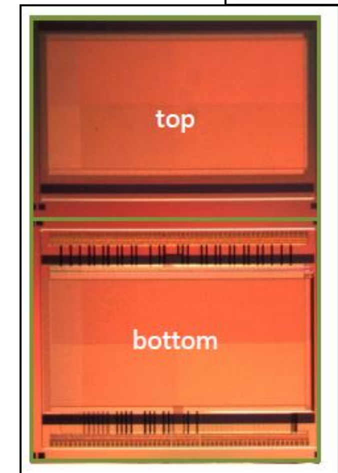
- 2 chips about to be submitted in September 2020
  - ✓ 1st: HEP applications ⇨ test Alpide/Mimosis-like pixels (FE), charge collection
  - ✓ 2nd: imaging ⇨ 192x128 pixels with rolling shutter or global shutter readout.
  - ✓ Complementarity with SOFIST family
- Digital librairies developped in cooperation with KEK.



Double-tier activities @ IPHC

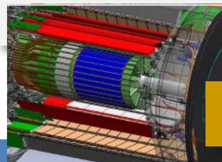


- Double-tier « 3D » in CMOS TJ 180nm technology
  - ✓ Bonding performed by T-micro (same company used for SOFIST)
  - ✓ Bonding pitch = 10 µm.
  - ✓ Pitch = 20 µm
  - ✓ Submitted in feb 2020
- Both chips are sensitive + ouput logic in bottom chip
- Goal: compare
  - ✓ Direct read-out from bottom chip
  - ✓ Read-out after transmission trough bonding from top chip
- Allows to
  - Test capacitive noise between the 2 layers
  - Test pixel dispersion

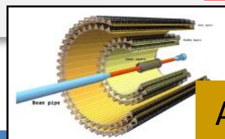


CMOS

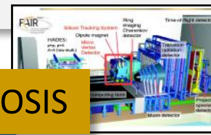
Evolving CPS



ULTIMATE

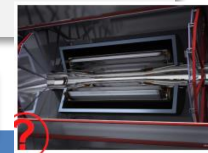


ALPIDE



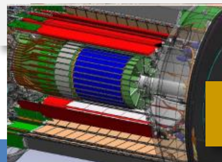
MIMOSIS

PSIRA proposal

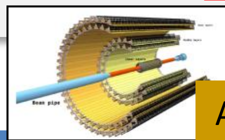


	STAR-PXL	ALICE-ITS	CBM-MVD	ILD-VXD
Data taking	2014-2016	>2021-2022	>2021	>2030
Technology	AMS-opto 0.35 μm	0.18 μm	0.18 μm	0.18 μm (conservative) < 0.18 μm ?
	4M	HR, V_{bias} ~-6V Deep P-well	HR, Deep P-well	?
Architecture	Rolling shutter + sparsification + binary output	Asynchronous r.o. In pixel discri.	Asynchronous r.o. In pixel discri.	Asynchronous r.o. (conservative)
Pitch (μm^2) / Sp. Res.	20.7 x 20.7 / 3.7	27 x 29 / 5	22 x 33 / <5	~ 22 / ~ 4
Time resolution (μs)	~185	5-10	5	1 – 4
Data Flow		~10^6 part/cm^2/s Peak data rate ~ 0.9 Gbits/s	peak hit rate @ 7 x 10^5 /mm^2/s >2 Gbits/s output (20 inside chip)	~375 Gbits/s (instantaneous) ~1166Mbits / s (average)
Radiation	O(50 kRad)/year	$2x10^{12}$ n_{eq}/cm^2 300 kRad	$3x10^{13}$ n_{eq}/cm^2/yr & 3 MRad/yr	O(100 kRad)/year & O($1x10^{11}$ n_{eq}(1MeV)) /yr
Power (mW/cm^2)	< 150 mW/cm^2	< 40 mW/cm^2	< 200 mW/cm^2	~ 50-100 mW/cm^2 + Power Pulsing
Surface	2 layers, 400 sensors, $360x10^6$ pixels 0.15 m^2	7 layers, $25x10^3$ sensors > 10 m^2	4 stations Fixed target	3 double layers 10^3 sensors (4cm^2) 10^9 pixels ~0.33 m^2
Mat. Budget	~ 0.39 % X_0 (1st layer)	~ 0.3% X_0 / layer		~ 0.15-0.2 % X_0 / layer
Remarks	1st CPS in colliding exp.	(with CERN)	Vacuum operation Elastic buffer	Evolving requirements

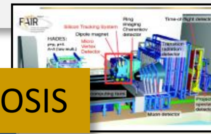
Evolving CPS



ULTIMATE

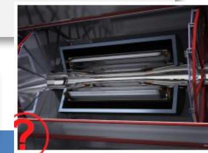


ALPIDE



MIMOSIS

PSIRA proposal



?

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Surface	2 layers, 400 sensors, 360x10^6 pixels 0.15 m^2	7 layers, 25x10^3 sensors > 10 m^2	4 stations Fixed target	3 double layers 10^3 sensors (4cm^2) 10^9 pixels ~0.33 m^2
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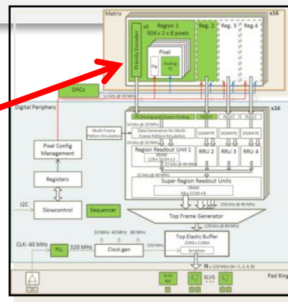
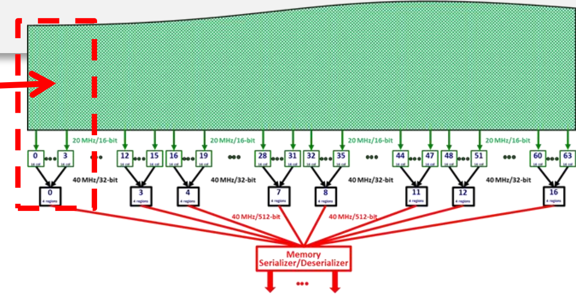
Remarks	1st CPS in colliding exp.	(with CERN)	Vacuum operation Elastic buffer	Evolving requirements

MIMOSIS = one step further to approach ILC requirements
(able to cope with the data flux of ILC)

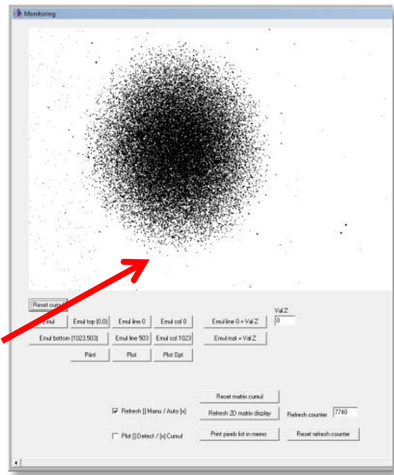
MIMOSIS roadmap



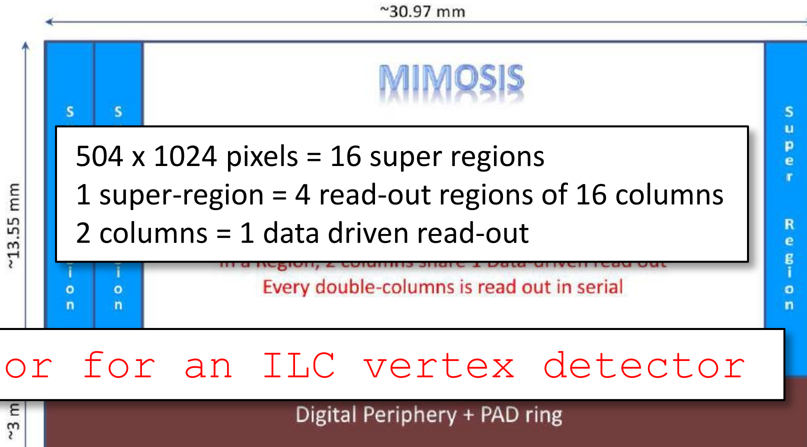


- 4 prototypes:
- MIMOSIS-0: = 2 regions
  - ✓ Back from foundry (2017)
  - ✓ Tests (2018-2019)

- MIMOSIS-1: 1st full size prototype
  - ✓ Back from foundry in Q2 2020
  - ✓ 6 epitaxial variants have been produced to study charge collection
    - Thinning to 50 µm, radiation tests
  - ✓ Functionnal, lab tests are starting
    - ^{55}Fe, β
  - ✓ Test beam foreseen in 2021



- MIMOSIS-2:
  - ✓ Mid-2021
- MIMOSIS-3: final pre-production sensor
  - ✓ >2022

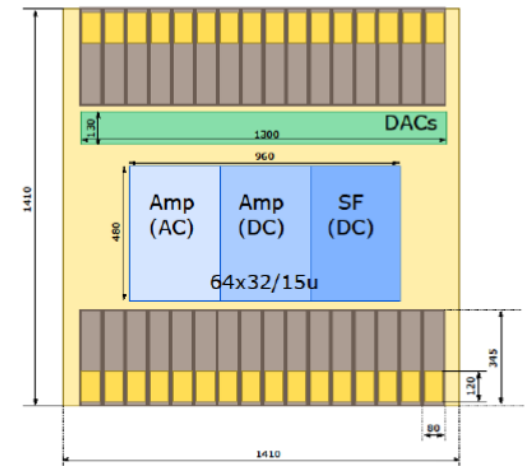


⇨ architecture adaptable to a fast sensor for an ILC vertex detector

TJ-65 nm: Le grand départ

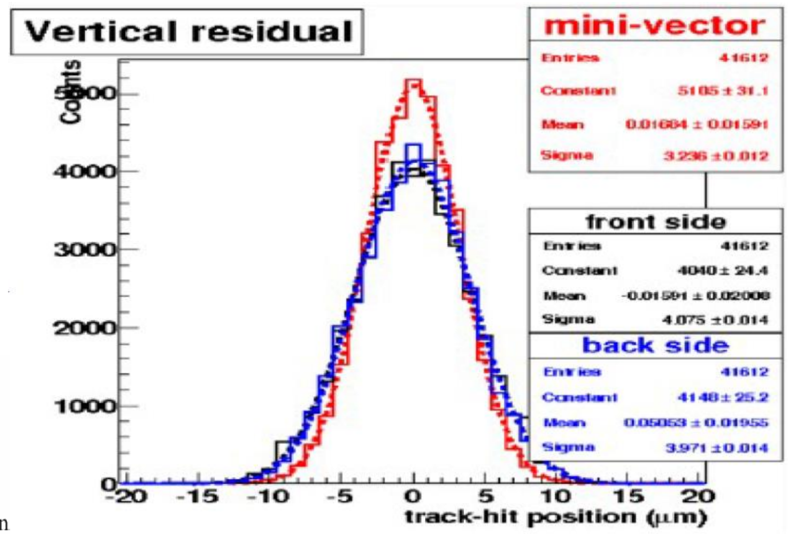
- TJ-65 nm now available
  - ✓ Main driver: CERN EP R&D WP 1 & ALICE upgrades (involves other labs)
  - ✓ Different requirements
    - EP: time resolution and radiation tol.
    - ALICE: granularity and material budget
    - Common R&D during the 1st years.
  - ✓ First submission in ~ autumn Q4 2020 (MLR)

- IPHC-Strasbourg involvement
  - ✓ Test structures, (DACs, etc.)
  - ✓ Technology exploration with single rolling shutter / analog output prototype
    - pitch, diodes, amps, etc.
    - Testable in beam
  - ✓ Caveat: sensitive volume not yet optimised for charged particle detection
  - ✓ Part of Cremlin+ program

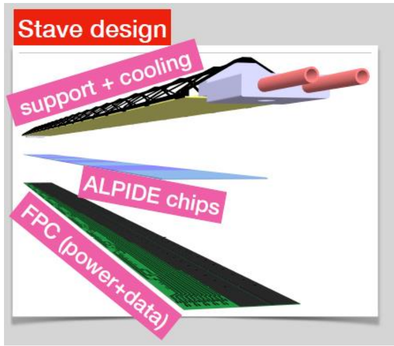


Material budget

- PLUME (Bristol, DESY, IPHC)
  - ✓ Double sided ladders with minimized material budget
  - ✓ 0.35% X_0 reached ⇨ ~0.3 X_0 doable (with air flow cooling)
  - ✓ Combining each side for improved resolution



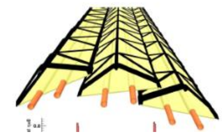
- ALICE ITS-2
  - ✓ Water cooling ⇨ ~0.35% X_0



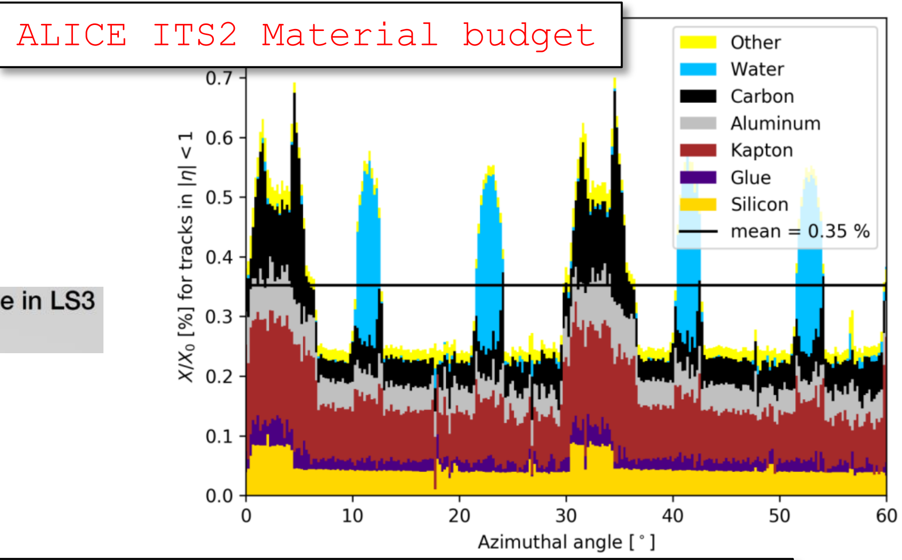
Proposal for an ITS upgrade in LS3

Magnus Mager (CERN)

LHCC 10.09.2019



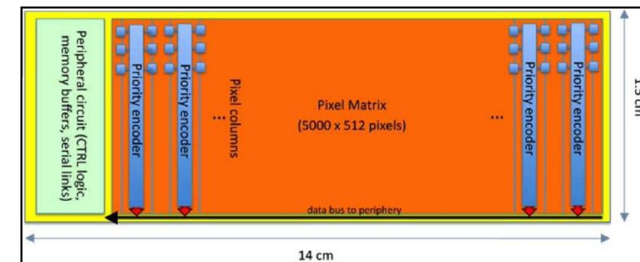
ALICE ITS2 Material budget



⇨ Contribution of sensors to total material budget ~ 20-30%
(Majority from cables + cooling + support)

A possible answer: stitching

- Silicon is flexible
  - ✓ Self supported and bended circuits + detectors !
    - ▪ ALICE: test beam of bended ALPIDE sensors
- Industry provides stitching
  - ✓ Multi-reticle size ladders
    - ▪ ~14 cm in 180 nm, 30 cm in 65 nm
    - ▪ Chip-to-chip interconnection
- Added value:
  - ✓ Very low material budget (~0.05-0.10 % X_0)
    - ▪ Flex cable ? Cooling ? Support ?
  - ✓ Large area detectors
    - ▪ Constant R = No overlaps or acceptance loss
    - ▪ Beam pipe as mechanical support
- ALICE R&D program
  - ✓ ALICE ITS upgrade beyond LS3
    - ▪ Exploit stitching
  - ✓ Proposal beyond LS4
    - ▪ 10 double sided layers
    - ▪ 100 m^2
- Challenge & potential issues
  - ✓ Bias voltage drops
  - ✓ Extended signal distance transport



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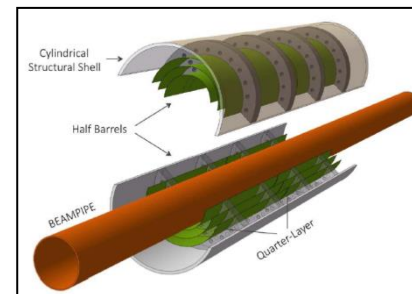
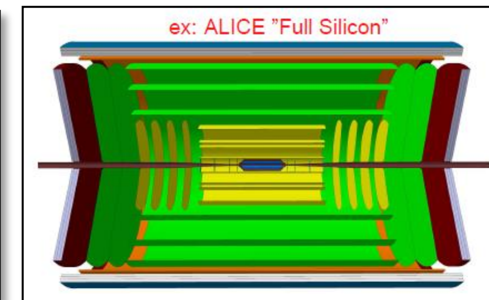
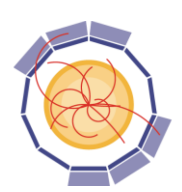
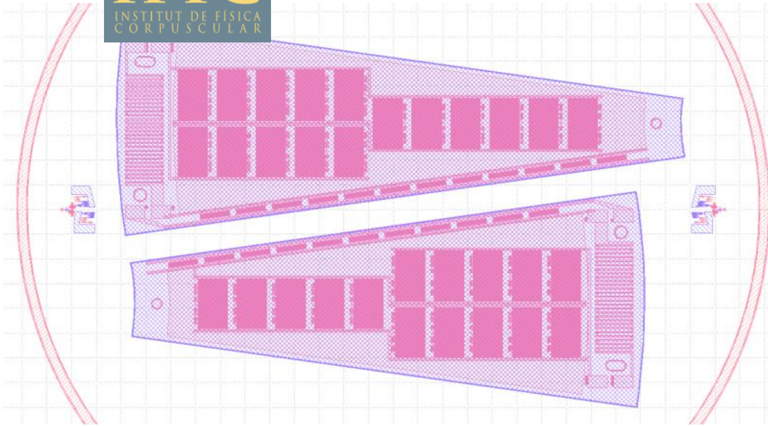
Magnus Mager (CERN)
LHCC 10.09.2019





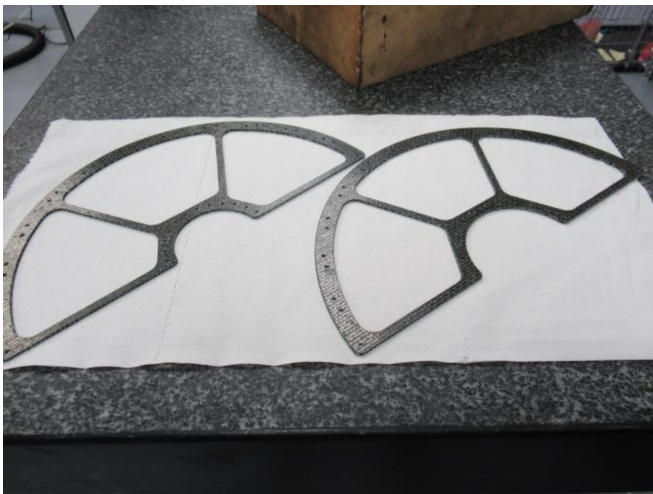


Mechanical samples from IFIC/HLL-MPG

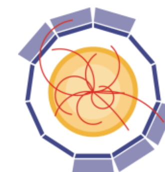


Thin Silicon samples designed by IFIC Valencia and produced at HLL-MPG to be tested in Oxford

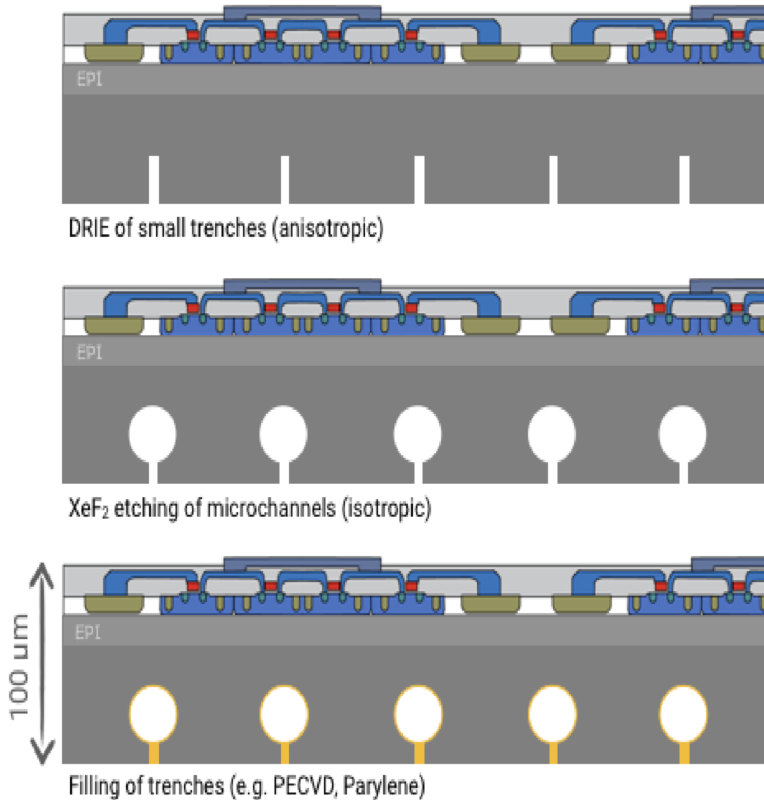
Disk assembly and initial characterization ongoing in Valencia



Ultra-thin CF – honeycomb sandwich produced at INTA (M. Frövel, M. de la Torre)



MCC for CMOS



A pattern of small trenches (3 x 10 µm) is etched on the backside of the pixel detector to a depth of 30 µm

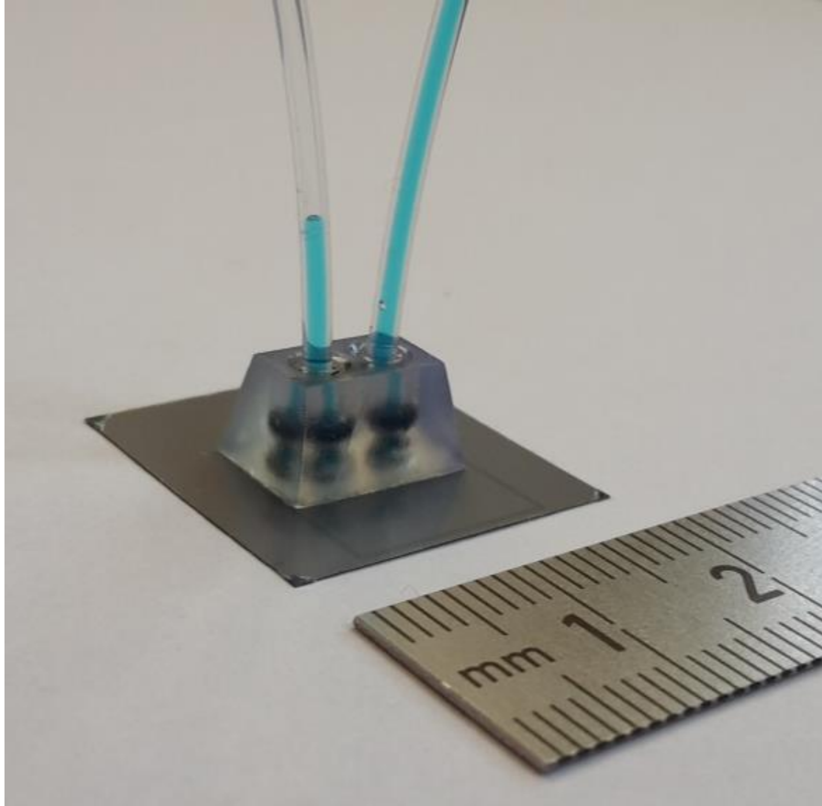
Microchannels are etched isotropically with XeF2
Diameter of the microchannels = 40 µm
Overall depth of the microfluidic circuitry = 50 µm

A thin film of parylene (5 µm) seals the microchannels. It is finally cured by a thermal cycle.

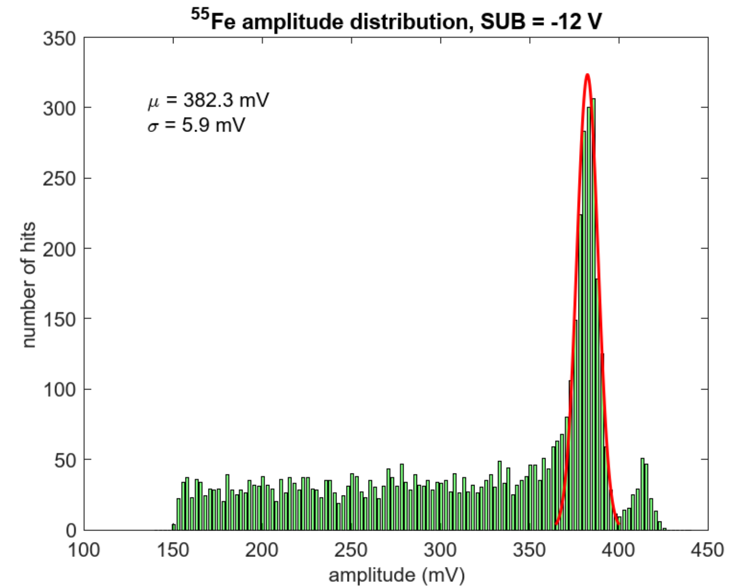
From R. Callegari

M. Boscardin et al., *Silicon buried channels for pixel detector cooling*, Nuclear Instruments and Methods in Physics Research, Section A, 2013
C. Lipp, *Approaches for the fabrication of silicon buried channels for the thermal management of monolithic pixel detectors*, MSc Thesis, EPFL, 2017
I. Berdalovic et al., *Monolithic pixel development in TowerJazz 180 nm CMOS for the outer pixel layers in the ATLAS experiment*, JINST 13 C01023, 2018

MCC for CMOS



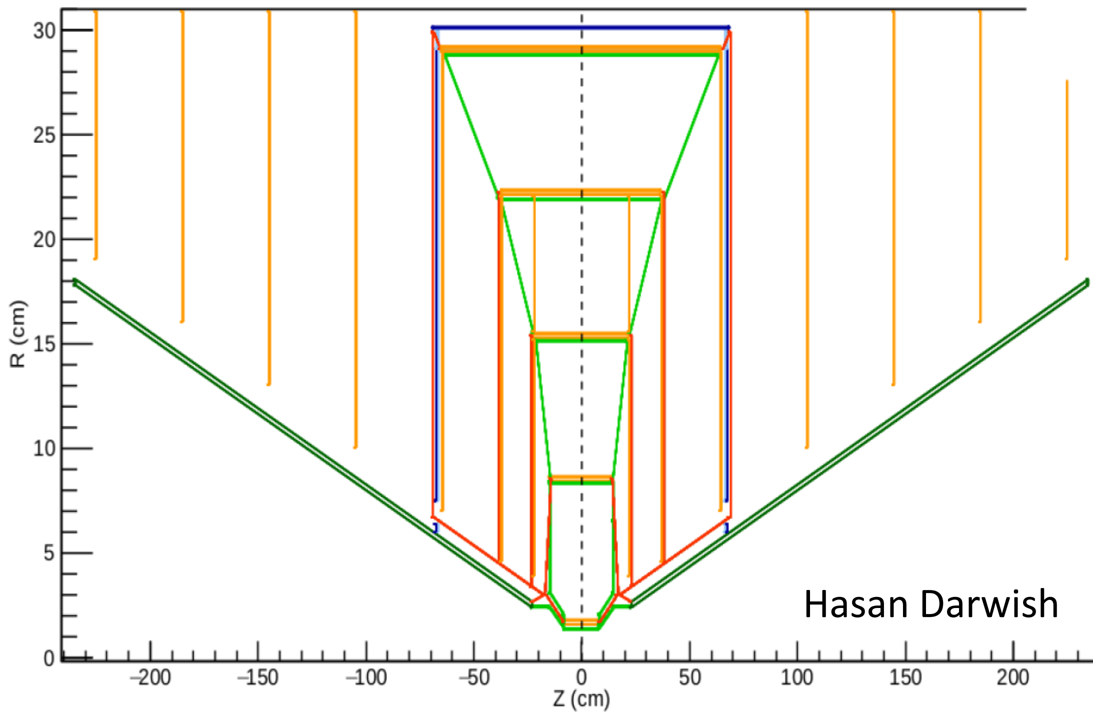
Proof of principle for a new technology that has tremendous potential!!

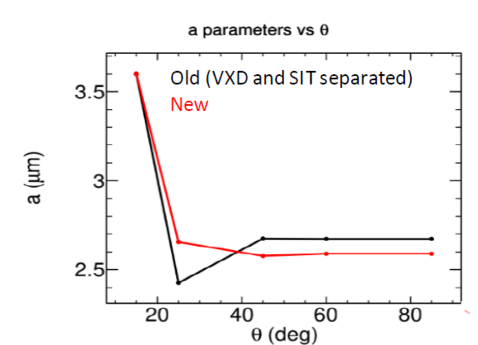


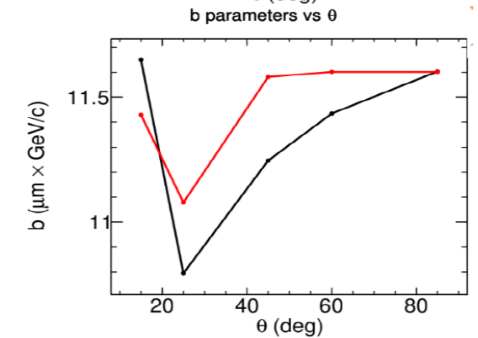
CMOS compatible post-processing at the die level demonstrated in a fully functional 100 mm thick device

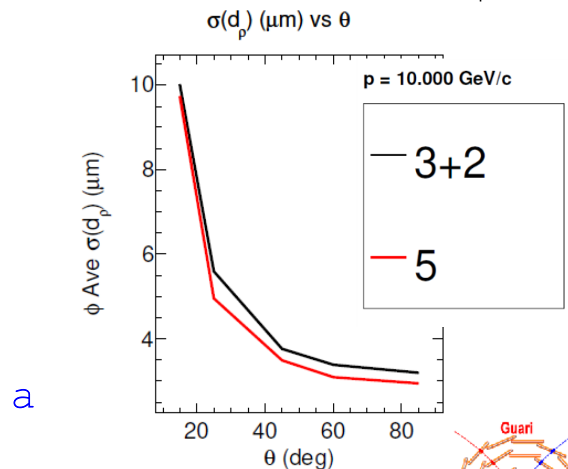
Liquid flows and the chip's electrical performance remains unaltered!

ILD VXd design optimisation: example

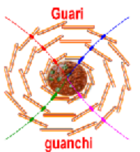








- Merge VXD & SIT into one detector ?
  - ✓ Equidistant radii for the 5 double layers
  - ✓ Faraday cage moved at larger radius ?
- Robustness of current geometry
  - ✓ Performances driven by the beam pipe shape a low polar angle



Summary

- Technologies
  - ✓ Despite R&D slow down, Generic R&D is still dynamic and benefits from other experiments & industry progress
  - ✓ Baseline: CMOS ⇨ 65 nm & stitching
  - ✓ New ideas/breakthroughs are possible in any technology !
    - e.g. : double-tier, wireless data transmission, smart pixels, etc.

- Integration open questions
  - ✓ Power & cooling (air flow, μchannels, etc.)
  - ✓ Control & Data transmission, Cable routing, connectors.
  - ✓ Mechanical support, double sided ladders & low material budget supports, etc.
  - ⇨ Integration issues will be the main challenge in the coming years (as soon as there is a green light !)
  - ⇨ Room for new groups

Backup slides

ILC Power: Results

- Chip read-out speed
  - 2 μs - 4 μs
- Power pulsing
  - Power ON, no beam during 1-2 s
    - ➢ Leading parameter With NO P.P.
  - Power OFF: 10-30 mW/chip
    - ➢ Leading parameter with P.P.
- Outer layers
  - Lower occupancy, larger surface
  - Power is dominated by outer layers
- Beam background rat
  - TDR – TDR × 2

Power Analog $(mW/chip)$	49.22
Power Bias $(mW/chip)$	4.5
Power PriorityEncoder $(mW/chip)$	4.219
Power DigitalPeriphery $(mW/chip)$	64.27
Power PLL $(mW/chip)$	18.5
Power Serializer With Data $(mW/chip)$	86.06
Power Serializer With No Data $(mW/chip)$	0
Power LVDS $(mW/chip)$	56.4

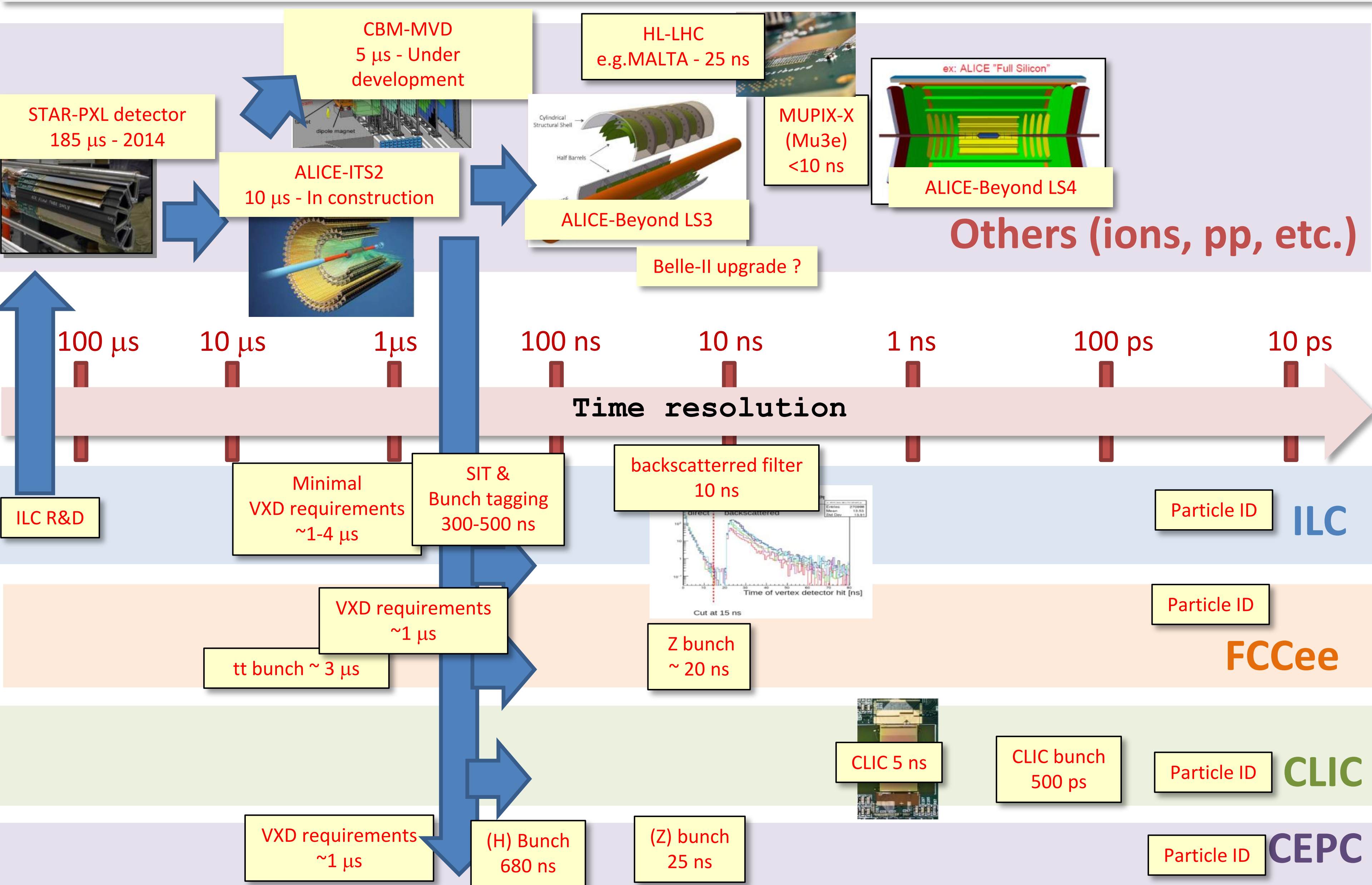
Period	Relative Energy
E during train	225 mJ ~ 4 %
E between train (Power ON)	380 mJ ~ 6 %
E between train (Power OFF)	5740 mJ ~ 90 %

Layers	Relative Power
Layers 0/1	~ 10 %
Layers 2/3	~ 35%
Layers 4/5	~ 55 %

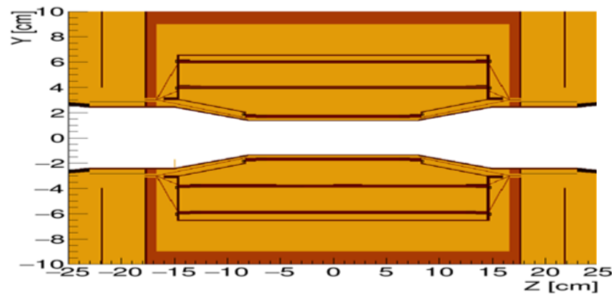
Pitch	Resolution	Power
30 μm	~ 5 μm	1
22 μm	~ 4 μm	×2 (matrix)
18 μm	~ 3 μm	×4 (matrix)

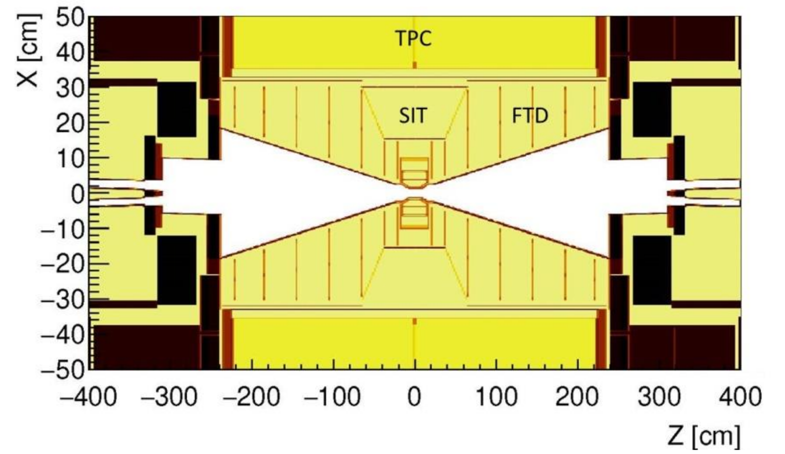
Beam background	Read-out speed	<Power (NO P.P.)	<Power> (P.P.)	
rate	(μs)	(W)	Conservative	Ambitious
TDR	4 μs	102 W	~31 W	~12 W
TDR	2 μs	122 W		
TDR x 2	4 μs	107 W		
TDR x 2	2 μs	127 W		

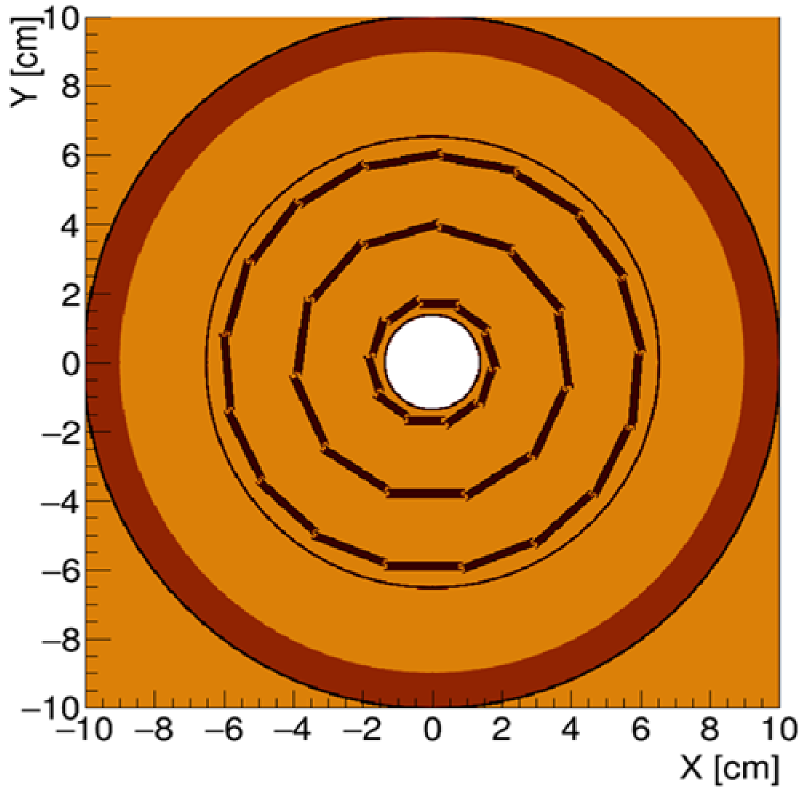
Time resolution in the context of e+e- colliders

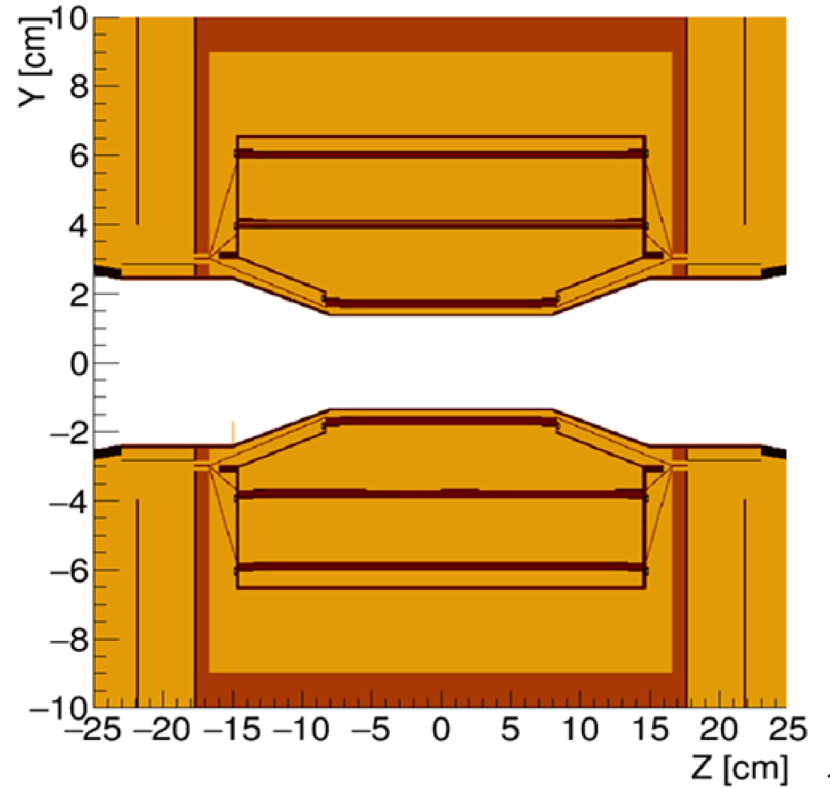


Geometry

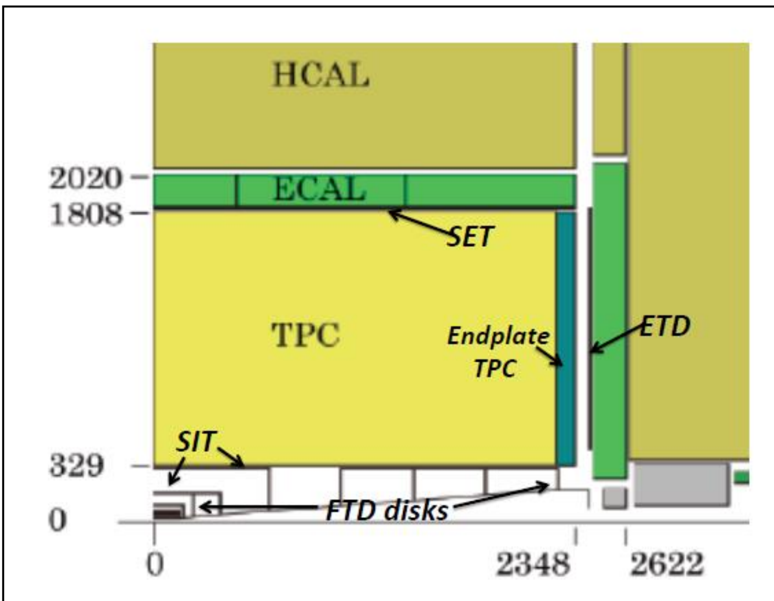








ILD dimensions



Barrel system						
System	R(in)	R(out) /mm	z	comments		
VTX	16	60	125	3 double layers	Silicon pixel sensors,	
				layer 1:	layer 2:	layer 3-6
				$\sigma < 3\mu m$	$\sigma < 6\mu m$	$\sigma < 4\mu m$
Silicon						
- SIT	153	300	644	2 silicon strip layers	$\sigma = 7\mu m$	
- SET	1811		2300	2 silicon strip layers	$\sigma = 7\mu m$	
- TPC	330	1808	2350	MPGD readout	$1 \times 6\text{mm}^2$ pads	$\sigma = 60\mu m$ at zero drift
ECAL	1843	2028	2350	W absorber	SIECAL	30 Silicon sensor layers, 5×5 mm^2 cells
					EcECAL	30 Scintillator layers, 5×45 mm^2 strips
HCAL	2058	3410	2350	Fe absorber	AHCAL	48 Scintillator layers, $3 \times 3\text{cm}^2$ cells
					SDHCAL	48 Gas RPC layers, 1×1 cm^2 cells
Coil	3440	4400	3950	3.5 T field	2λ	
Muon	4450	7755	280	14 scintillator layers		

SIT characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	$\cos\theta$	Resolution R-ϕ[μm]	Time [ns]	RL[%]
153	368	0.910	R: σ=7.0,	307.7 (153.8)	0.65
300	644	0.902	z: σ=50.0	σ=80.0	0.65

SET characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	$\cos\theta$	Resolution R-ϕ[μm]	Time [ns]	RL[%]
1811	2350	0.789	R: σ=7.0,	307.7 (153.8)	0.65

ETD characteristics (current baseline = single-sided Si micro-strips, same as SET ones)				
Geometry			Characteristics	Material
R[mm]	Z[mm]	$\cos\theta$	Resolution R-ϕ[μm]	RL[%]
419.3-1822.7	2420	0.985-0.799	x:σ=7.0	0.65

FTD characteristics (design baseline: pixels for two inner disks, microst				
Geometry			Characteristics	Material
R[mm]	Z[mm]	$\cos\theta$	Resolution R-ϕ[μm]	RL[%]
39-164	220	0.985-0.802	σ=3-6	0.25-0.5
49.6-164	371.3	0.991-0.914		0.25-0.5
70.1-308	644.9	0.994-0.902	σ=7.0	0.65
100.3-309	1046.1	0.994-0.959		0.65
130.4-309	1447.3	0.995-0.998		0.65
160.5-309	1848.5	0.996-0.986		0.65
190.5-309	2250	0.996-0.990		0.65

Costs (VXD & SIT)

VXD

Figures per layers						
Layer	0	1	2	3	4	5
Layer Radius (mm)	16	18	37	39	58	60
Layer $\|z\|max$ (mm)	61.9	61.9	123.8	123.8	123.8	123.8
Chip Pixel Number in X	1440	1440	1440	1440	1440	1440
Chip Pixel Number in Y	512	512	1024	1024	1024	1024
Chip Pixel PitchX (μm)	21.5	21.5	21.5	21.5	21.5	21.5
Chip Pixel PitchY (μm)	21.5	21.5	21.5	21.5	21.5	21.5
Chip Dimension X (mm) (sensitive area)	30.96	30.96	30.96	30.96	30.96	30.96
Chip Dimension Y (mm) (sensitive area)	11.01	11.01	22.02	22.02	22.02	22.02
Chip Dimension Y (mm) (non sensitive area)	2.0	2.0	2.0	2.0	2.0	2.0
Chip Surface (mm^2) (sensitive area)	341	341	682	682	682	682
Chip Surface (mm^2) (non sensitive area)	62	62	62	62	62	62
Chip Surface (mm^2) (total)	403	403	744	744	744	744
Ladder Length (mm) (sensitive area)	123.8	123.8	123.8	123.8	123.8	123.8
Ladder Width (mm) (sensitive area)	11.01	11.01	22.02	22.02	22.02	22.02
N chip per ladder on each side	4	4	4	4	4	4
Layer Surface (cm^2) (sensitive area)	136.3	136.3	599.7	599.7	926.9	926.9
N Chips Per Layer	40	40	88	88	136	136
Total surface (cm^2) (sensitive area)	3484					

Figures per double layers			
	Layer 0/1	Layer 2/3	Layer 4/5
N Chips in z	4	$4+4=8$	$4+4=8$
N Ladders	10	$2\times 11=22$	$2\times 17=34$
N Chips Per double Layer	80	176	272
N Chips (per architecture)	80	448	
N Total Chips	528		

SIT

Figures per layers				
Layer	0	1	2	3
Layer Radius (mm)	153	155	298	300
Layer $\|z\|max$ (mm)	368	368	644	644
Chip Pixel Number in X	1152	1152	1152	1152
Chip Pixel Number in Y	800	800	800	800
Chip Pixel PitchX (μm)	26.6	26.6	26.6	26.6
Chip Pixel PitchY (μm)	27.5	27.5	27.5	27.5
Chip Dimension X (mm) (sensitive area)	30.64	30.64	30.64	30.64
Chip Dimension Y (mm) (sensitive area)	22.0	22.0	22.0	22.0
Chip Dimension Y (mm) (non sensitive area)	2.0	2.0	2.0	2.0
Chip Surface (mm^2) (sensitive area)	674	674	674	674
Chip Surface (mm^2) (non sensitive area)	61	61	61	61
Chip Surface (mm^2) (total)	735	735	735	735
Ladder Length (mm) (sensitive area)	367.7	367.7	643.4	643.4
Ladder Width (mm) (sensitive area)	22	22	22	22
N chip per ladder on each side	12	12	21	21
Layer Surface (cm^2) (sensitive area)	8089	8089	25500	25500
N Chips Per Layer	1200	1200	3780	3780
Total surface (cm^2) (sensitive area)	$\simeq$ 67 000			

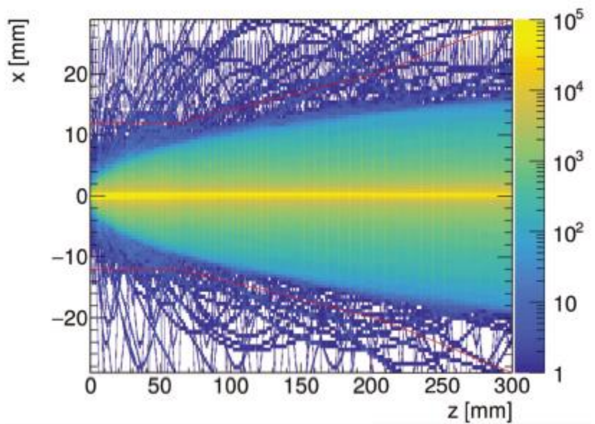
Figures per double layers		
	Layer 0/1	Layer 2/3
N Chips in z	$12+12=24$	$21+21=42$
N Ladders	$\simeq 2\times 50=100$	$\simeq 2\times 90=180$
N Chips Per double Layer	1200	7560
N Total Chips	$\simeq$ 9000	

Table 4: SIT dimensions

Detector	Cost	Sensors	Mechanics	Eletronics	Services	Installation	Total
VXD	Material	1152	452	486	770	100	2960
	Manpower	100	500	400	250	200	1450
	TOTAL (kEUR)	1252	952	886	1020	300	4410
SIT	Material	3820	760	1275	1580	110	7545
	Manpower	200	500	800	300	200	2000
	TOTAL (kEUR)	4020	1260	2075	1880	310	9545

Occupancy and beam background (Guinea Pig)

- RUNNING CONDITIONS DOMINATED BY BEAMSTRAHLUNG $E^{\pm}$:
  - Radiation doses: O(100) kRad, $< 10^{12}$ $n_{eq}/cm^2/yr$
  - Rate of $e^{\pm}_{BS}$ impacts: several tens/cm^2/BX
    - ⇛ governs time resolution requirements
  - sizeable uncertainties: σ_{BS}, luminosity
    - ⇛ substantial safety factors mandatory !



ILD @ 250 GeV

	hits/BX			hits/BX/cm^2		
	mean	±	RMS	mean	±	RMS
VXD 1	914	±	364	6.64	±	2.65
VXD 2	545	±	207	3.96	±	1.51
VXD 3	129	±	60	0.213	±	0.100
VXD 4	107	±	53	0.177	±	0.088
VXD 5	40	±	26	0.043	±	0.029
VXD 6	34	±	24	0.037	±	0.026

Daniel Jeans, Akiya Miyamoto

e^+e^- Pairs

Beamstrahlung

Pitch ~ 17-25 µm
Cluster multiplicity ×5
Safety factor ×3-5
Time resolution ~few µs
⇨ ~Per mil level occupancy
⇨ Bunch separation ?

VXD-ILD: Data flux

Layer	DBD occupancy (hits/cm^2/BX)	Detector surface (mm^2)	#hits/BX	#hits/read out	#hits/train	# hits/s	Data rate (Mbits/train)	Data rate (Mbits/s)	Data rate (Mbits/train) With safety factor of 3	Data rate (Mbits/s) With safety factor of 3
	@ √s = 500 GeV	Length x width x # ladders		assuming 4 μs i.e. 8 BX	Assuming 1312 bunches per train	Assuming 5 trains / s	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit
0	6.32 ± 1.76	125 x 11 x 10 = 13 750	870	7000	1140 K	5700 K	114	570	342	1710
1	4.00 ± 1.18	125 x 11 x 10 = 13 750	550	4400	720 K	3600 K	72	360	216	1080
2	0.25 ± 0.11	125 x 2 x 22 x 11 =60 500	150	1200	197 K	985 K	19.7	98.5	59.1	295.5
3	0.21 ± 0.09	125 x 2 x 22 x 11 =60 500	130	1040	171 K	855 K	17.1	85.5	51.3	256.5
4	0.04 ± 0.03	125 x 2 x 22 x 17 =93 500	40	320	52 K	260 K	5.2	26	15.6	78
5	0.04 ± 0.03	125 x 2 x 22 x 17 =93 500	40	320	52 K	260 K	5.2	26	15.6	78
TOTAL		335 500 mm^2 (~0.35 m^2)	1780	14280	2332 K	11660 K	233.2	1166	700	3500

- average raw data size (without or with safety factor on beam background included)

Average size per BX : ~0.18 Mbits / BX ⇨ 0.54 Mbits / BX (with safety factor of 3) ~375 Gbits/s (instantaneous)

Average size per event (~8 BX) : ~1.4 Mbits/ readout ⇨ 4.3 Mbits / readout (with safety factor of 3)

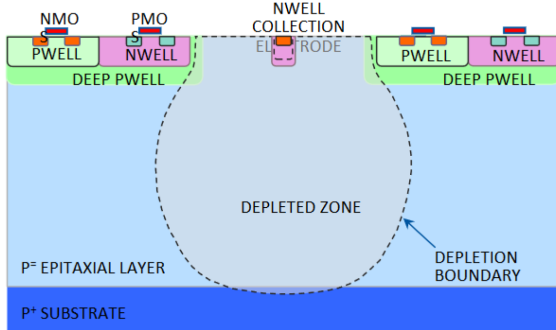
Average size per train : ~233 Mbits / train ⇨ 700 Mbits / train (with safety factor of 3)

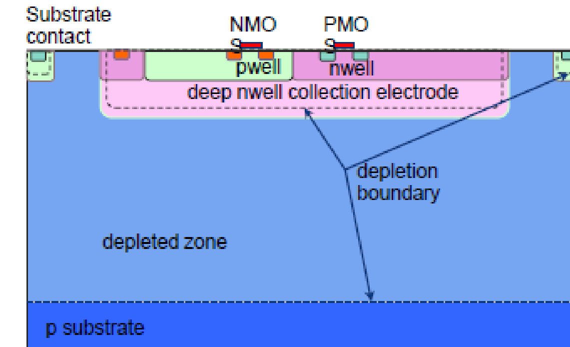
Average size per second : ~1166Mbits / s ⇨ 3500 Mbits / s (with safety factor of 3)

CPS: Large vs small nwell collection electrode

Small electrode ⟵⟶ Large electrode

Standard : no full depletion

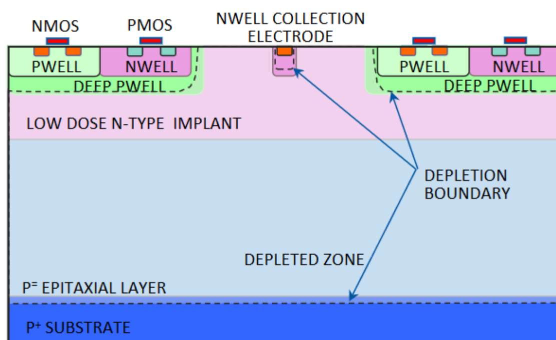




- ❑ Partial depletion
  - ✓ Charge sharing ⇨resolution

- ❑ Full depletion
  - ✓ No Charge sharing ⇨ S/N
  - ✓ Charge collection time ⇨ very fast timing
  - ✓ Radiation hardness (not an issue in e^+e^- colliders)

Modified : full depletion, faster charge collection



- ❑ Capacitance
  - ✓ Analog power ~ $(C/Q)^2$

⇨ Design should favor spatial resolution and power consumption w.r.t. radiation hardness and charge collection time*

⇨ Small electrodes more adapted for e^+e^- colliders

*Exception: CLIC

ALICE ITS Material budget