R&D Projects of LCTPC

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for LCTPC

ILD phone meeting
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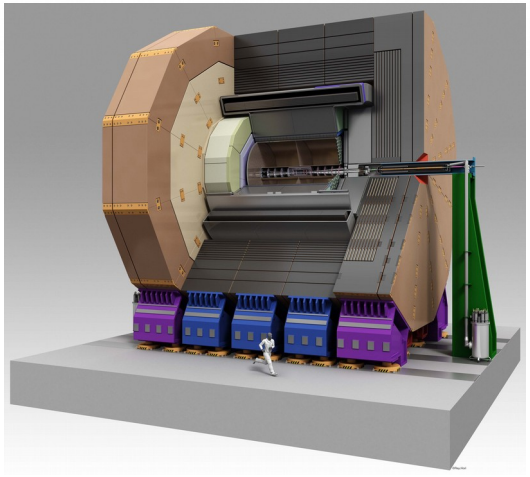
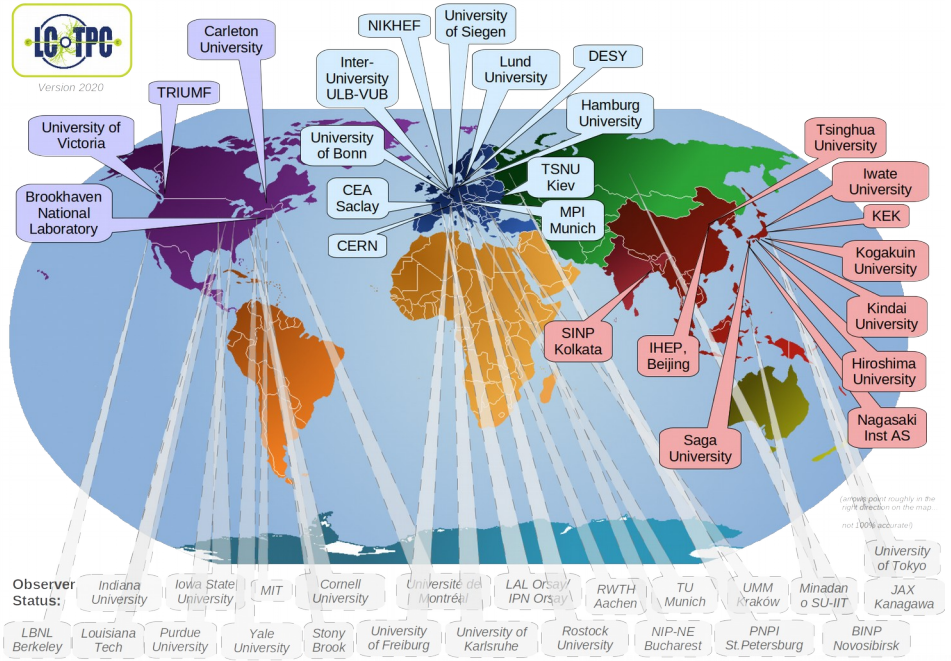
UNIVERSITÄT BONN

A TPC for ILD



International Large Detector
- TPC as main tracker

LCTPC studies a MPGD-based TPC



TPC Requirements :

Parameter			
Geometrical parameters	r_{in}	r_{out}	z
	329 mm	1808 mm	$\pm$ 2350 mm
Solid angle coverage	up to $\cos\theta \simeq 0.98$ (10 pad rows)		
TPC material budget	$\simeq 0.05\ X_0$ including outer fieldcage in r		
	$< 0.25\ X_0$ for readout endcaps in z		
Number of pads/timebuckets	$\simeq$ 1-2 $\times 10^6$/1000 per endcap		
Pad pitch/ no.padrows	$\simeq 1\times$ 6 mm^2 for 220 padrows		
σ_{point} in $r\phi$	$\simeq$ 60 μm for zero drift, $<$ 100 μm overall		
σ_{point} in rz	$\simeq 0.4 - 1.4$ mm (for zero – full drift)		
2-hit resolution in $r\phi$	$\simeq$ 2 mm		
2-hit resolution in rz	$\simeq$ 6 mm		
dE/dx resolution	$\simeq$ 5 %		
Momentum resolution at B=3.5 T	$\delta(1/p_t) \simeq 10^{-4}$/GeV/c (TPC only)		

MPGDs in TPCs

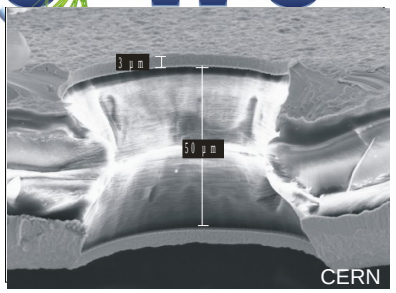
- Ion backflow is reduced significantly
- Small pitch of gas amplification regions
  => strong reduction of E×B-effects
- No preference in direction
  => all 2 dim. readout geometries possible

Three Baseline Technologies

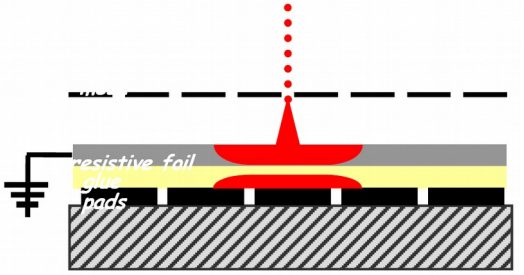
GEMs: copper-insulator- copper sandwich, with holes

2 configurations are being tested:

- triple GEMs with ‘standard CERN GEMs’
- double GEMs with 100µm LCP insulator



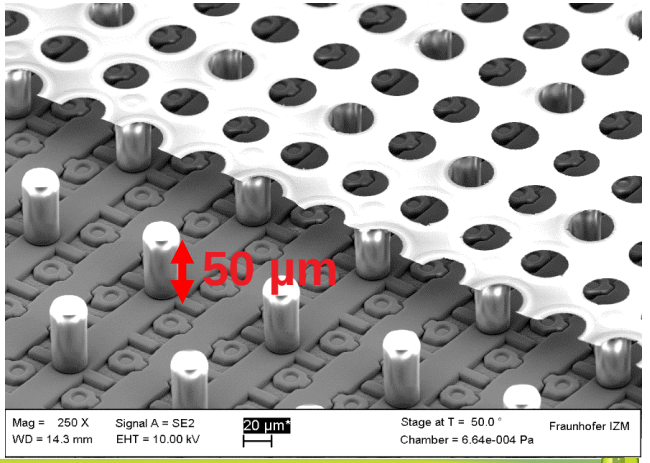
Resistive Micromegas: Bulk-Micromegas with 128 µm gap size between mesh and resistive layer



NIM A581(2007) 254

GridPix: Micromegas with 1 µm Al-grid over Pixel readout ASIC

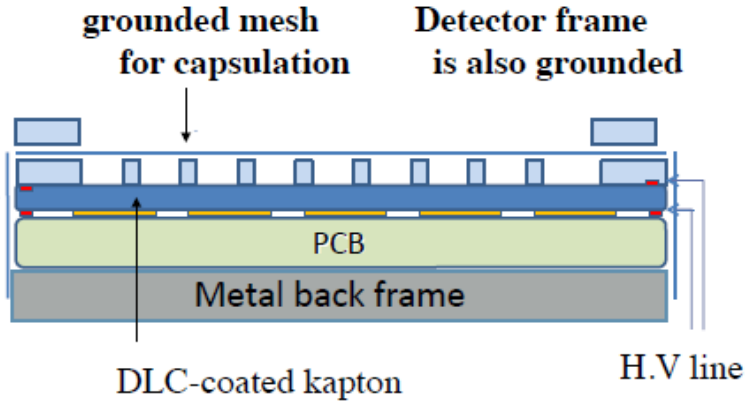
- 55µm pitch of readout pixels
- resistive layer needed for protection of ASIC



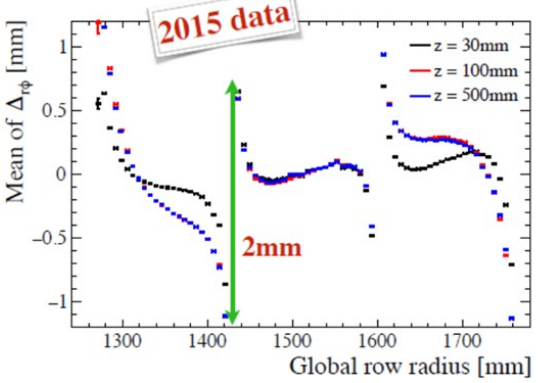
Optimization of Modules

Recent progress on many details. Here, only 2 examples should be given:

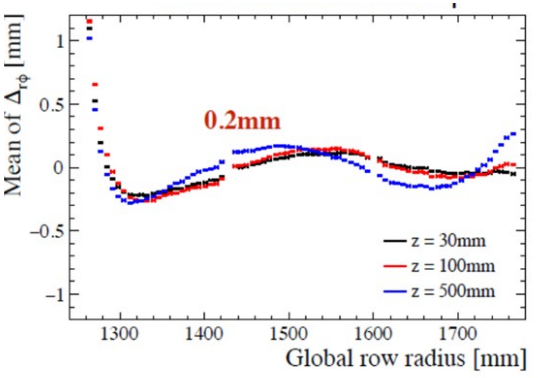
1.) Micromegas: New HV scheme of the module places grid on ground potential and reduces field distortions significantly



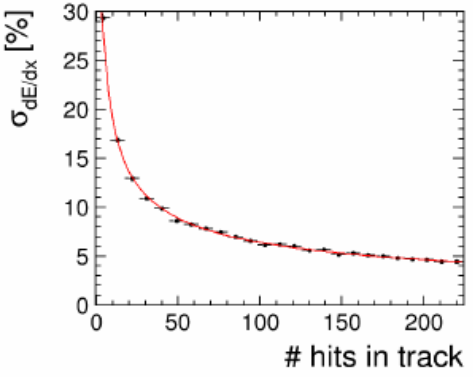
Old scheme

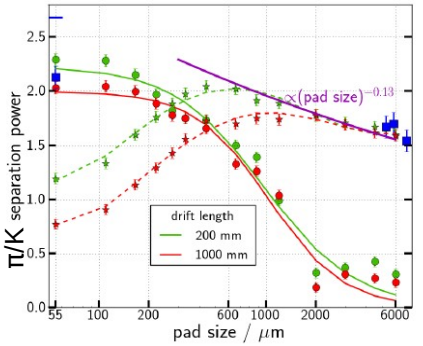


New scheme



2.) GEM modules: dE/dx performance is scrutinized. Also, in dependence on the pad sizes.





Detector Modules

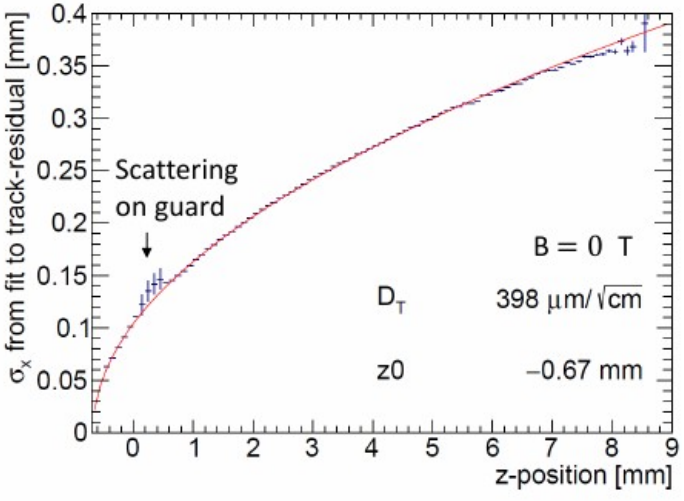
GEM and Micromegas groups have finished analysis of test beam data with previous set of detector modules. Both groups want to implement improvements in a new generation of modules. They are discussing new common modules with
- a more final design and
- a more comparable design.

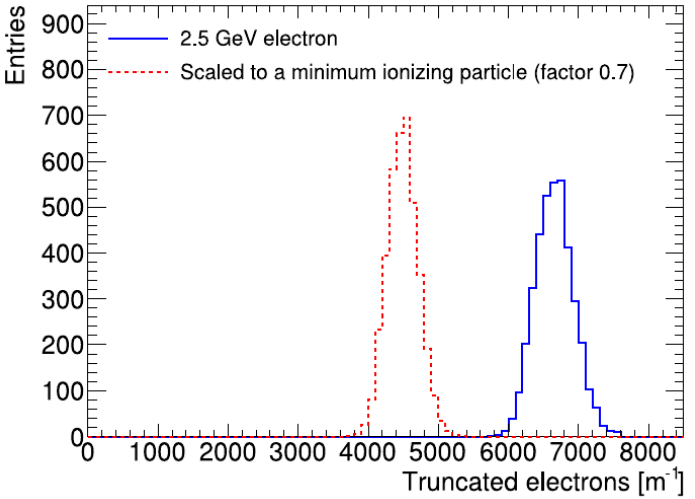
These common modules should have a
- common readout electronics (sALTRO),
- an identical gating device (gating GEM) and
- possibly a common pad plane

→ Only the gas amplification stage differs => better comparison of performance for a technology decision.

GridPix Detectors

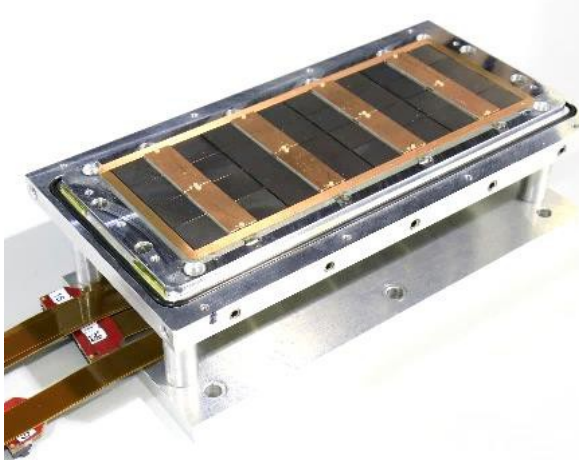
GridPix detector have moved from Timepix to Timepix3 ASICs. Tests with single and quad devices have been successful done and published.





A first module with 32 GridPixes has been constructed and will be tested in a planned test beam at DESY - including a test in a magnetic field. A complete LCTPC module would consist of about 100 GridPixes.

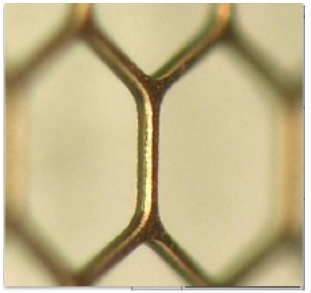
The ion back flow of the module has been measured and can be further reduced by applying a double grid. Also the resistivity of the protection layer will have to be reduced.

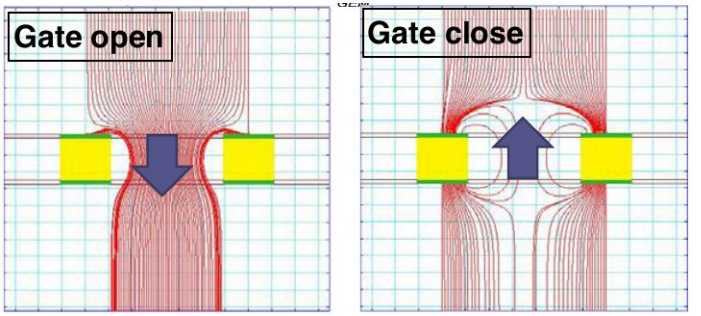


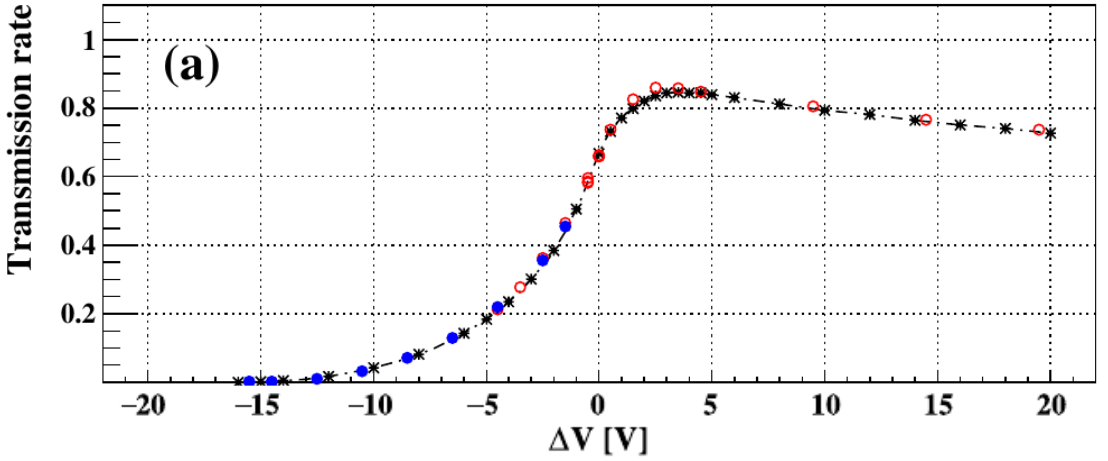
Gating GEM

To avoid track distortions because of charge in drifting volume, gating is needed. As a gating device the gating GEM is a favorite, which has large holes (Ø 300 µm) and thin strips inbetween (30 µm).

The electron transparency has been determined with different measurements and corresponds to 82 % as expected from simulations.





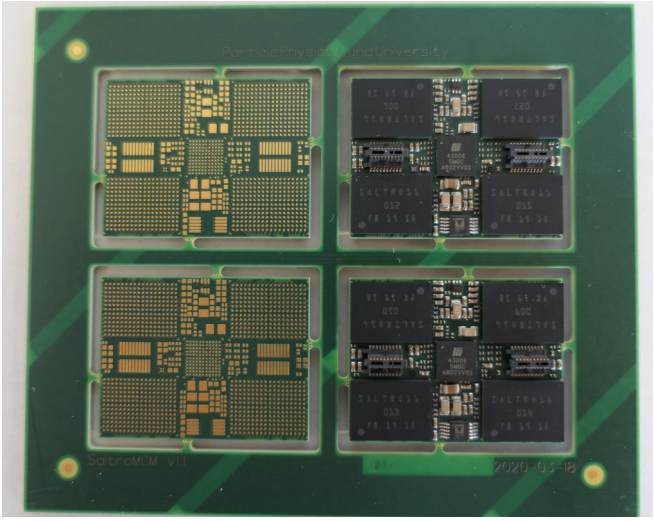


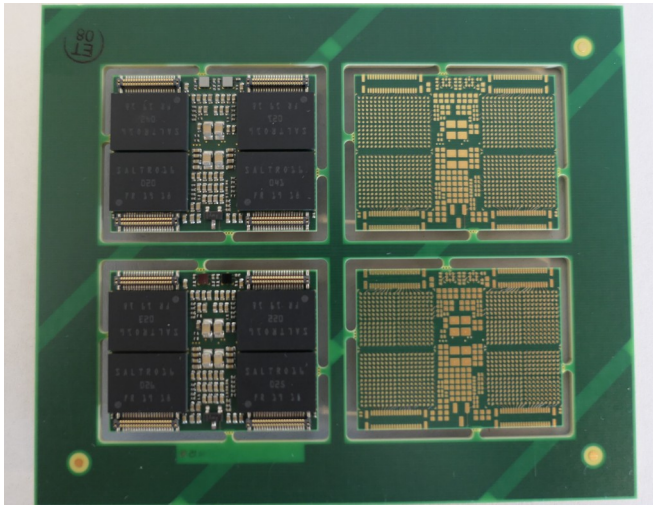
The ion blocking power still has to be determined and quantified.
First measurements have been initiated for this, but no results yet.
Also a fast HV switching circuit has to be developed.
The gate should also be tested in B = 3.5-4 T.

Electronics

A new electronics for R&D purposes is being developed.
It is based on the sALTRO ASICs.

- All ASICs are packaged and are being tested now.
- Additional boards have been designed and first (test) boards have been assembled. Tests show a full functionality
- The final layout is being designed.
- Still looking for an FPGA programmer to finalize the firmware.



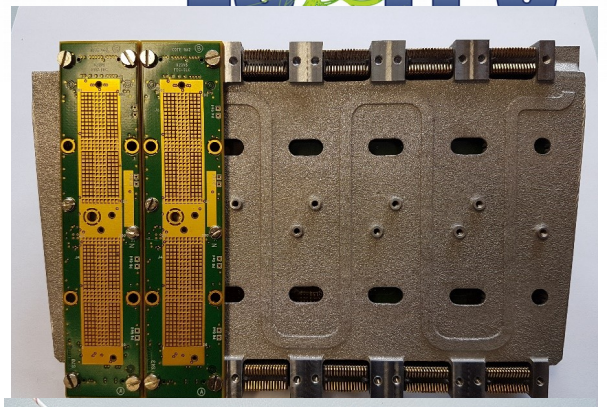


Top and bottom of a panel with 4 MCM-boards out of which 2 MCM-boards are fully mounted.

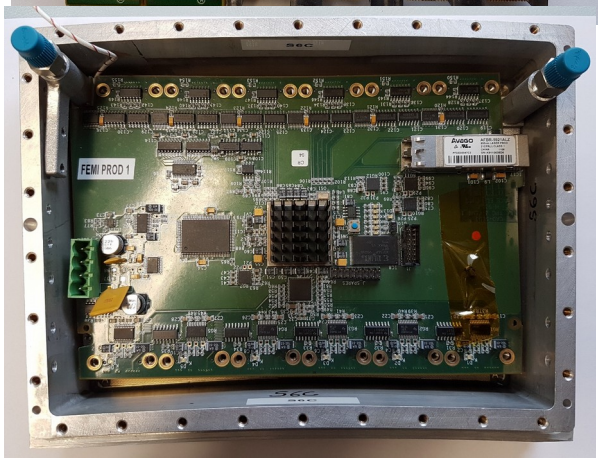
Determine design parameters for final ASIC.

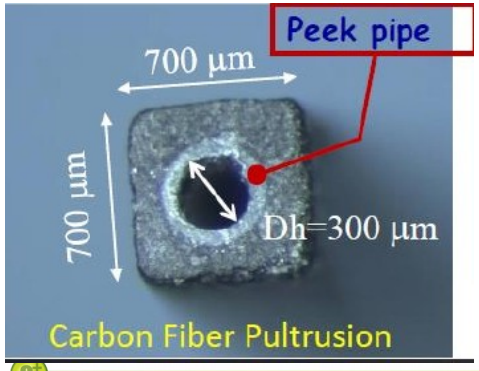
Cooling

Despite the power pulsing, the readout electronics will require a cooling system. 2-phase CO2-cooling is a very interesting candidate. A fully integrated AFTER-based solution has been tested on 7 Micromegas modules during a test beam.

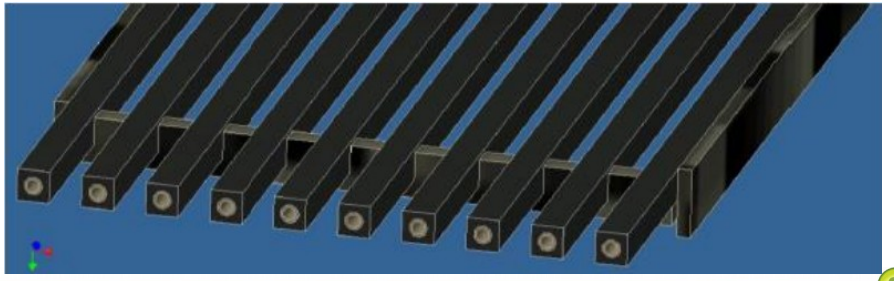


To optimize the cooling performance and the material budget, 3D-printing is an attractive possibility for producing the complex structures required. A prototype for a full module is available now at CEA, Saclay. It will be increased to 4 modules until 2021.



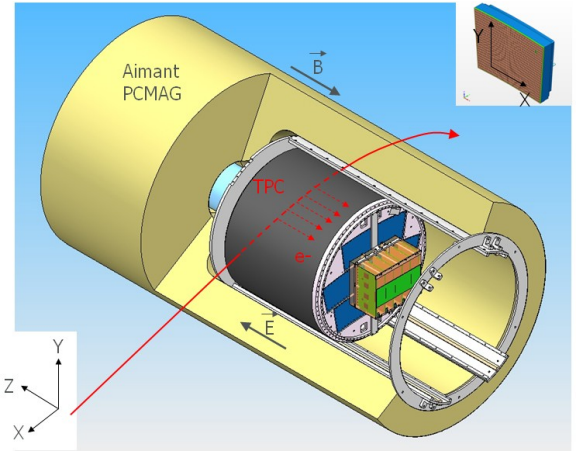


Alternatively, Lund is exploring micro channel cooling together with Pisa. These consists of pipes with Ø 300 µm in carbon fiber tubes.



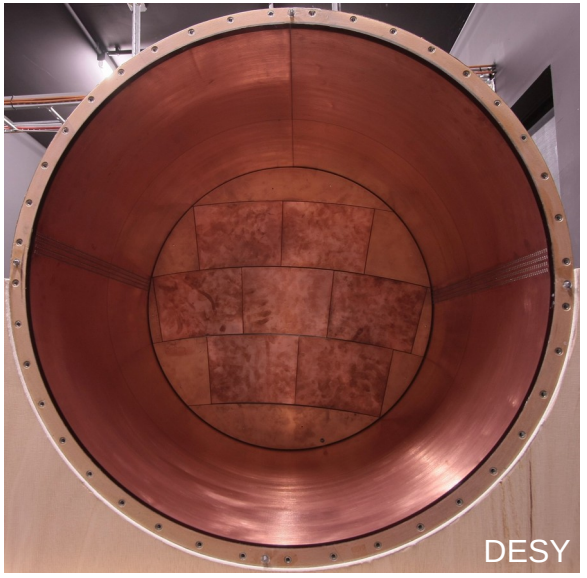
Test setup at DESY

PCMAG: B < 1.2 T, bore diameter: 85 cm
Electron test beam: E = 1- 6 GeV
LP support structure
Beam and cosmic trigger



<u>LP Field Cage Parameter:</u>
length = 61 cm
inner diameter = 72 cm
up to 25 kV at the cathode
=> drift field: E ≈ 350 V/cm
made of composite materials: 1.24 % X_0

<u>Modular End Plate</u>
two end plates for the LP made from Al
7 module windows (one is space frame)
→ size ≈ 22 × 17 cm^2 (ILD: 240 modules/endcap)



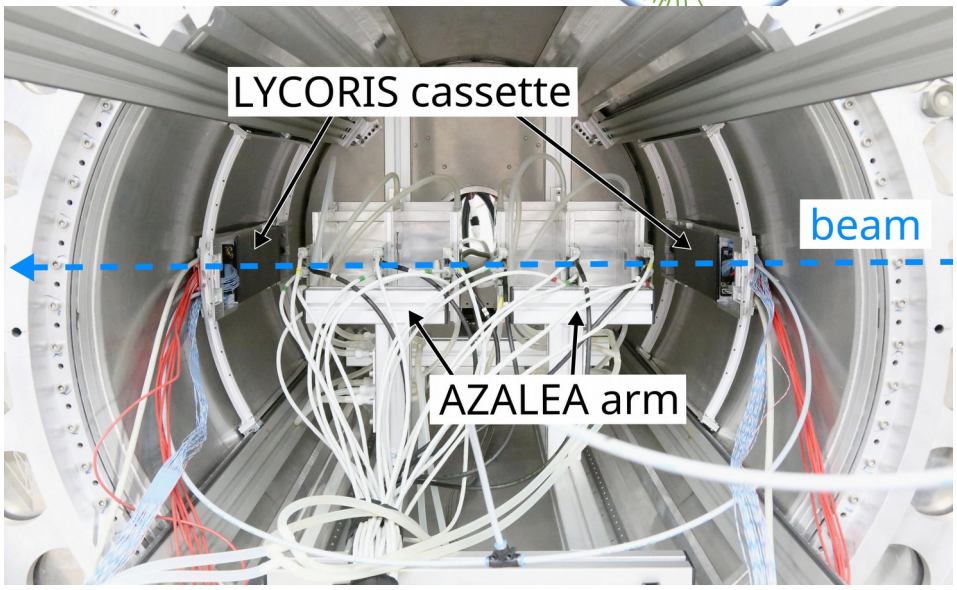
Large Prototype has been built to compare different detector readouts under identical conditions and to address integration issues.

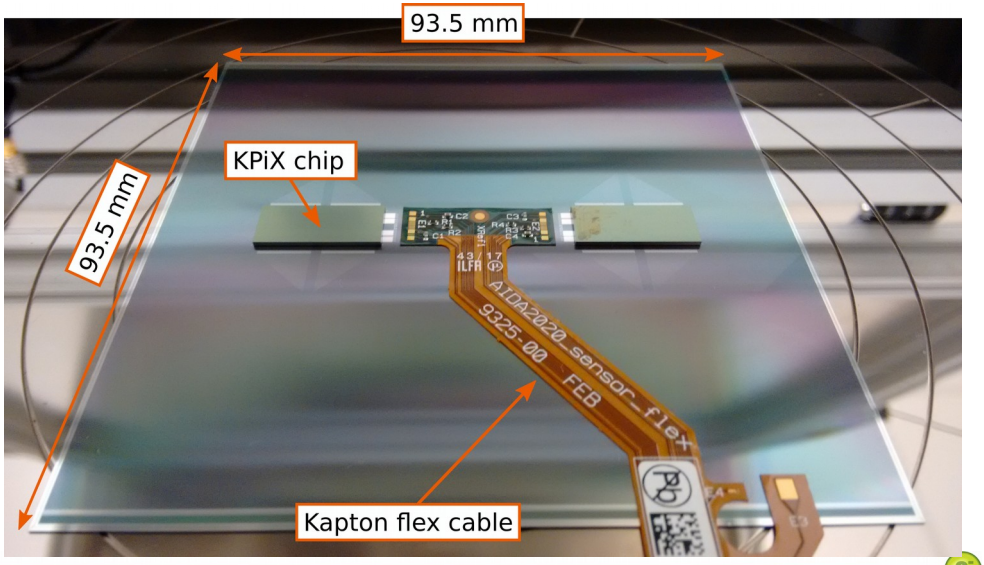
Setup at DESY

Further improvements of the test beam setup at DESY are in progress or planned:

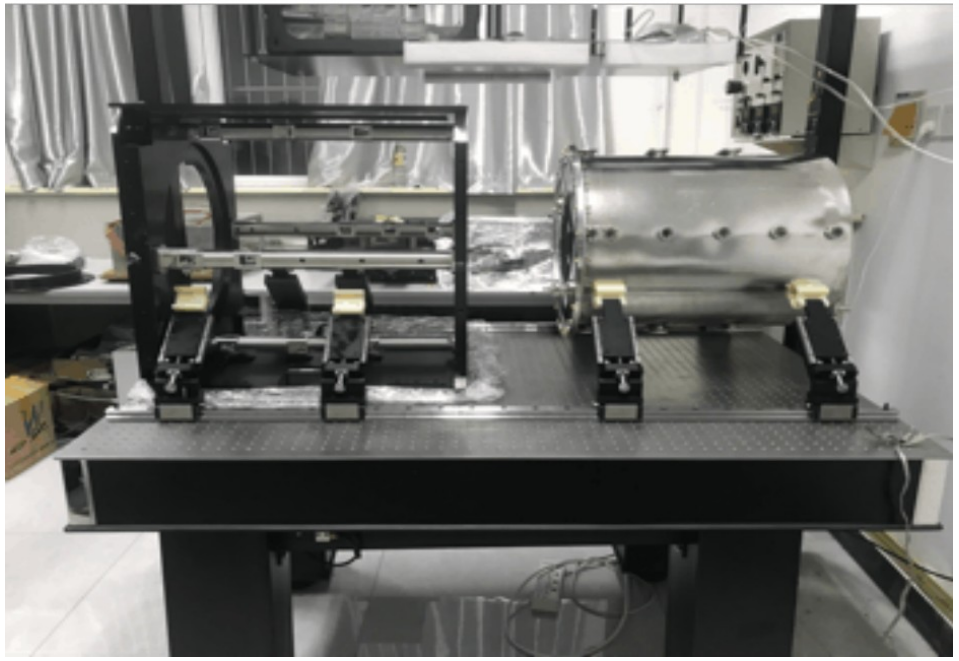
- An external silicon tracker for the Large Prototype (LP) is advanced and first test beams have been performed. But there is still work to integrate everything.
  All groups will redo measurements with newest module types to study distortions

- Current field cage shows misalignments of the axis to the endcaps.
  → Construction of an improved field cage for the LP.
  → Also important for learning to build the final detector.

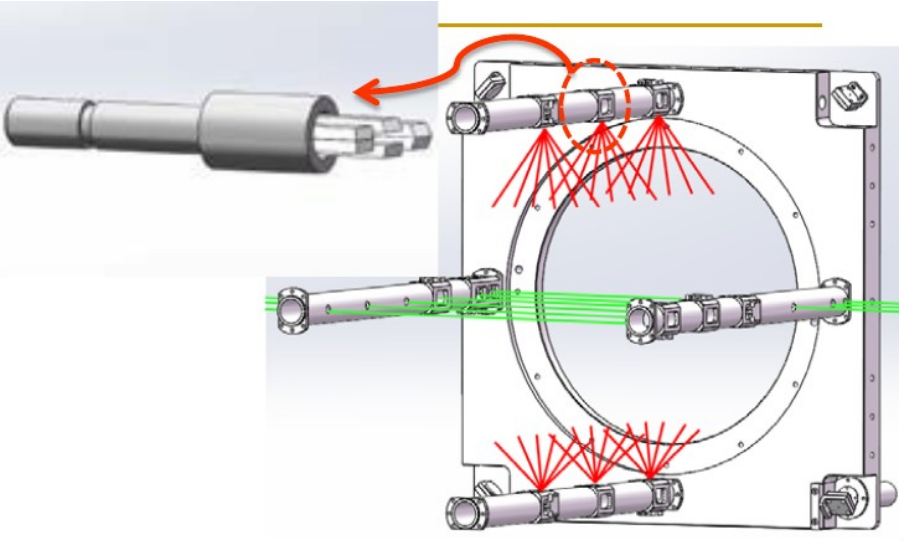


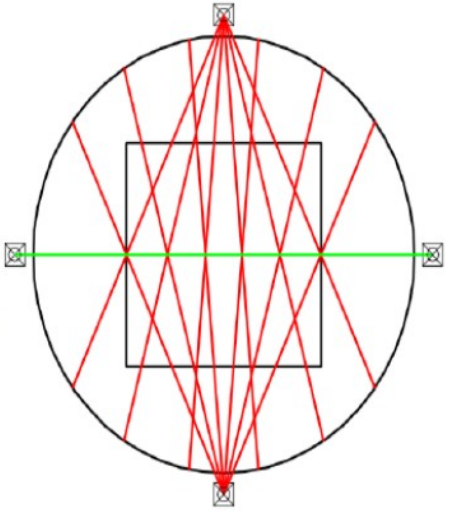


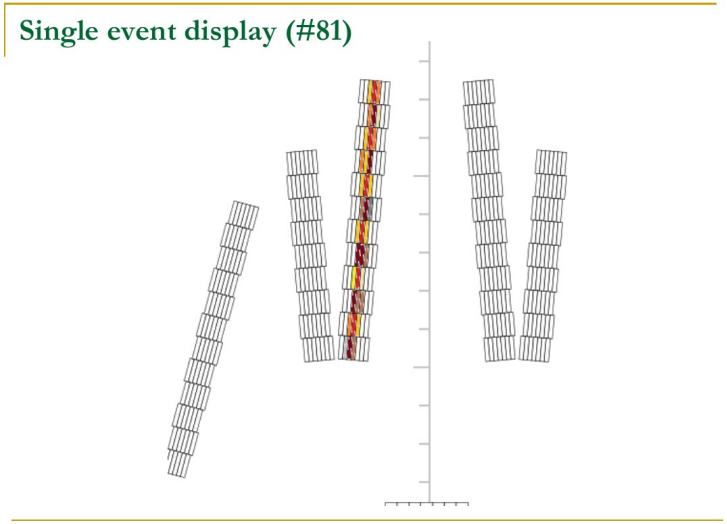
Test Setup with Laser Tracks



- Setup in IHEP, Beijing
- Smaller prototype with 50cm drift length
- Tracks at 42 positions can be generated by 266nm UV laser
- Only 1280 readout channels
  → pads are aligned to laser tracks
- Ionization studied using laser beam of 0.85mm^2 in T2K, P10 and Ar/CO2(90/10)







Open Issues

There is still a long list of open issues, which is very difficult to address, because a lot of manpower is missing.
Most of the issues are connected to simulating the TPC in detail:

Simulation

(a1) Implementation of the response of the resistive anode in our simulation, and, test of one module with a resistive anode in the ILC events with beam backgrounds conditions.

(a2) Test of our current dE/dX code for the LP events, and provide it to the physics simulation.

(a3) Study of the pad size/length in the two hit separation, the occupancy, and the spatial resolutions (in the comparison to the current condition used in the physics analysis)

(b1) Studies of the dependencies of TPC and ILD tracker performances on TPC size and configurations in cooperation with the optimization group.

(b2) Pinpoint performance requirements based on various physics analysis for the technology choice, i.e. looking at different physics channels and charting distributions and requirements (single point, double track resolution, momentum and dE/dx resolution, reliability in performance), which allow the CB later to define the technology choice. Also, suggestions for the test procedure need to be studied.

(b3) Physics simulation to study the benefit of a TPC (vs. Si detectors): dE/dx, continuous tracking, non-pointing tracks. Find appropriate channels and show what a TPC can do better.
→ mostly done by ILD optimization group, but need input and some work from LCTPC

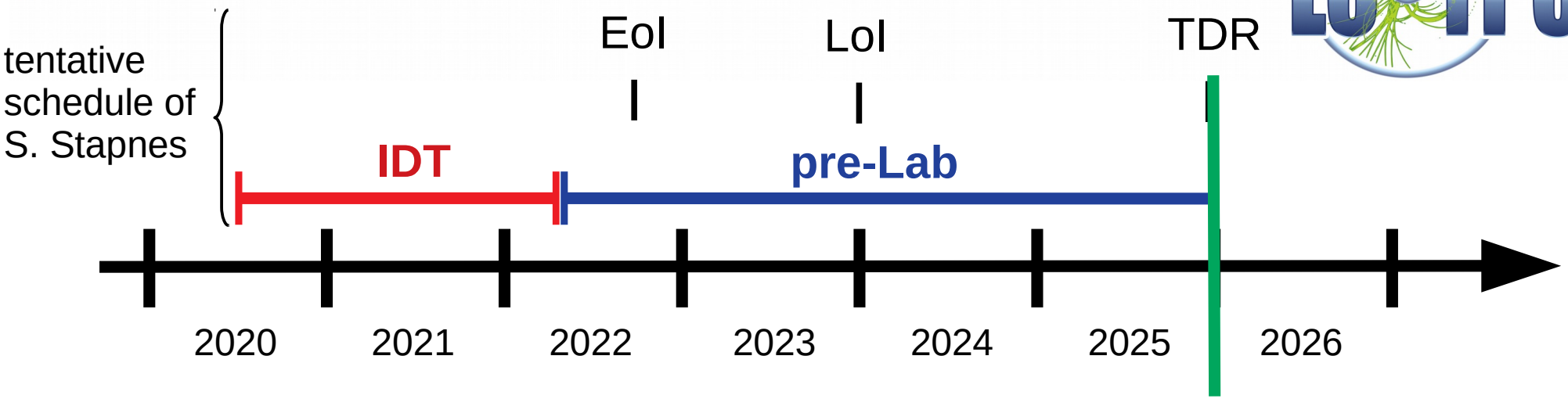
(c1) Study of benefit of pad/pixel readout: This may be partially included in the (b2). For the pixel readout optimized reconstruction algorithms are needed.

(c2) Simulation of physics events to understand requirements on two track/hits separation: This may be studied partially in (a3) for the pad readout.

Software – partially covered and large overlap with simulation tasks

- Further development of MarlinTPC and better understanding of the data already taken.
- Develop correction procedure for local field distortions → give 'final' result for single point resolution in PCMAG and 3.5 T.
- Develop simulation and reconstruction tools for 2 hit/2track reconstruction.

Timeline



Test in B = 4 T

Ion blocking

Development of new readout electronics

Efficient and precise construction of large number of GridPixes

Treatment of large amount of data from GridPixes

Calibration and alignment methods

Simulations

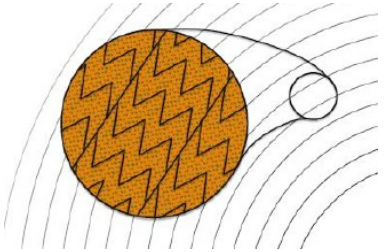
Looking beyond our nose….

We need still a lot of support for finishing the research program!
But in case of a green light soon and a larger number groups joining LCTPC, there are more ideas, which could be looked at. Some examples were presented at the Workshop: ‘New horizons in time projection chambers’ (https://indico.cern.ch/event/889369/) and are listed here:

1.) new ideas of ion backflow reduction (e.g. COBRA, ...)

2.) new ideas of reducing discharge probabilities
– e.g. double resistive MPGDs

3.) Modules with 2 GEMs and MM



4.) chevron type pads as suggested for sPhenix

5.) Do we gain anything with an (additional) optical readout?

Summary

- Continue GEM, Micromegas and pixel tests at the LP in preparation for the preliminary design of the LCTPC after the green light.

- A gate should be included in the next-generation GEM, Micromegas and pixel modules.

- Synergies with T2K / ALICE / CEPC allow us to continue R&D and of course we learn from their experiences and R&D.

- Continue electronics, cooling and powerpulsing development.

- Many simulations are still necessary to understand the detailed requirements of the final detector (e.g. number of ADC bits, pad sizes, etc.)