# Test Beam preparation:

# Synchronisation between systems

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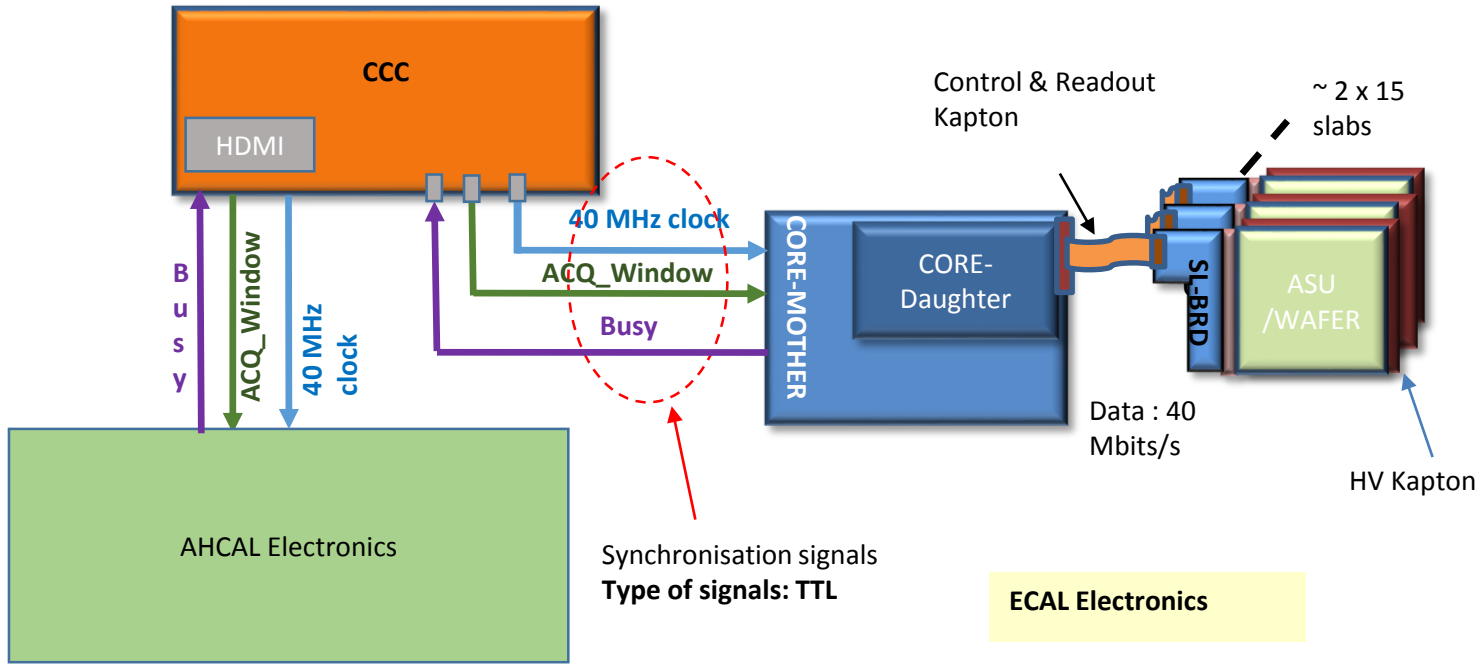
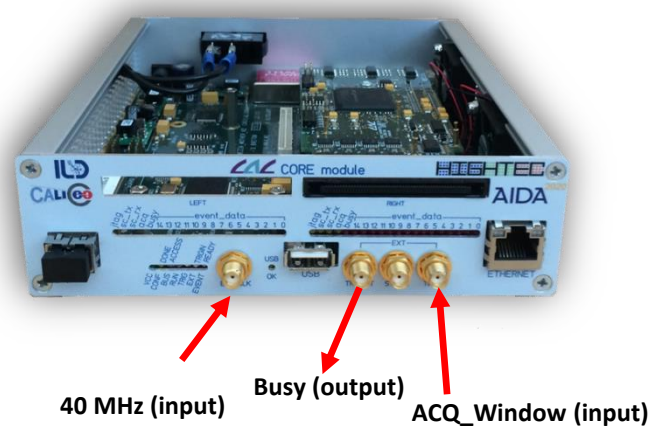
# Synchronising with AHCAL



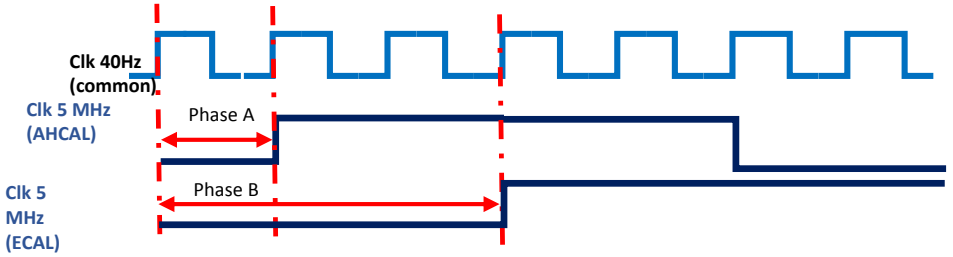




➢ Last year we prepared synchronisation with AHCAL for our next testbeam (March 2020 → may 2021 → October 2021 ??)

- Common 40 MHz **Clock** and **AcqWindow** source.
- **Busy signal** (*corresponding to End of readout of All Skirocs AND buffers empty in SL-Board*) sent from CORE-Module to CCC
- FPGA timestamp is Reset with **first Start Acq**.

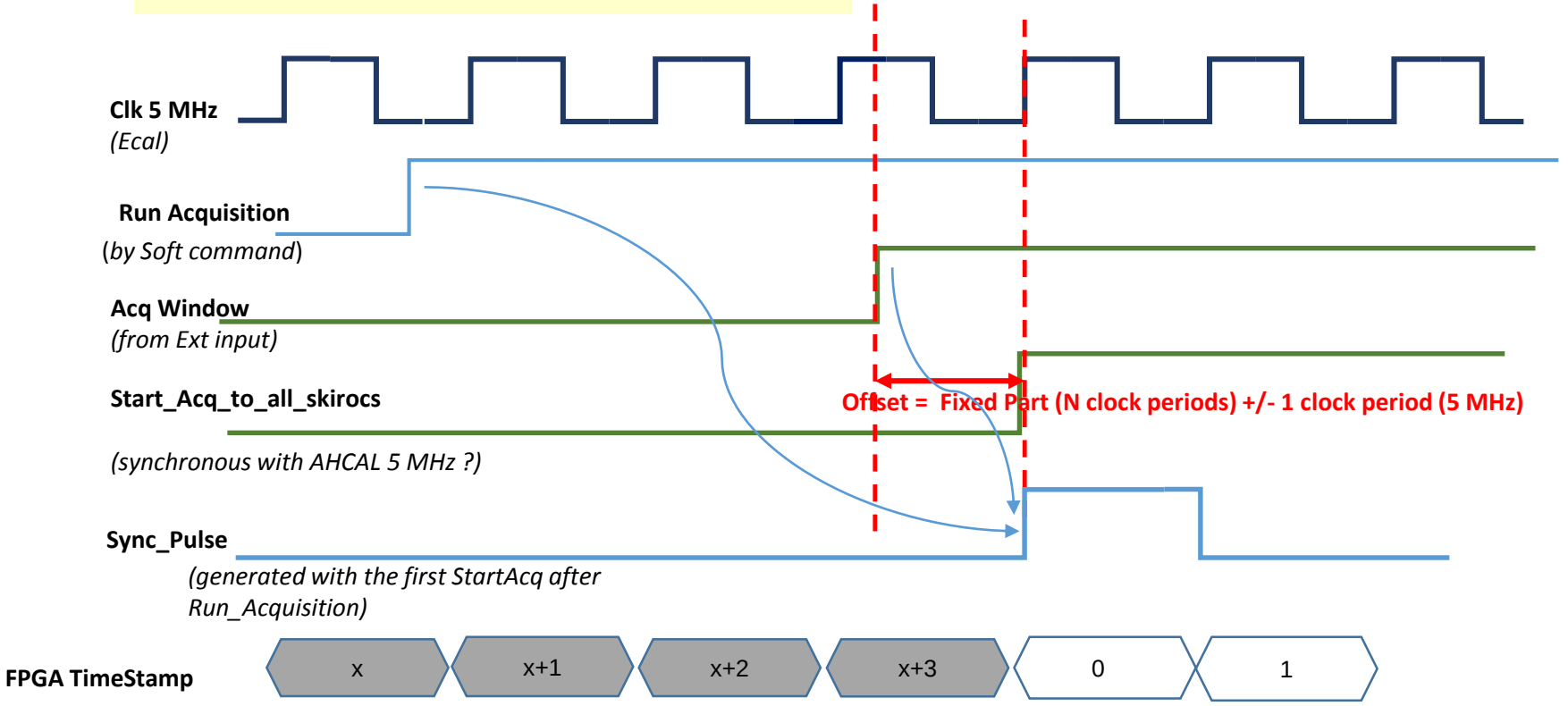
CORE Module inputs/outpus are **SMA female.**
➔ We will need **Lemo to SMA male adapters**

# Reminder of sychronisation chronograms (1/2)



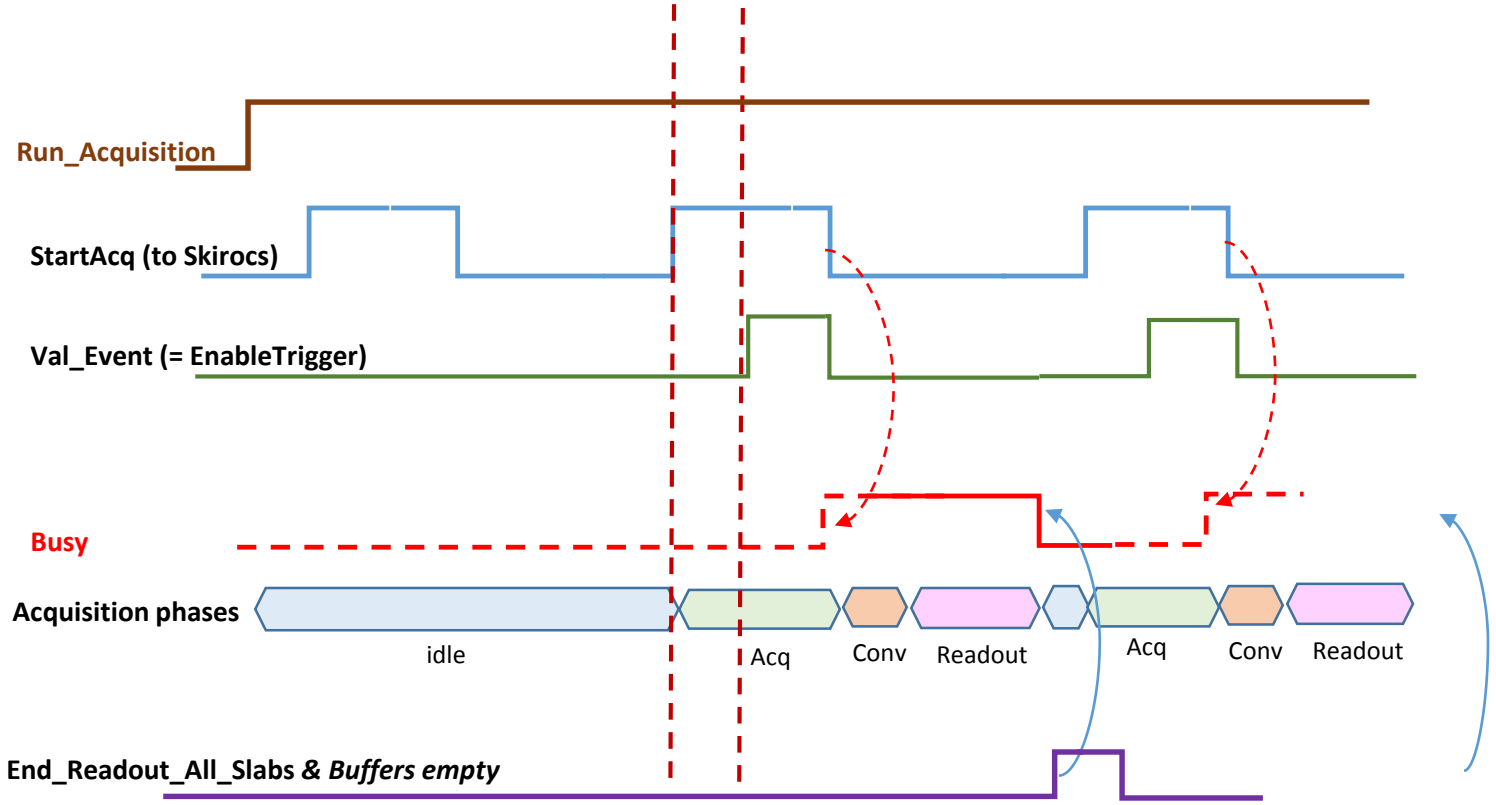

**PhaseB – PhaseA = fixed Offset between AHCAL and ECAL at each power ON**
**Max = 200 ns (1 clock period of 5 MHz)**

Phase offset between AHCAL and ECAL




TimeStamps in AHCAL and ECAL have a **fixe offset part** due to synchronization stages in the firmware.

# Reminder of sychronisation chronograms (2/2)




- Busy signal permits to send “Start Acq” only when both systems are ready.
- CCC is the master.

# What about common DAQ? EUDAQ…

Proposal:

- Add EUDAQ interface to the current software.
  - Keep the graphical interface
  - Start/Stop Acquisition from EUDAQ commands.
  - Send data via network + local data saving to disk
- Question : How does it affect acquisition speed?
- Need a protocol for commands and data acquisition:
  - Commands:
    - Load setup from file
    - Start Acquisition
    - Stop Acquisition
    - Others?
  - Protocol for data acquisition with handshake ?
- is it possible to organize tests before the test beam?