CALICE Collaboration Meeting

Progress of Fast Timing Electronics with PETIROC2B for SDHCAL

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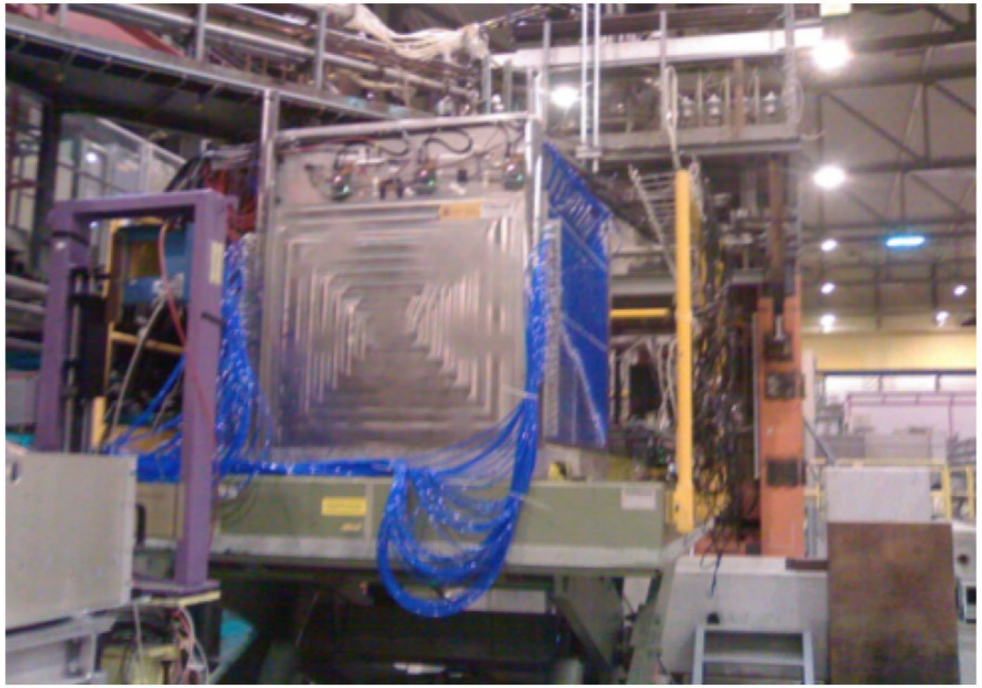
Outline

- Introduction of SDHCAL prototype
- Motivation of using timing information
- Prototype of Front End Electronics (FEE)
- Design of data acquisition system
- Brief summary and future plan

Introduction of SDHCAL prototype

- Semi-Digital Hadronic CALorimeter technological prototype (SDHCAL)
- High granularity calorimeter based on Glass RPC (cell size 1cm × 1cm)
- **Hits associated to three thresholds**:
  - 1^{st} threshold = 110fC
  - 2^{nd} threshold = 5pC
  - 3^{rd} threshold = 15pC

  → Semi-digital readout (0, 1, 2)

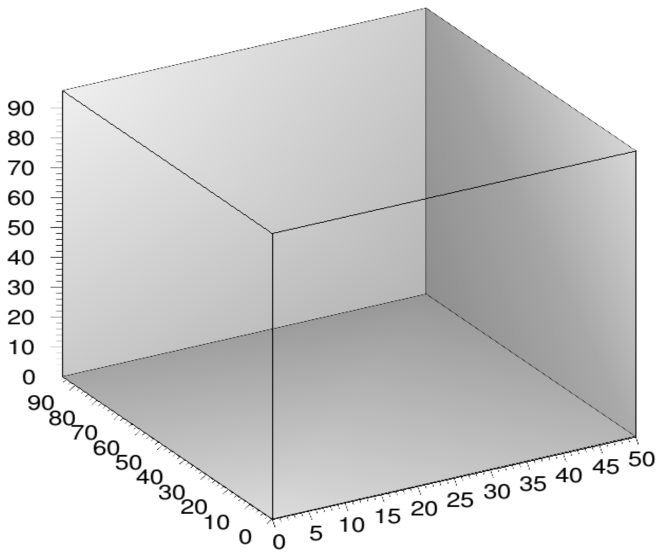


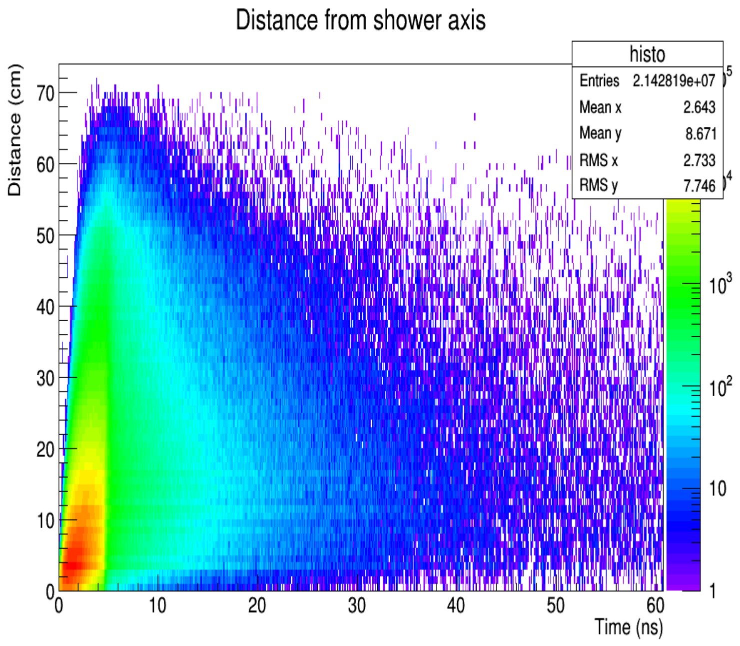
- 48 layers with GRPC as sensitive medium

  → Dimensions: 1m × 1m × 1.3m
- 6 Interaction length ($6\lambda_I$)

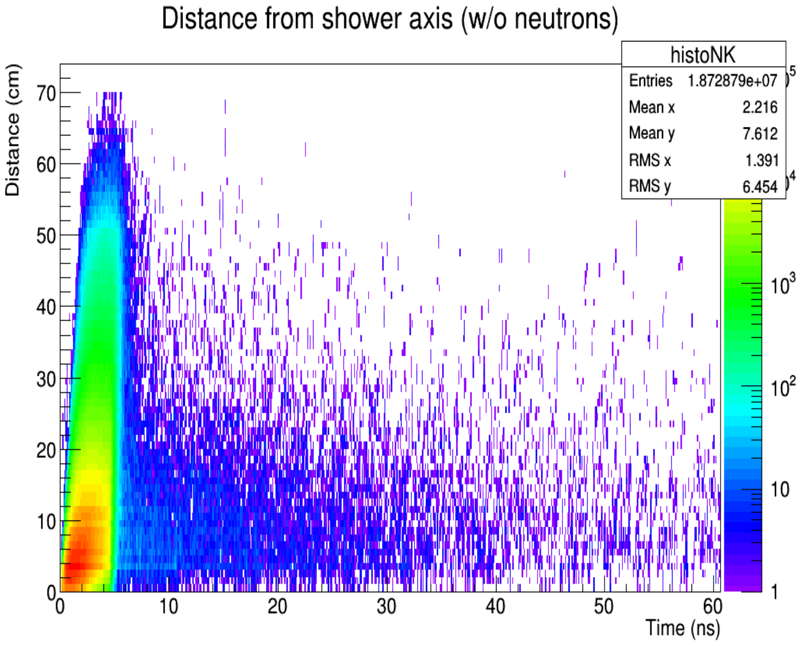
Motivation using timing information

- Timing could be an important factor to identify delayed neutron and **better reconstruct their energy**.





With Neutrons

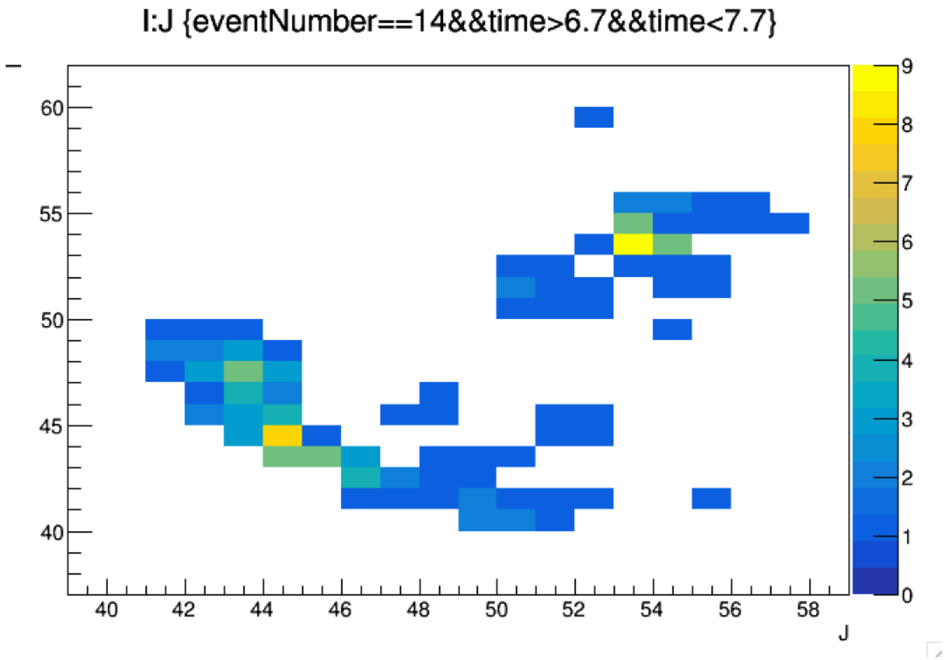


Without Neutrons

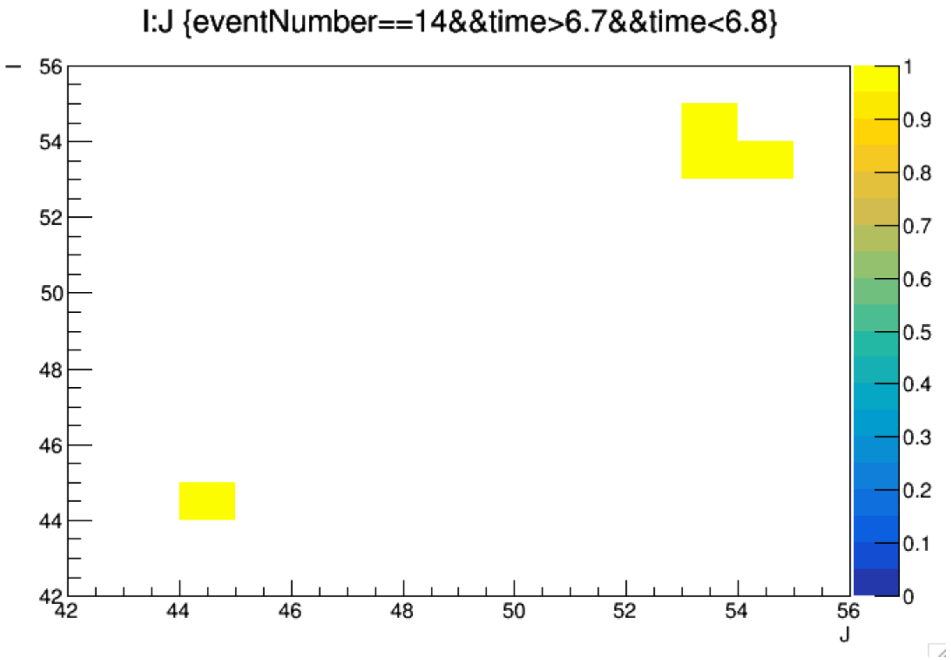
Timing information

- Time information can be very helpful to **separate close by showers** and **reduce the confusion** for a better PFA application.

1 ns resolution

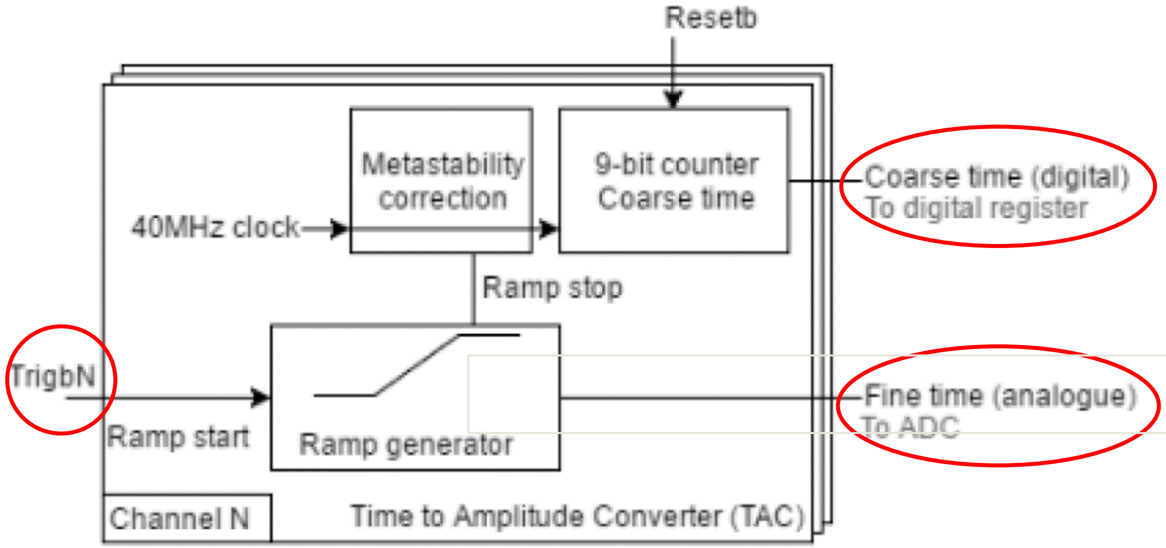


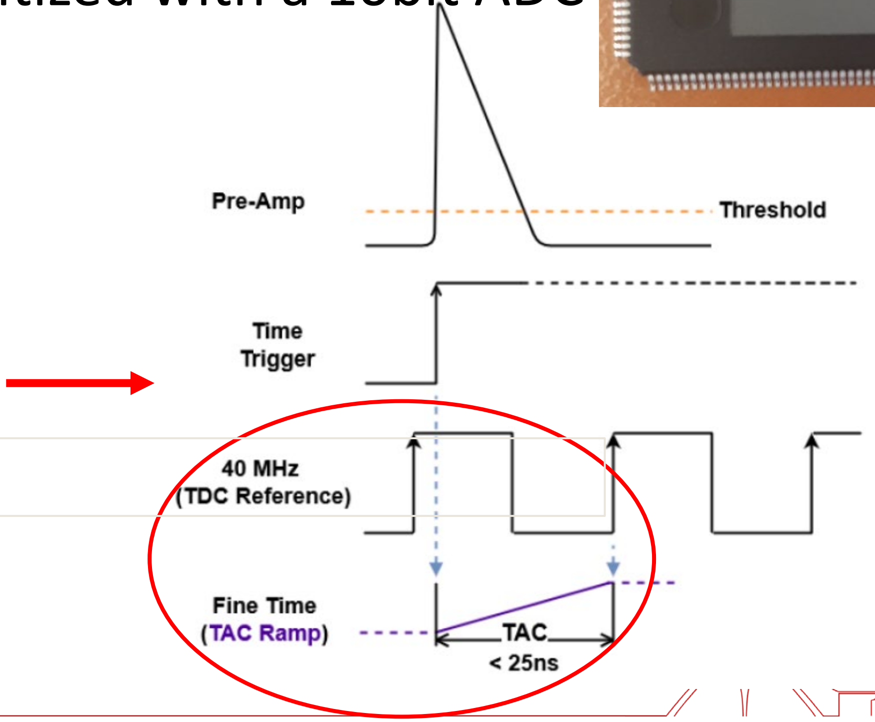
100ps resolution



Introduction of PETIROC

- Time measurement
  - Coarse time is from a counter
  - Fine time by interpolating 40MHz
  - Jitter ~18 ps RMS on trigger output (4 photoelectrons injected)
- Charge measurement
  - 32chs input connected with PAD (readout unit)
  - Variable time shaper
  - Digitized with a 10bit ADC





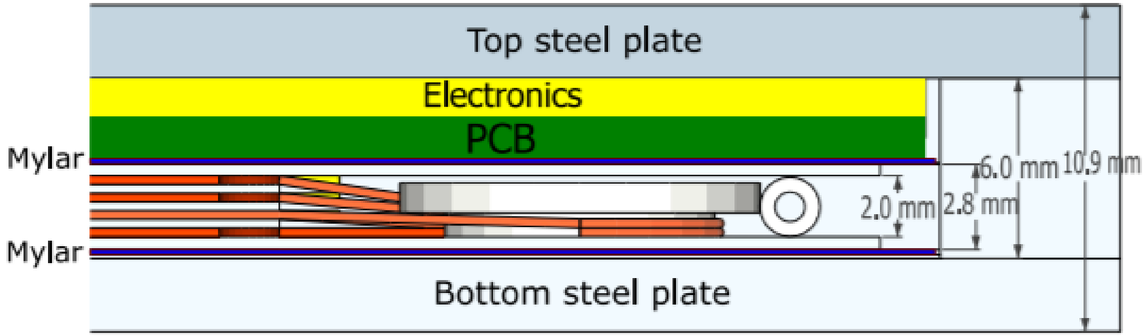
How to achieve fast timing measurement

- Purpose: => Identify neutral and charged hadrons
- Position, Energy and **Timing** => 5D HCAL

- Adding MRPC layers in the SDHCAL
- Front-end board for MRPC readout
  - Charge and timing measurement
  - High resolution timing measurement

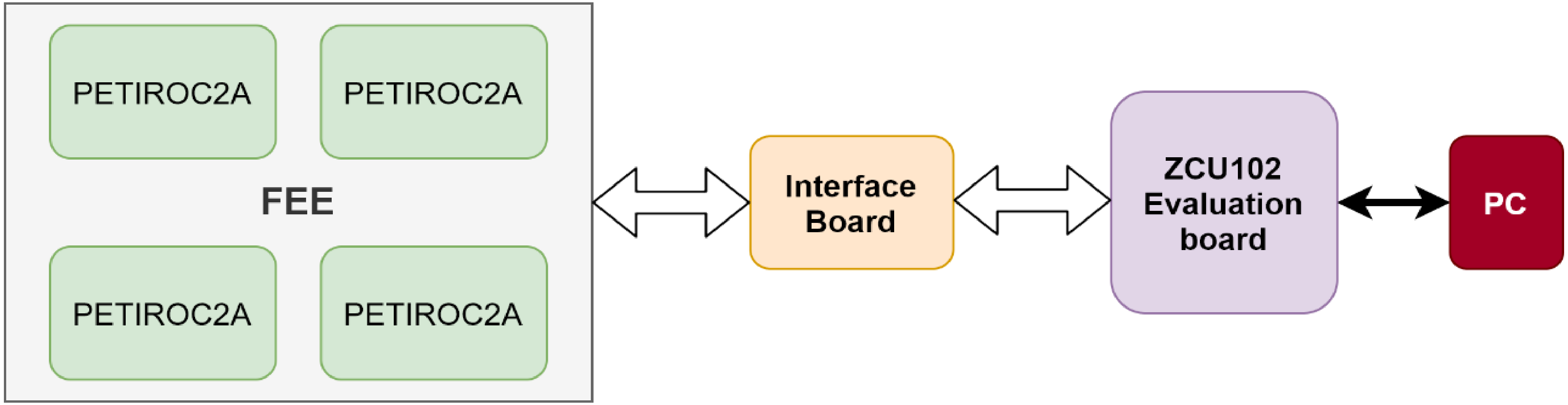
✓ First step：
Design a front-end prototype board with four PETIROC2B chips

➢ Second step:
Build the 1m╳1m **PETIROC2B FEE**

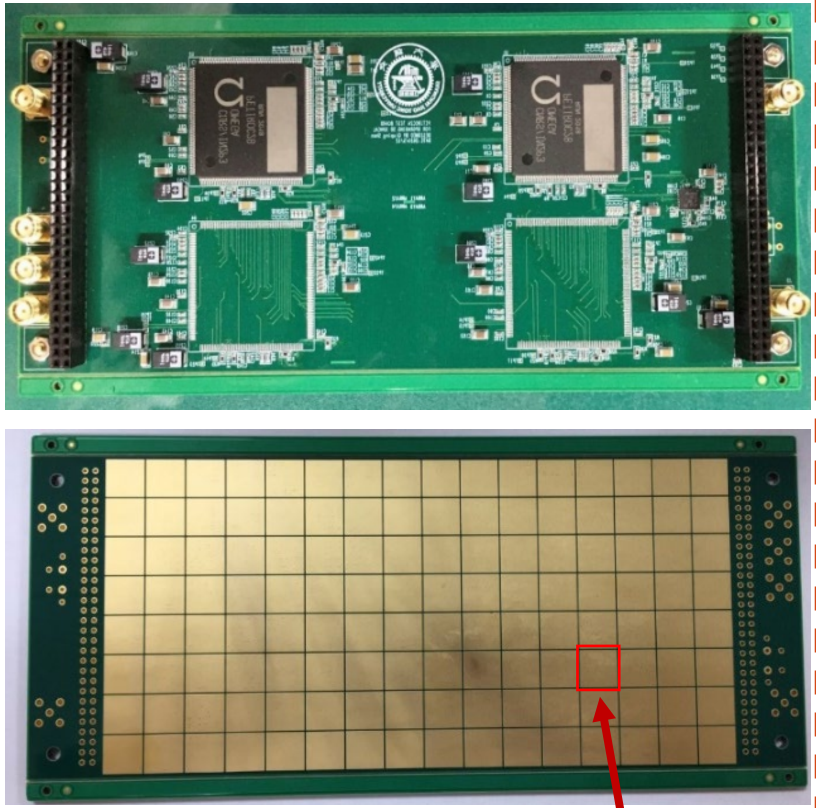


Prototype of timing electronics

- The FEE prototype includes four PETIROC chips, 128 readout pads on the PCB bottom side.
- Detector Interface(DIF) card was designed to connect FEB and FPGA board
  - Data transmission, power rail and clock source.
- The DAQ system should be developed to transfer data between FPGA and PC.

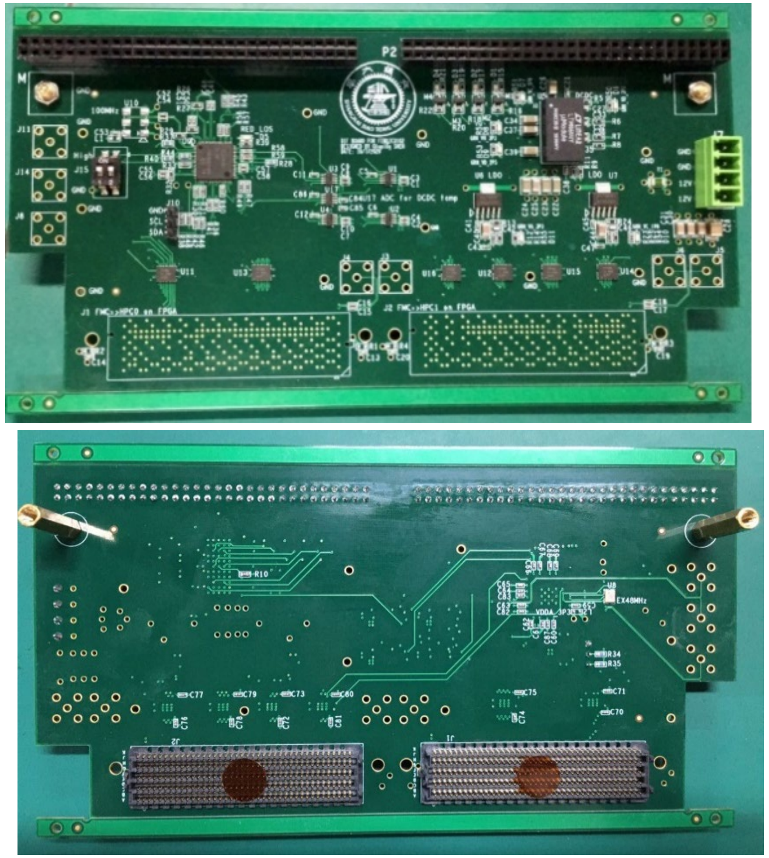


Hardware of prototype

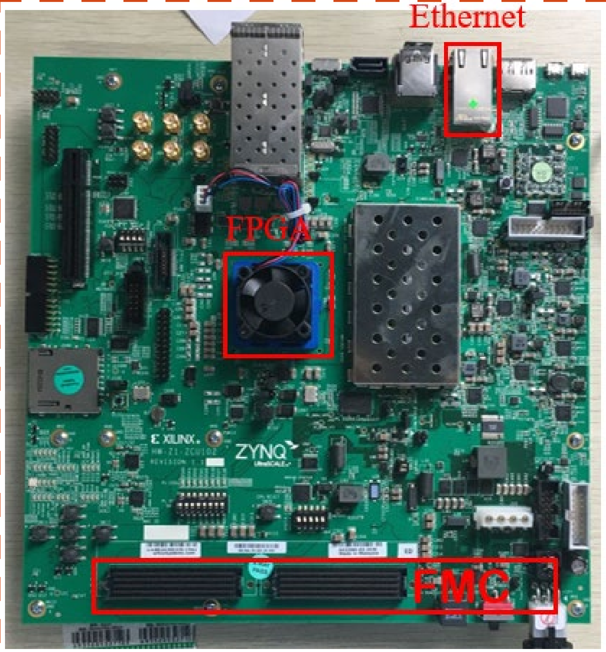


FE Board

128 pads with the cell size 1cm × 1cm



DIF Card

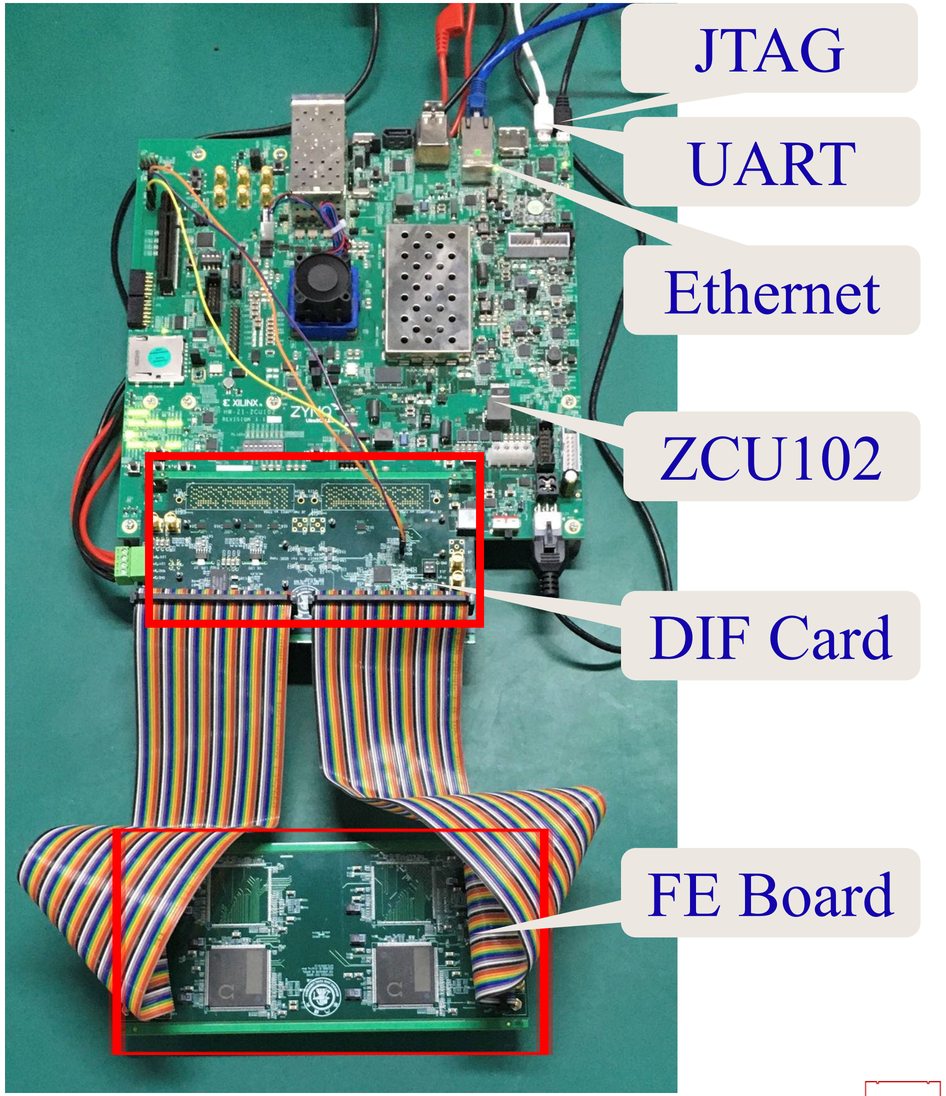


ZCU102

Test system and setup

- The test platform has been setup.
- **FEB, DIF card, DAQ** based on ZCU102

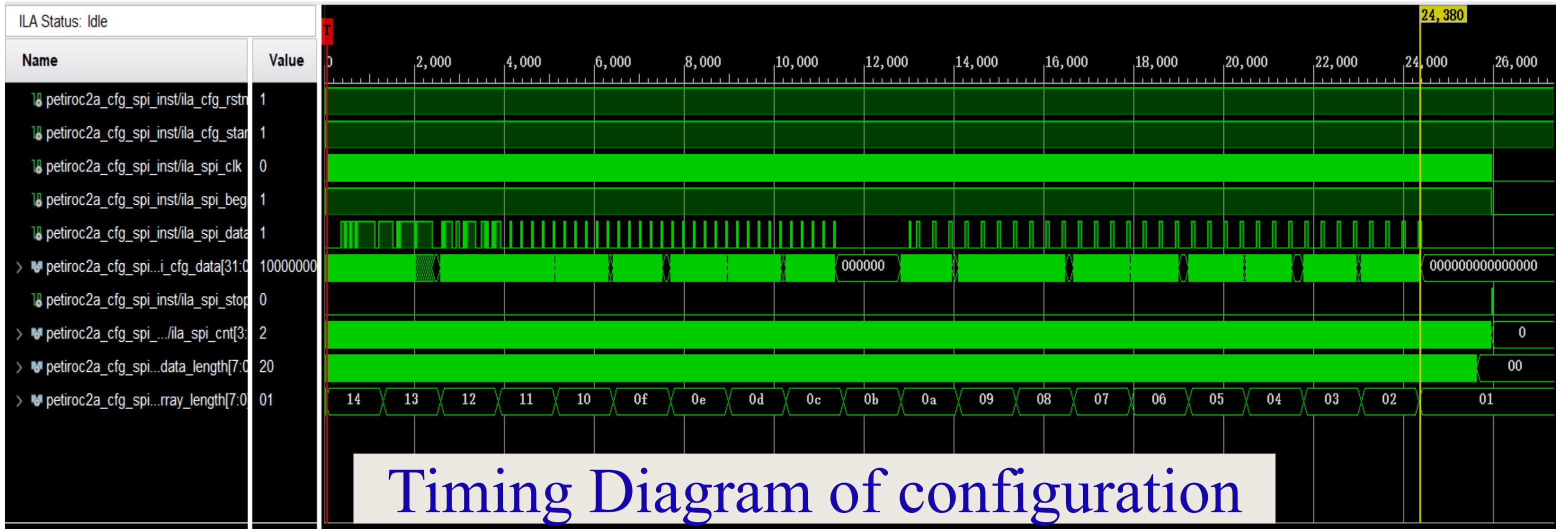
- Status of the platform:
  - Configuration of PETIROC
  - Data transmission between FEB, FPGA and PC
  - Performance test of PETIROC chips, timing measurement



PETIROC chips configuration

- 648 bits data with SPI method is sent to Shift Register inside PETIROC.
- PETIROC configuration works well.
  - All bias voltage values are correct.
  - Output data has been checked, after sending trigger signals

Configuration FPGA Logic

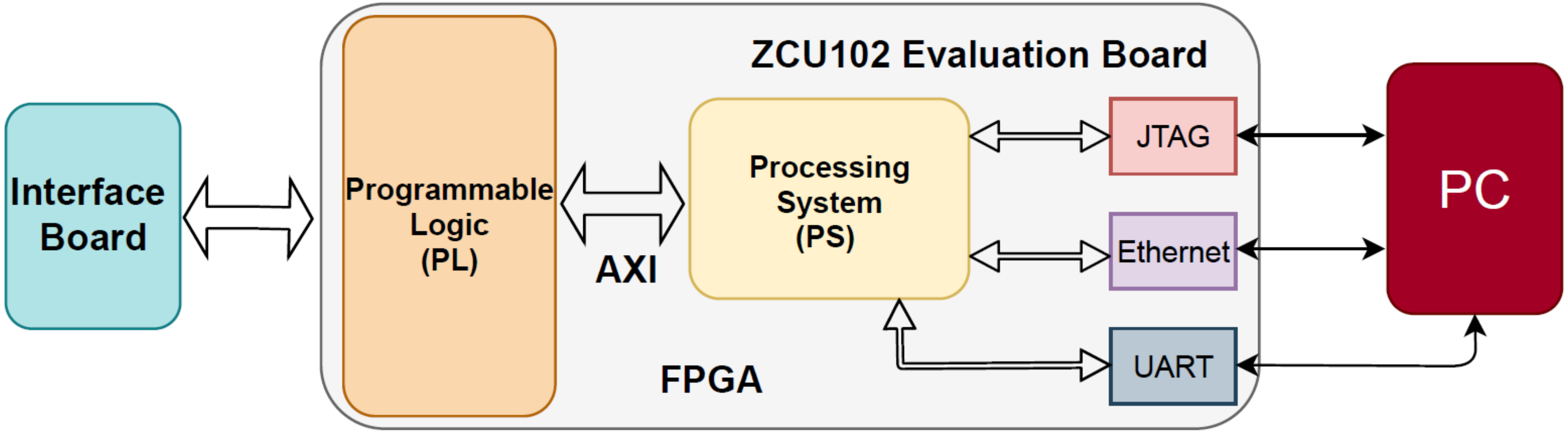


Timing Diagram of configuration

Bias Voltage	Value(V)
vref_inpdac	0.989
vref_time	1.664
vref_charge	0.976
vref_tdc	0.133
vref_adc	0.961
vref_time_pad	1.658

Data acquisition system design

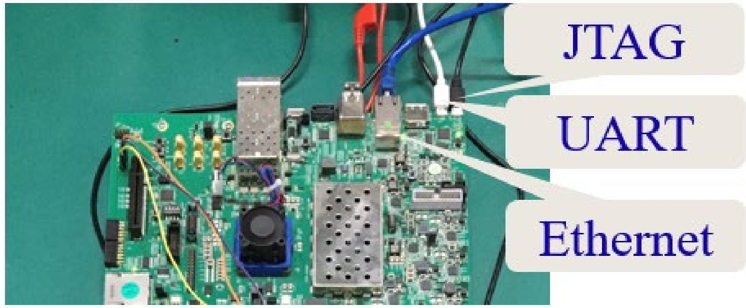
- DAQ system is based on Xilinx ZCU102(FPGA) that contains Processing System(PS) and Programmable Logic(PL).
- Embedded design (SDK) in ZCU102(PS) side
  - The UART communication of FPGA and PC
  - Ethernet communication between FPGA and PC used to transfer data
  - Data transmission with AXI Bus between PS and PL, inside of ZCU102



FPGA Logic Design Block Diagram

DAQ system -- UART

- The embedded design in ZCU102(PS side) contains:
  - Serial port communication (UART)
  - Ethernet communication (TCP/IP)

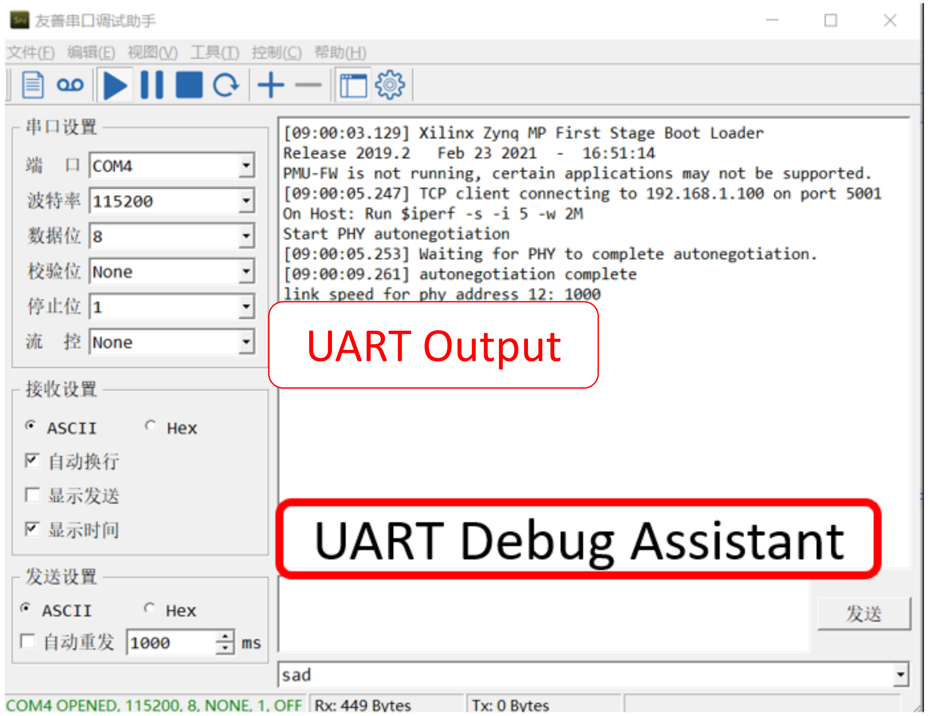


- UART test in PS side:
  - Hardware only needs Processing System part on ZCU102.
  - Run the C++ program on the hardware platform.
  - Information is printed on the tool window through UART port.

PS code

1

```c
#include <stdio.h>
#include <string.h>

#include "lwip/err.h"
#include "lwip/tcp.h"
#include "lwipopts.h"
#include "xil_cache.h"
#include "xil_printf.h"
#include "sleep.h"

#define TX_SIZE 102

static struct tcp_pcb*connected_pcb = NULL;
unsigned client_connected = 0;
//Static Global Function, blind for external file
uint tcp_trans_done = 0;

//u_char data[TX_SIZE] = {0, 1, 2, 3, 4, 5, 6, 7, 8, 9};
u_char data[TX_SIZE] = "Hello World! Successfully Send Word From PS Client";

int send_data()
{
    err_t err;
    struct tcp_pcb *tpcb = connected_pcb;

    if (!tpcb)
        return -1;

    //判断发送数据长度是否小于发送缓冲区剩余可用长度
    if (TX_SIZE < tcp_sndbuf(tpcb)) {
        //Write data for sending (but does not send it immediately).
        err = tcp_write(tpcb, data, TX_SIZE, 1);
        if (err != ERR_OK) {
            xil_printf("txperf: Error on tcp_write: %d\r\n", err);
            connected_pcb = NULL;
            return -1;
        }

        //Find out what we can send and send it
        err = tcp_output(tpcb);
        if (err != ERR_OK) {
            xil_printf("txperf: Error on tcp_output: %d\r\n",err);
            return -1;
        }
```



UART communication test

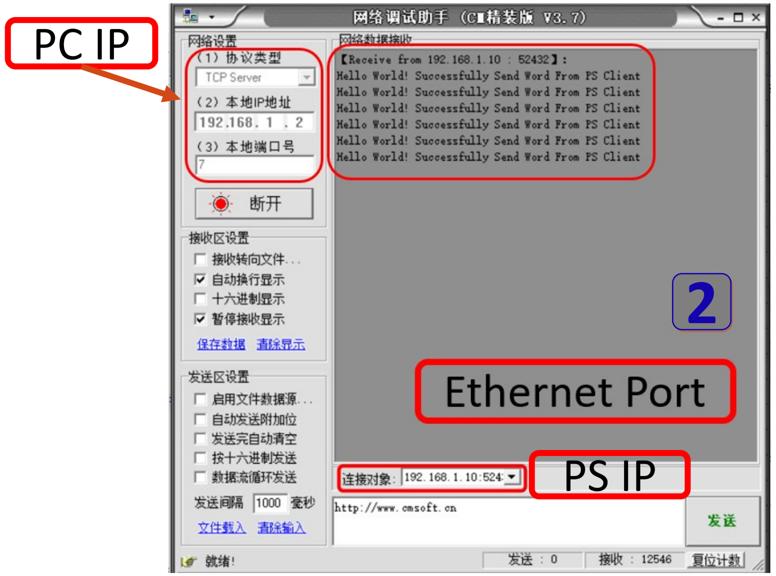
DAQ system -- Ethernet

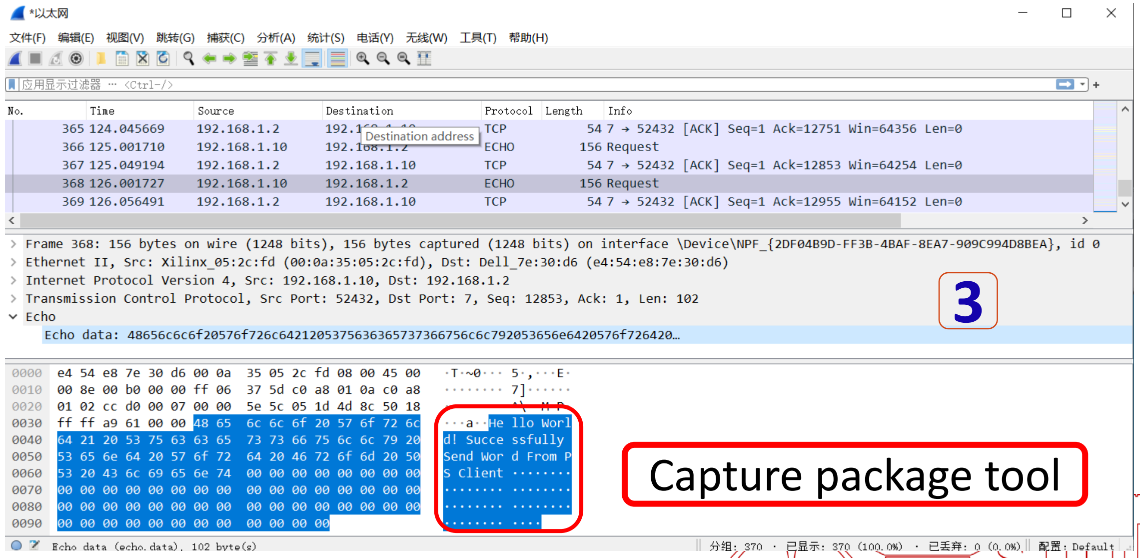
- Ethernet communication test:
  - 1 PS program sent the data to PC.

```
//u_char data[TX_SIZE] = {0, 1, 2, 3, 4, 5, 6, 7, 8, 9};
u_char data[TX_SIZE] = "Hello World! Successfully Send Word From PS Client";
```

  - UART used to print PS information (IP, Sub netmask, Gateway)
  - 2 Ethernet port connected with PC, used to test the transmission and print the transfer data.
  - 3 Capture package tool can grab the transmit information.

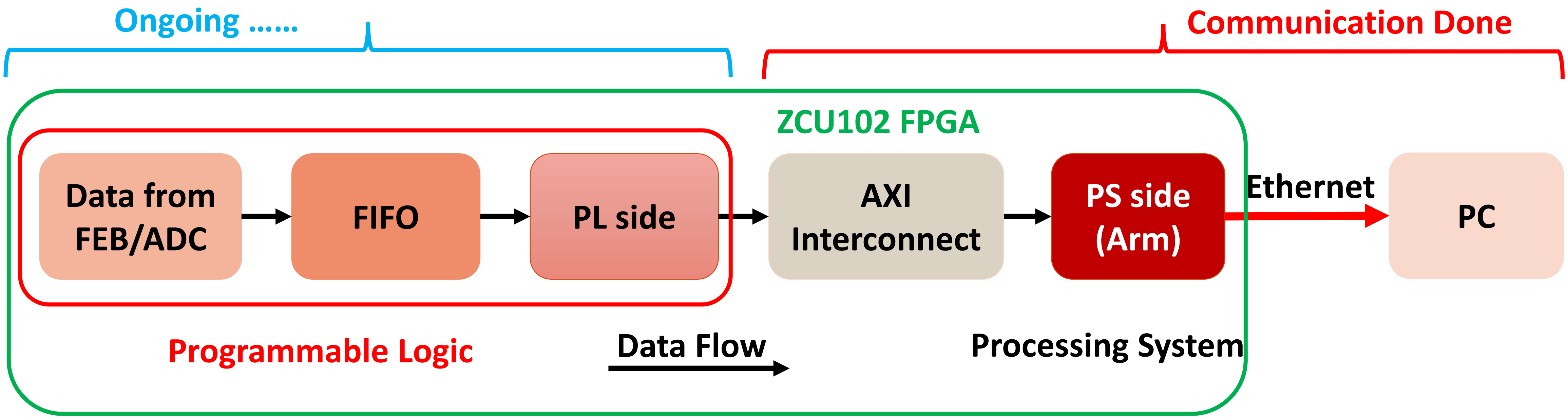
- ZCU102(PS) and PC can successfully communicate over ethernet.





Design of DAQ system

- UART communication works well.
- Ethernet transmission between ZCU102(PS) and PC is completed.
- The communication between FE Board, FIFO and ZCU102(PL) is ongoing.
- The configuration of PETIROC chips over ethernet will be included.



Brief summary and future plan

Summary:

- The timing electronics have been designed and manufactured.
- Test platform and setup for PETIROC have been constructed.
- PETIROC chips can be successfully configured.
- Ethernet transmission between FPGA and PC has been realized.
- The design of DAQ system is still under the development.

Future Plan:

- Continue the design of DAQ system based FPGA ZCU102 to achieve the data transmission and slow control over the ethernet communication.
- Perform the signal injection test for PETIROC FE board (Timing and Charge)

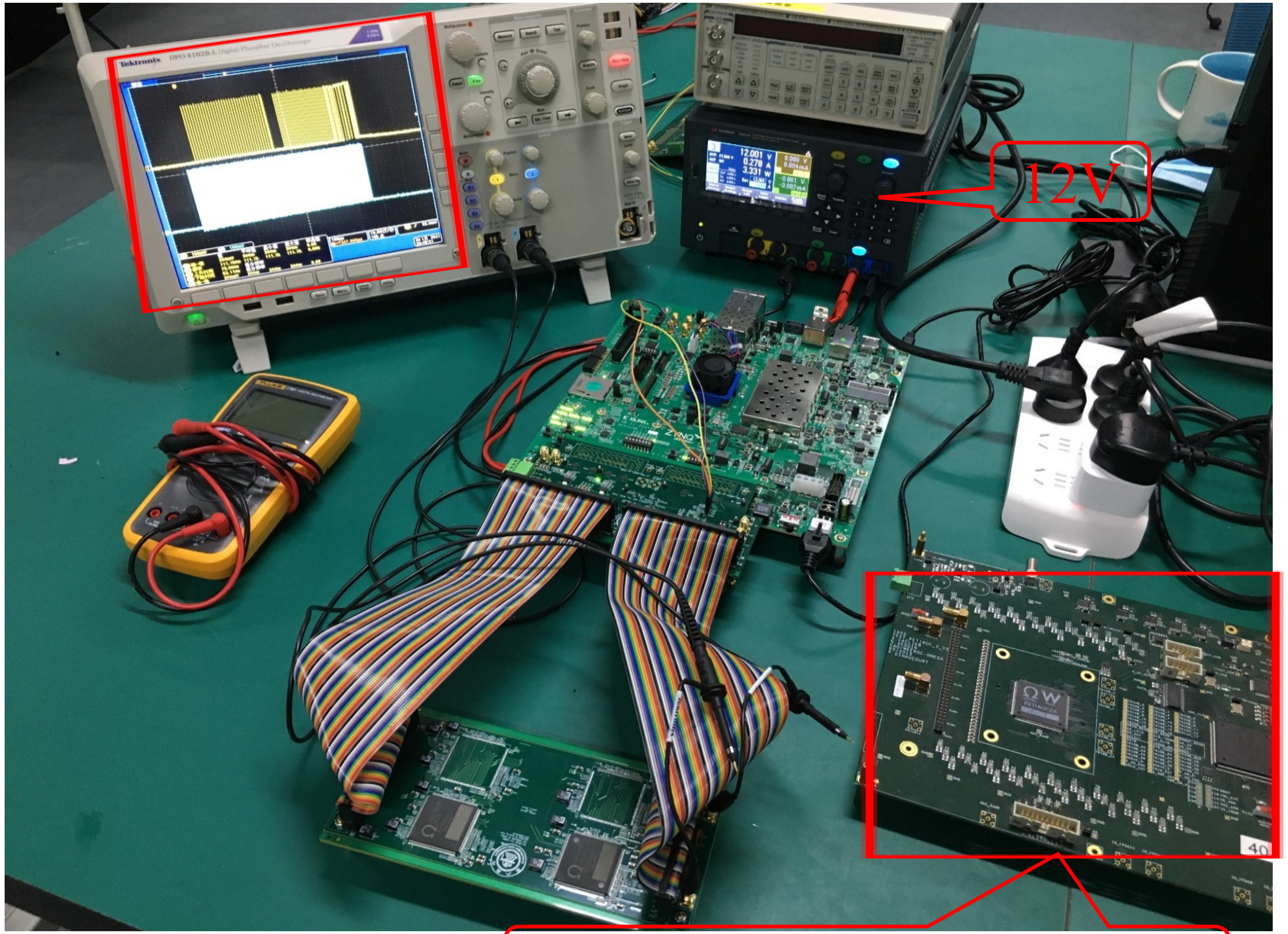
Thanks for your attention!

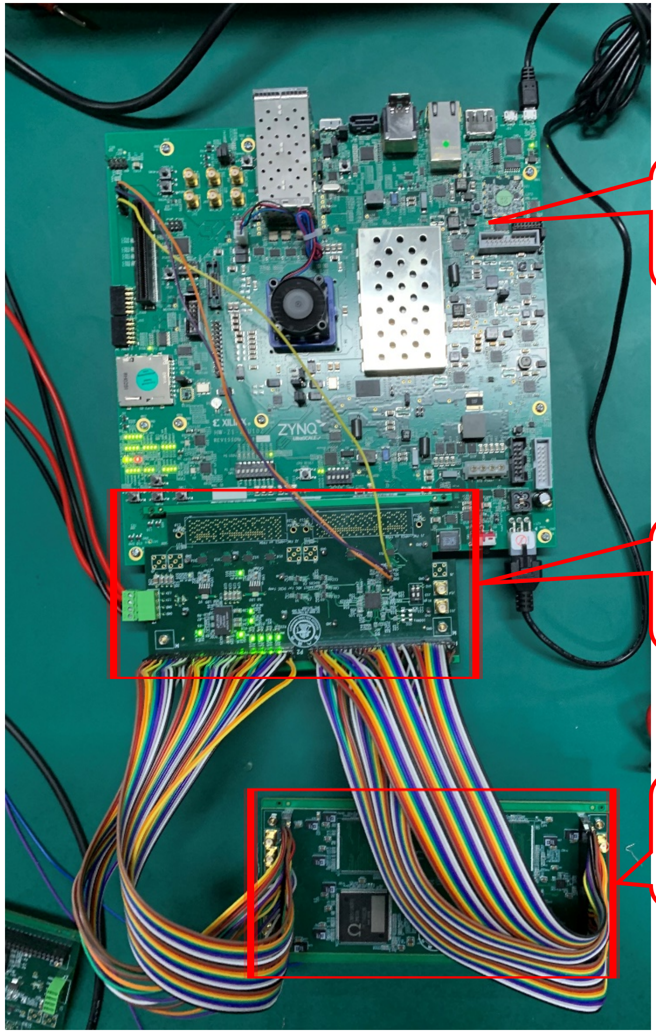
Backup Slides

Introduction of PETIROC chip

- Time measurement with 10bits TDC interpolating 40MHz coarse time
- Charge measurement (Q>50fC) with 10bits DAC
- Voltage input amplifier, 200Ohm matching
- High bandwidth preamp (GBWP> 1.2 GHz)
- PETIROC parameters:
  - One chip with 32-channels and mixed analog/digital
  - The 32chs input connected with PAD (detector unit)
  - One channel split into two parts, respectively for charge and time measurement
  - Internal DAC for each channel to adjust the amplitude of the input signal
  - Lower power consumption (~6mW/channel)
  - Jitter ~18 ps RMS on trigger output (4 photoelectrons injected)

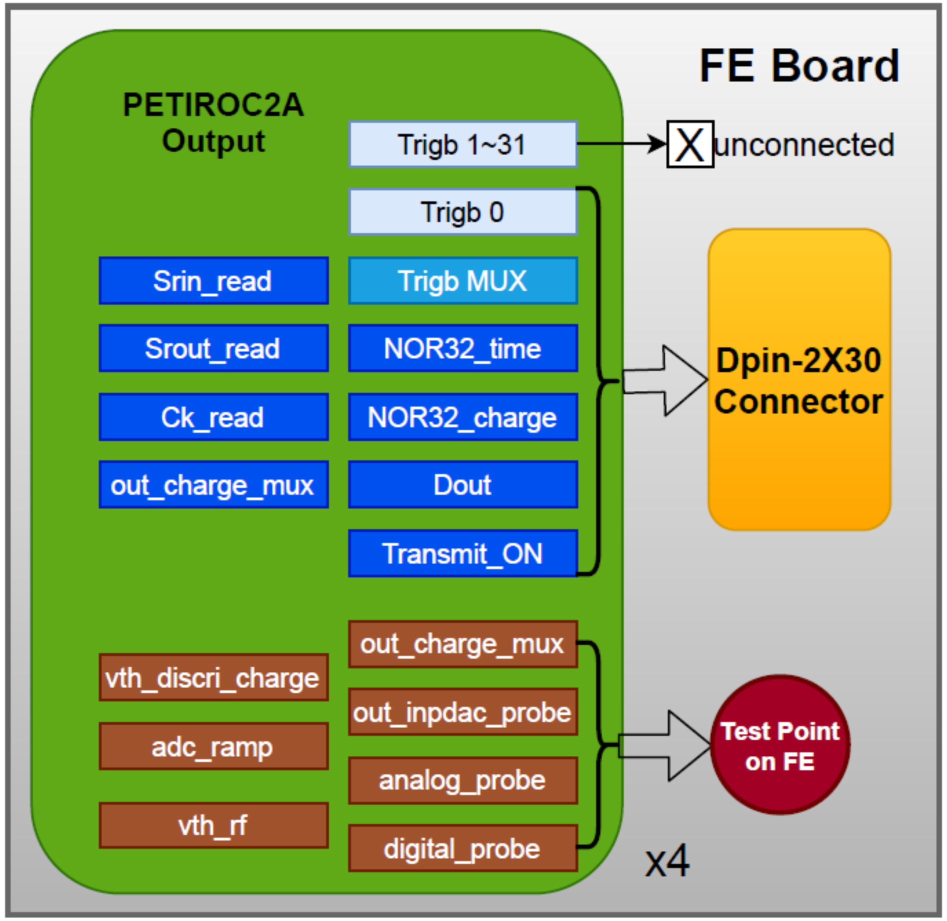
Test System and Setup



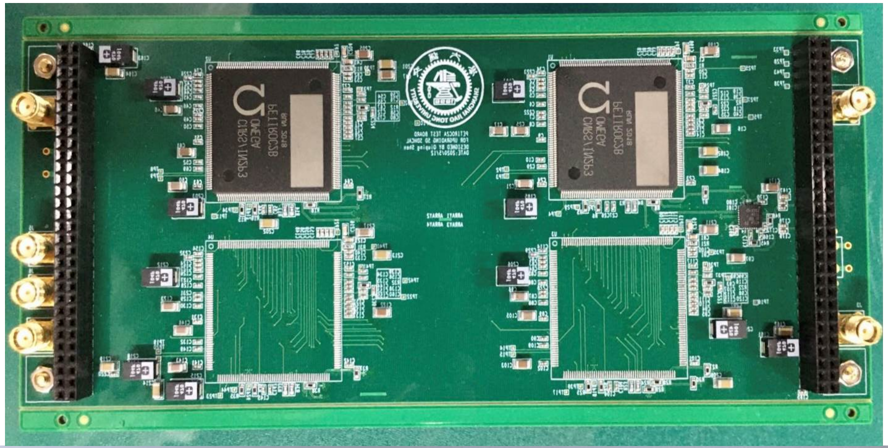


Sub-component Design and Testing

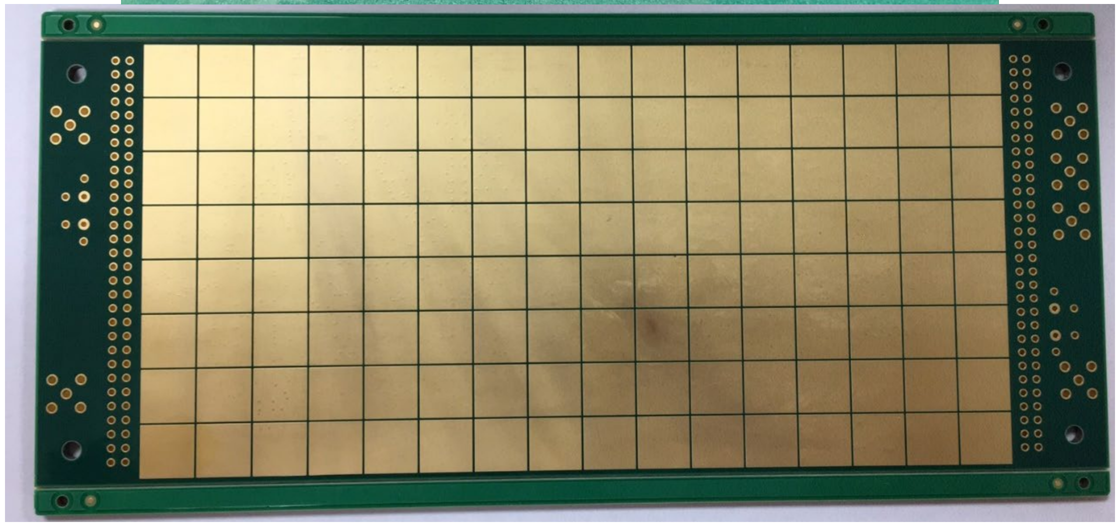
- Front-End readout Board Design with pads and four petiroc2b



Block diagram of front-end electronics



Front



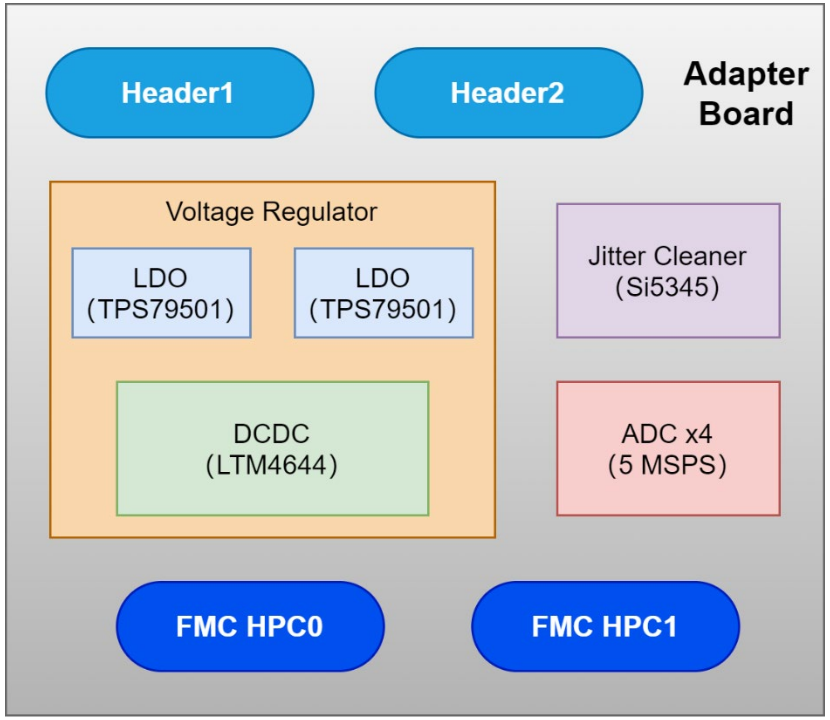
Back

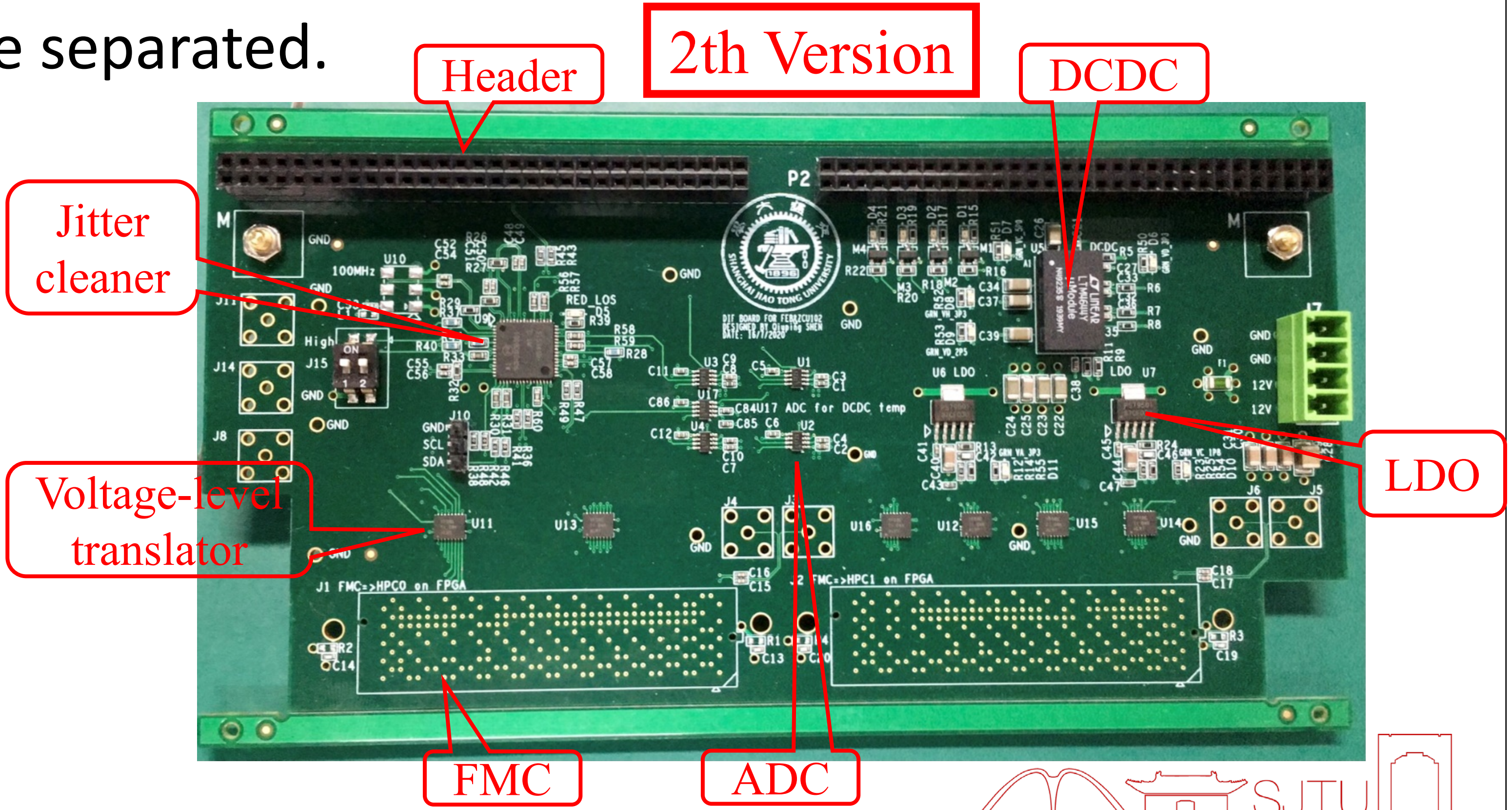
Sub-component Design and Testing

- Detector Interface Card Design: mainly jitter cleaner and power system
- DIF card will be in charge of the communication and data transfer with the FE electronics(two headers) and ZCU102(two FMCs).

More Details

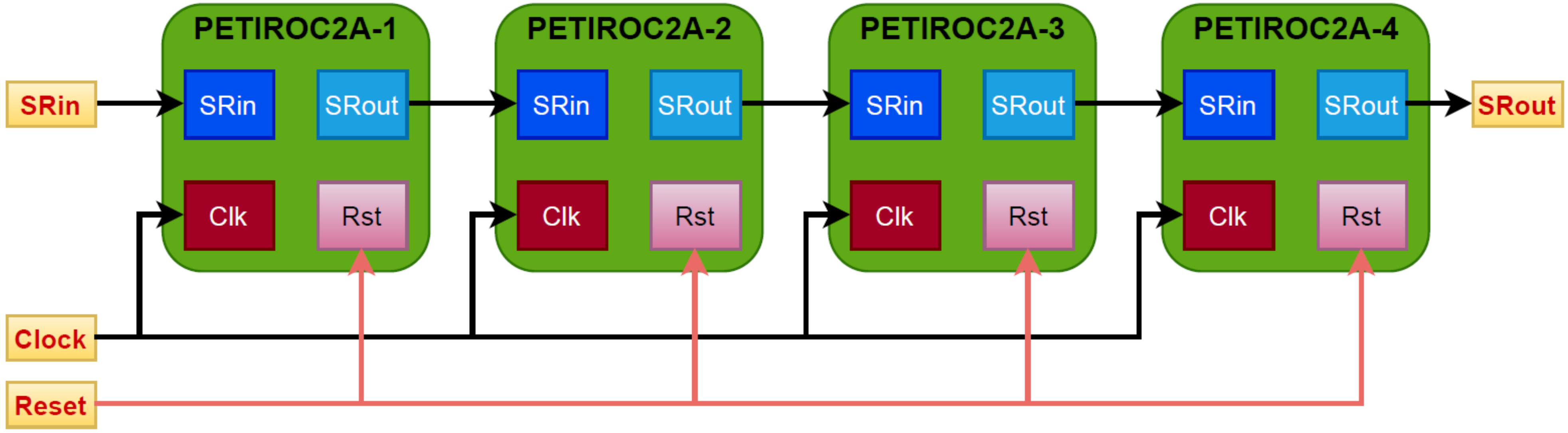
- Analog and digital power are separated.





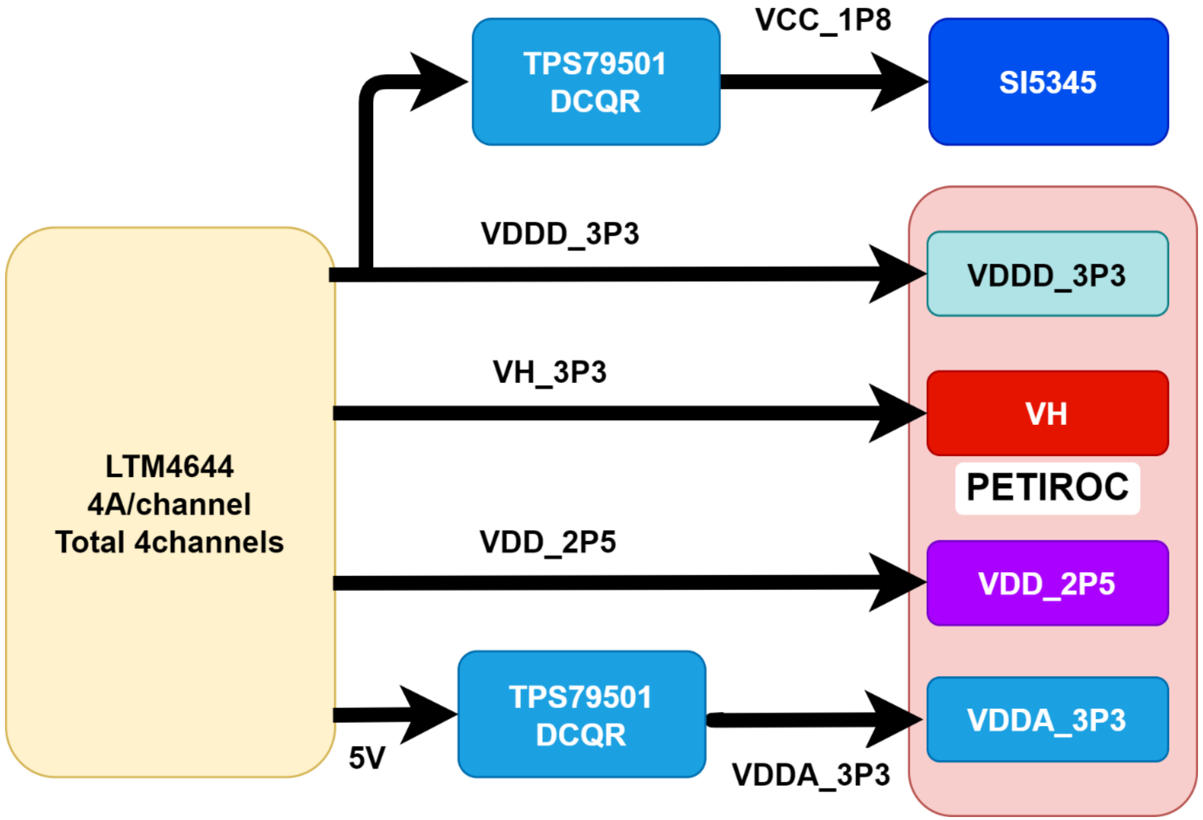
Sub-component Design and Testing

- Front-End readout Board Design
- Components: 4 Petiroc2B, clock buffer, 2 headers, SMA for signal injection .
- 128 pads at the bottom, induction unit size: 1cm × 1cm.
- The dimension:197mm*82mm, the blind/buried via technology.
- Configuration for petiroc2a with daisy-chain (SPI sending shift register data)

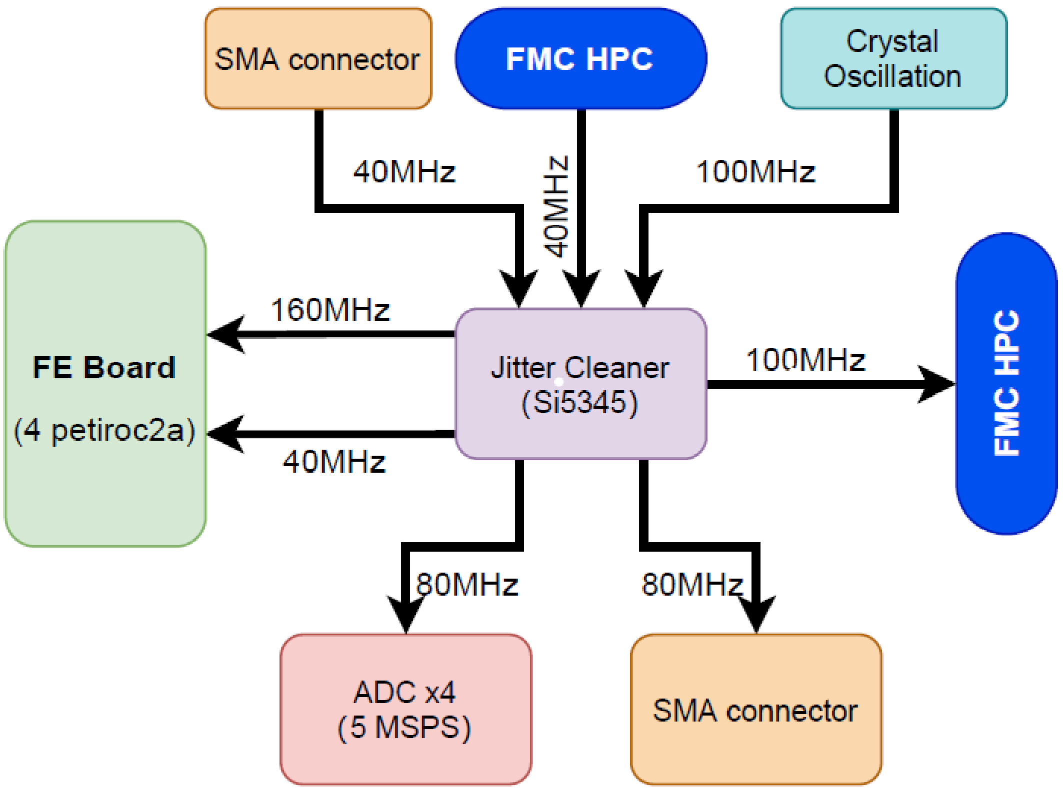


Details on DIF Design and Testing

- Detector Interface Card Design: mainly jitter cleaner and power system



Block diagram of Power Rail



Block diagram of Clock