News on FEV2.0

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IJClab - LLR

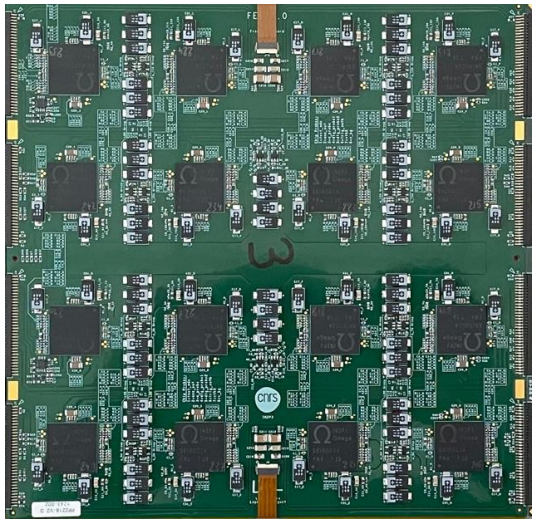
New FEV2.0

- ❑ Dimensions: 180mm x 180mm
- ❑ Thickness: 1.6mm
- ❑ New features:
  - ❑ Local LDO to reduce common noise and cancel voltage drop
  - ❑ Locally buffered clock for configuration the system
  - ❑ New connector for interconnexion
  - ❑ Add connector & HV filter for individual wafer
  - ❑ New system with individual HV kapton

Discussion about features of FEV2.1

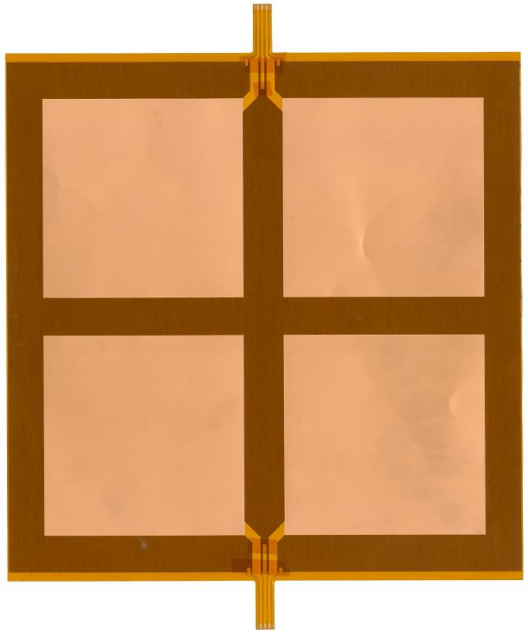
- ❑ Analog probe to check connection to pixel
- ❑ Add thermal sensor + voltage monitoring + unique ID with OneWire chip

  Ex: MAX DS2704



First results are very promising:

- + 7% of good data
- Less crosstalk
- …

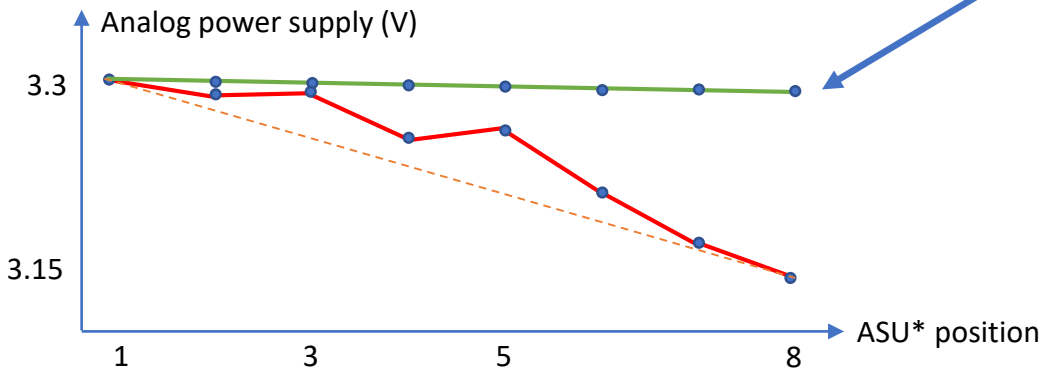


New HV kapton:

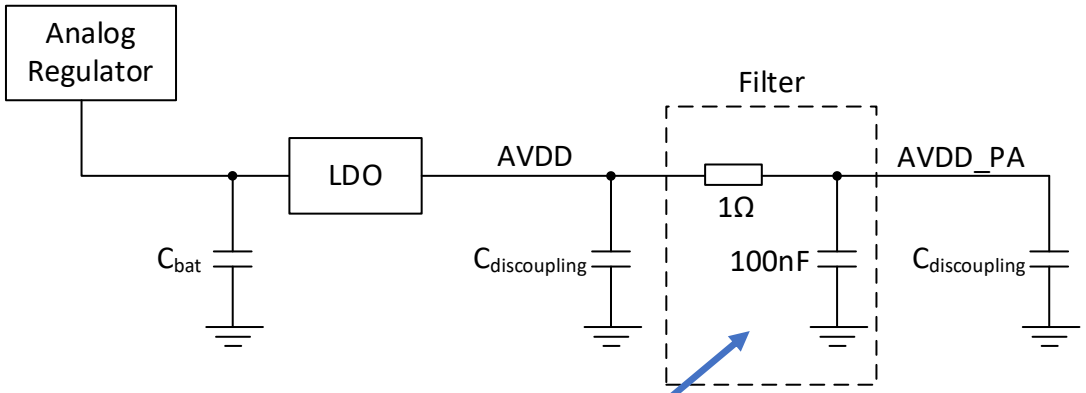
Higher reliability

- Easy to handle ASU
- Only 1 board glued per kapton

Power distribution



ASU* (Active Sensor Unit)



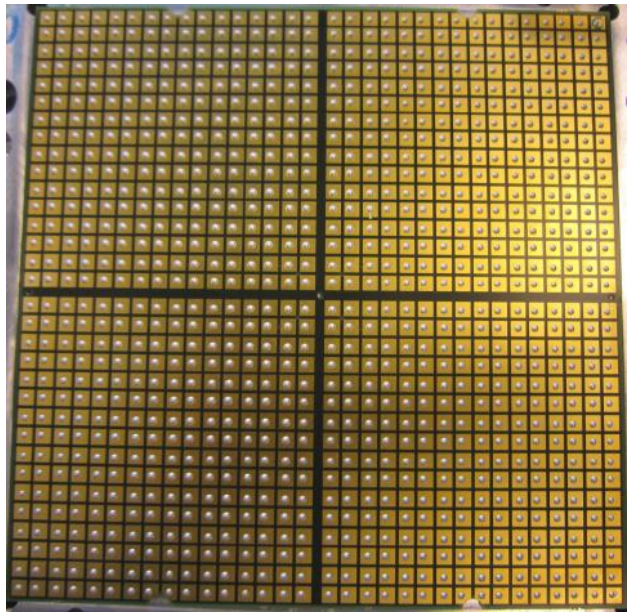
Add filter to generate local preamplifier power supply

Expected results

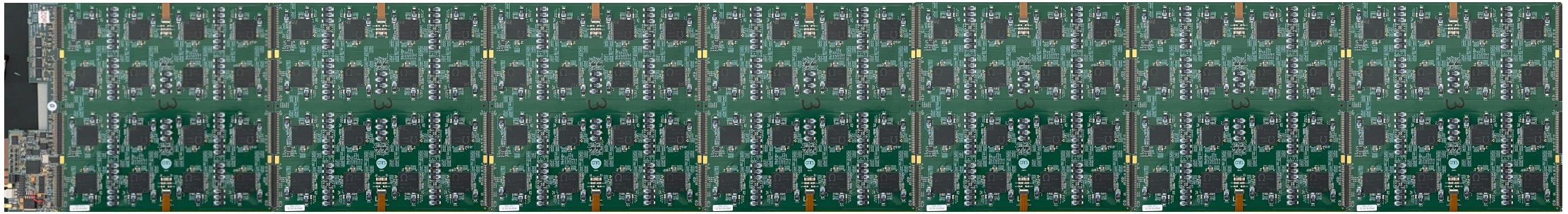
In the electrical long SLAB, 8 boards are chained and due to resistivity of layer per board on analog 3.3V, we measure voltage drop along the long SLAB coupled with bandgap distribution.

→ We decide to generate local power supply with LDO (Low Drop Out) to cancel voltage drop and reduce common noise.

2023 GOALs



- ❑ Understand problem of gluing
- ❑ Assembly 1 ASU (FEV2.0 + wafers + kapton)
  - ❑ If good results → produce 10 PCB of FEV2.0 or 2.1
    - ❑ 360 SK2A chip & 20 wafers available @LLR
    - ❑ Need to buy 12 wafers or ask for collaboration swap
- ❑ Chain 2 to 8 FEV
  - ❑ If good electrical results → Assembly 8 new ASU gradually
- ❑ **Assembly LONG slab of 8 ASU**



Thanks for you attention
Any questions ?