Contribution ID: **96** Type: **Oral presentation using Zoom**

CMOS Upgrade to the Belle II Vertex Detector

Thursday, 28 October 2021 15:30 (20 minutes)

The success of the Belle II experiment at KEK (Japan) relies on the very high instantaneous luminosity, close to 6x10^35 cm-2 s-1, expected from the SuperKEKB collider. The beam conditions to reach such luminosity levels generate a large rate of background particles in the inner detection layers of Belle II. The hit rate in the innermost vertex detector layer will exceed 100 MHz/cm2 translating into radiation levels of 100 Mrad TID and fluences reaching 5x1014 neq cm-2. This beam-induced background creates stringent constraints on the vertex detector, in addition to the requirements coming from the physics performance needed.

Belle II has started to define a vertex detector upgrade program to make it more robust and performant even in the presence of high backgrounds facilitating the SuperKEKB running at high luminosity, coupled to an accelerator consolidation in the timeframe of 2026-2027.

In this context, the Belle II collaboration is considering the possibility to install an upgraded all-layer monolithic pixel vertex detector on the time scale around 2026 and R&D activities on fully depleted CMOS sensors have started. Such an upgrade should provide a sufficient safety factor with respect to the background rate expected at the nominal luminosity and possibly enhance performances with improved vertex resolution and higher tracking efficiency at low momentum range.

New CMOS monolithic technologies for pixel sensors offer a combination of granularity, speed, low material budget and radiation tolerance. In particular, latest developments on the TJ-Monopix2 family make this development to match Belle II requirements and will be the baseline to exploit the design of a fully pixelated 5 layer vertex detector, called VTX.

This talk will review the context of the proposed VXD upgrade with monolithic technologies in Belle II, providing details of the technological proposal, system integration and discussing performance expectations from simulations.

1st preferred time slot for your oral presentation

15:30-17:30 JST (8:30-10:30 CEST, 2:30-4:30 EDT, 23:30-1:30 PDT)

2nd preferred time slot for your oral presentation

19:00-21:00 JST (12:00-14:00 CEST, 6:00-8:00 EDT, 3:00-5:00 PDT)

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Session Classification: C-1: Tracking detectors

Track Classification: Parallel sessions: Detectors: Session C: Tracking detectors