Contribution ID: **89** Type: **Oral presentation using Zoom**

Status of the DoTPiX development:

Wednesday, 27 October 2021 14:36 (24 minutes)

During last year, we made significant progress about the material structures that make the fabrication of a DoTPiX pixel and pixel array a reachable goal. The trend is to obtain a small pixel reaching the 1 micrometre x 1 micrometre scale. The structure was simulated as early as 2017 (N. Fourches, IEEE TED 2017) to assess tits electrical and detector capabilities. A work-group was founded with IRFU and other CNRS laboratories. We will present the successive steps needed for a successful implementation of the DoTPiX on a silicon substrate, with the justifications of the use of a quantum well. . To say the needed epitaxial process which is in course of development at University Paris-Saclay, with full characterisation of the CVD epi-layers. The next step is the evaluation of a NMOS process (LAAS) which will host the DoTPiX structures, with n-channel MOS device characterization. After this technology bottleneck (process) fixed DoTPiX pixels arrays will be made for in-lab characterization.

1st preferred time slot for your oral presentation

19:00-21:00 JST (12:00-14:00 CEST, 6:00-8:00 EDT, 3:00-5:00 PDT)

2nd preferred time slot for your oral presentation

15:30-17:30 JST (8:30-10:30 CEST, 2:30-4:30 EDT, 23:30-1:30 PDT)

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Session Classification: D-1: New technologies & ideas for collider detectors

Track Classification: Parallel sessions: Detectors: Session D: New technologies & ideas for collider detectors