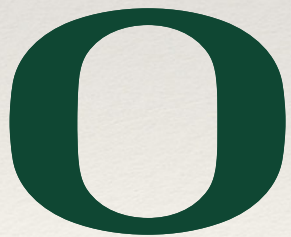




October 27, 2021

The SiD Digital ECal based on Monolithic Active Pixel Sensors

Jim Brau,
University of
Oregon

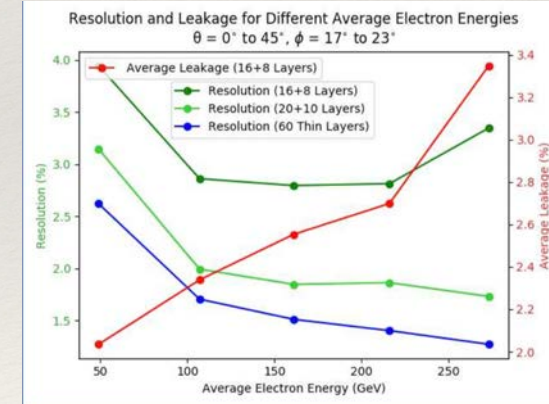
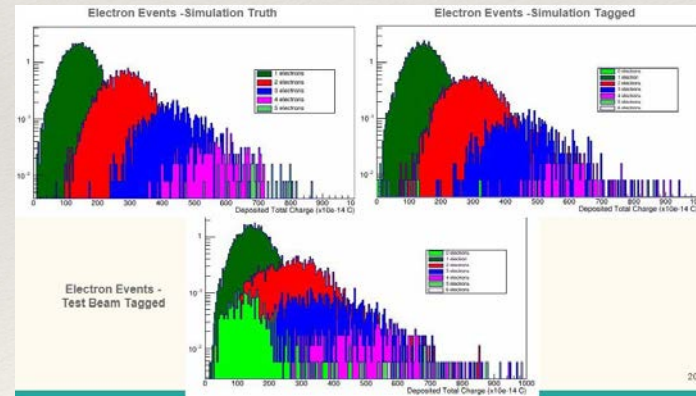
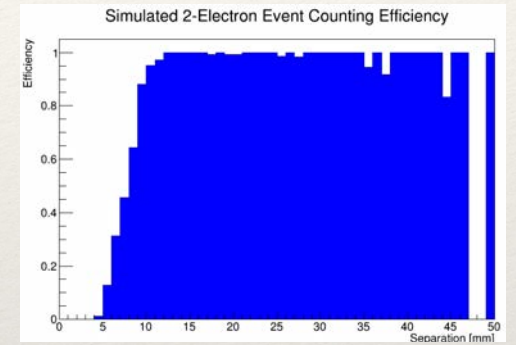
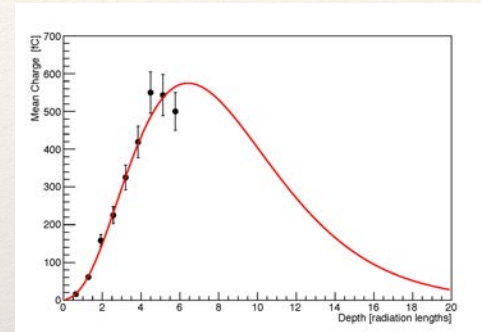
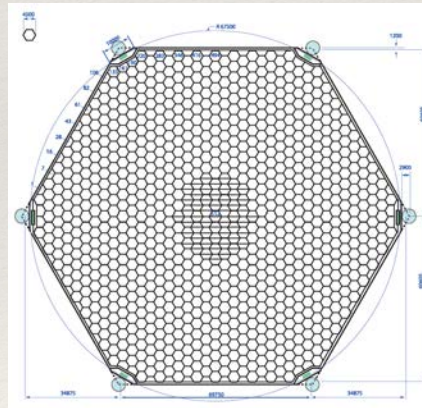
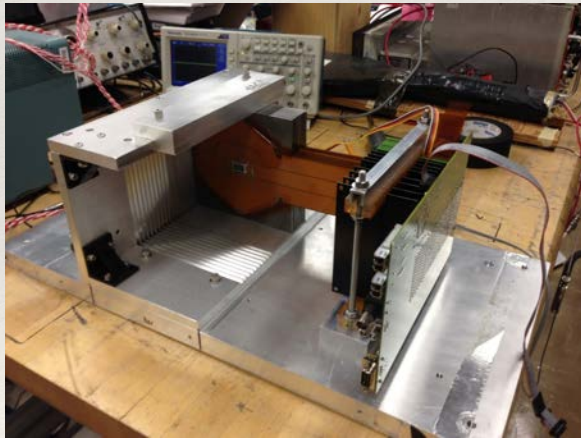


UNIVERSITY OF
OREGON

on behalf of
the SiD MAPS Collaboration
(M. Breidenbach, L. Rota, et al.)

The SiD Digital ECal based on Monolithic Active Pixel Sensors

- ❖ SiD TDR ECal design successfully tested in 9 layer SLAC beam test.
 - ❖ 13 mm² pixels on 6 inch wafers
 - ❖ 1024 pixels per wafer
 - ❖ KPiX readout bump-bonded to sensor



- ❖ Improved ECal design under development based on 25 μm x 100 μm MAPS

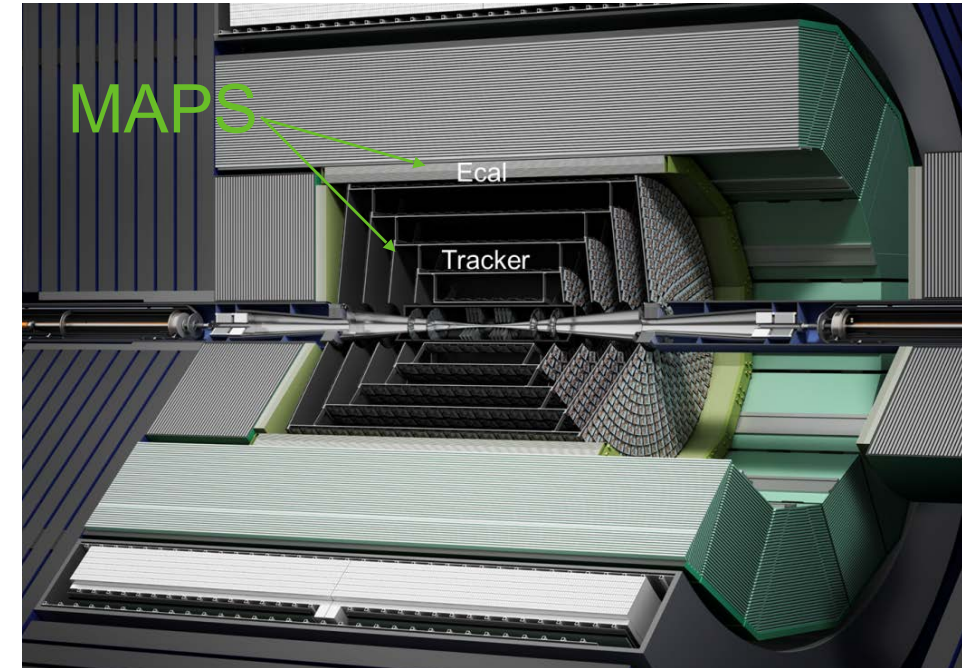
Large area MAPS for SiD tracker & ECal

Benefits of large-area MAPS:

- Standard CMOS foundry, low resistivity: **cost** ↓
- Sensing element and readout electronics on same die
 - In-pixel amplification: **noise** ↓, **power** ↓
 - No need for bump-bonding: **cost** ↓
- Area > 10x10 cm² → enable O(1) m² modules

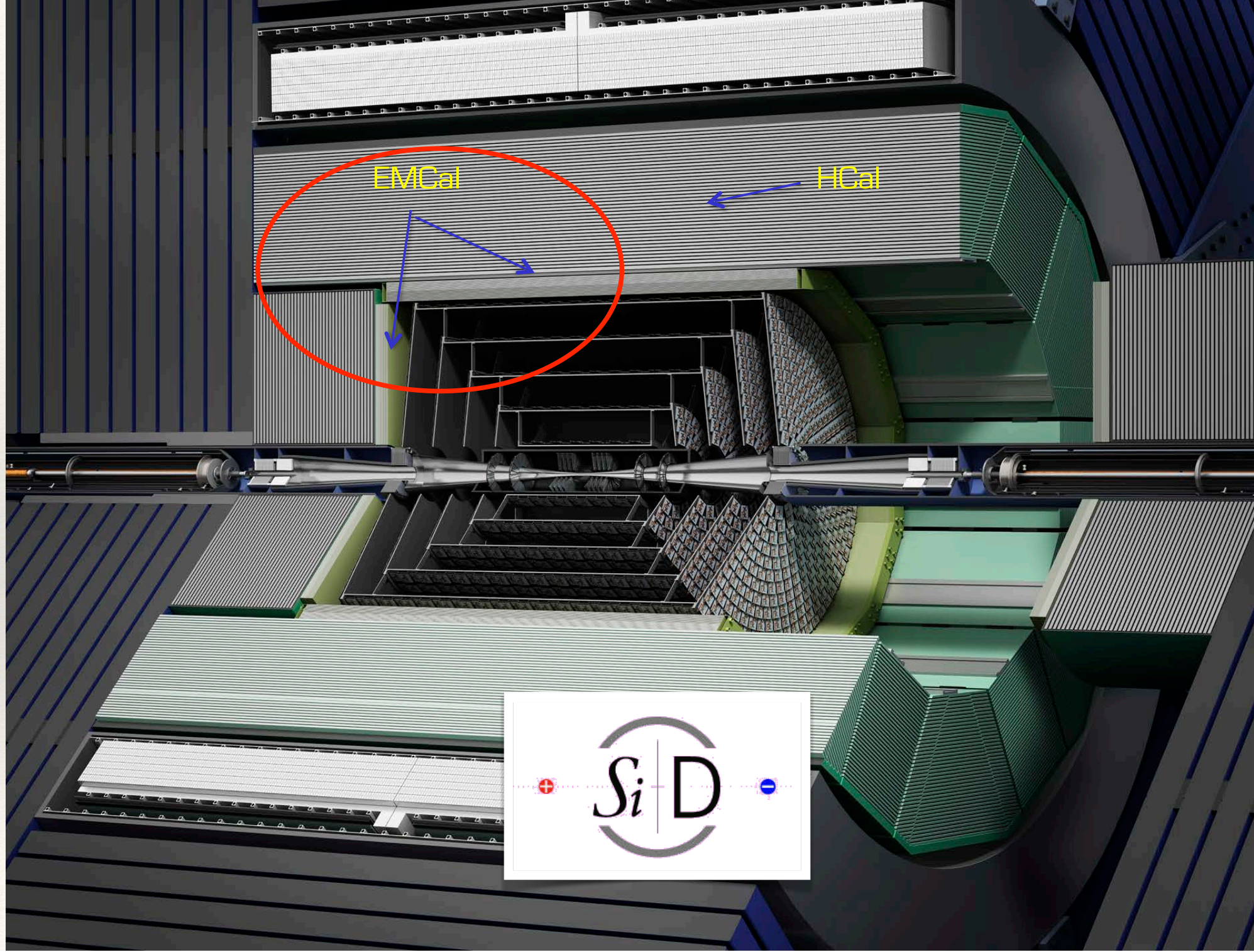
Several design challenges:

- Large on-die variations, mismatch
- Yield
- Stitching layout rules
- Distribution of power supply
- Distribution of global control signals/references



An example of the SiD Tracker and the ECal overall design

Goals of R&D: find solutions and explore novel design techniques



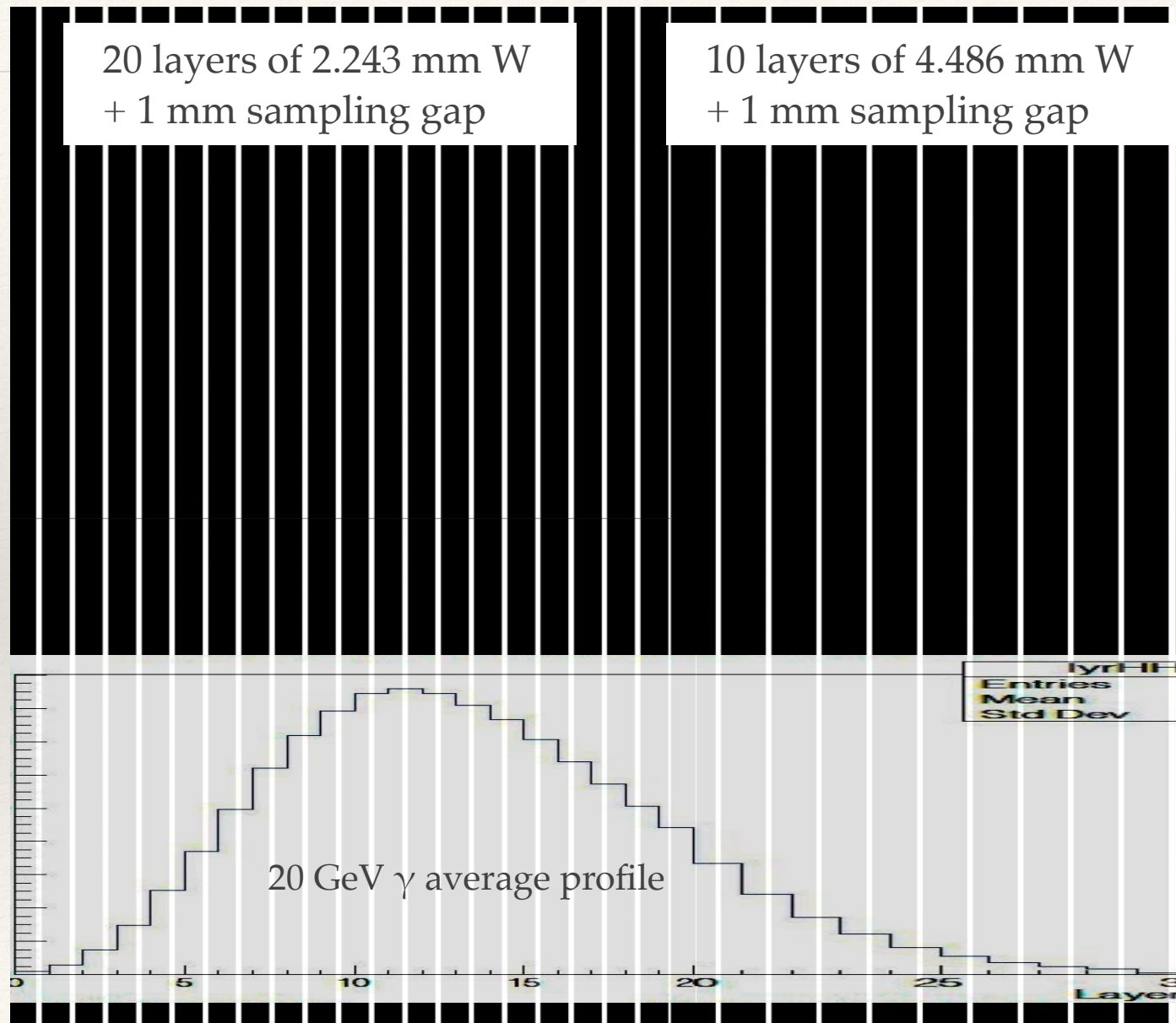


Model of longitudinal structure of SiD ECal

Total = $27 X_0$

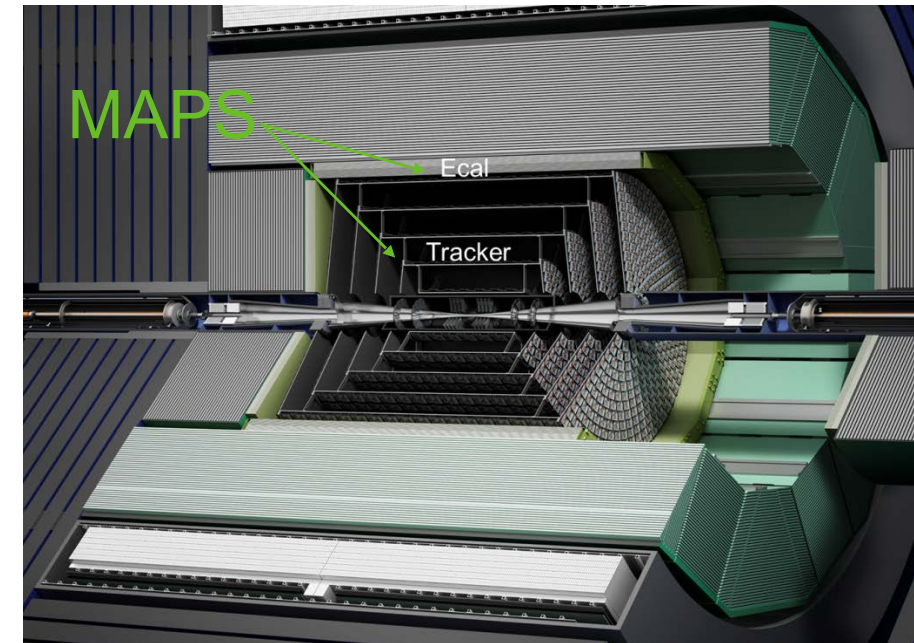


Minimize sampling gap to achieve optimal Moliere radius and shower separation



Main specifications for Large Area MAPS development

Parameter	Value	Notes
Min Threshold	140 e ⁻	0.25*MIP with 10 μm thick epi layer
Spatial resolution	7 μm	In bend plane, based on SiD tracker specs
Pixel size	25 x 100 μm ²	
Chip size	10 x 10 cm ²	Requires stitching on 4 sides
Chip thickness	300 μm	<200 μm for tracker. Could be 300 μm for EMCAL to improve yield.
Total Ionizing Dose	100 kRads	Total lifetime dose, not a concern
Hit density / train	1000 hits / cm ²	
Hits spatial distribution	Clusters	Due to jets
Balcony size	1 mm	Only on one side, where wire-bonding pads will be located.
Power density	20 mW / cm ²	Based on SiD tracker power consumption: 400W over 67m ²



SiD Tracker and the ECal

ILC time structure & operation phases

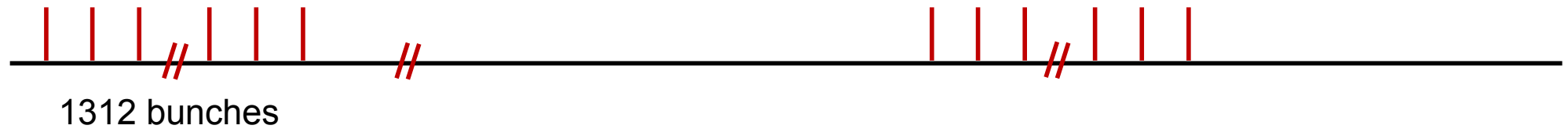
Phases:







Bunch repetition: 200 ms

Bunch train: 727 μ s

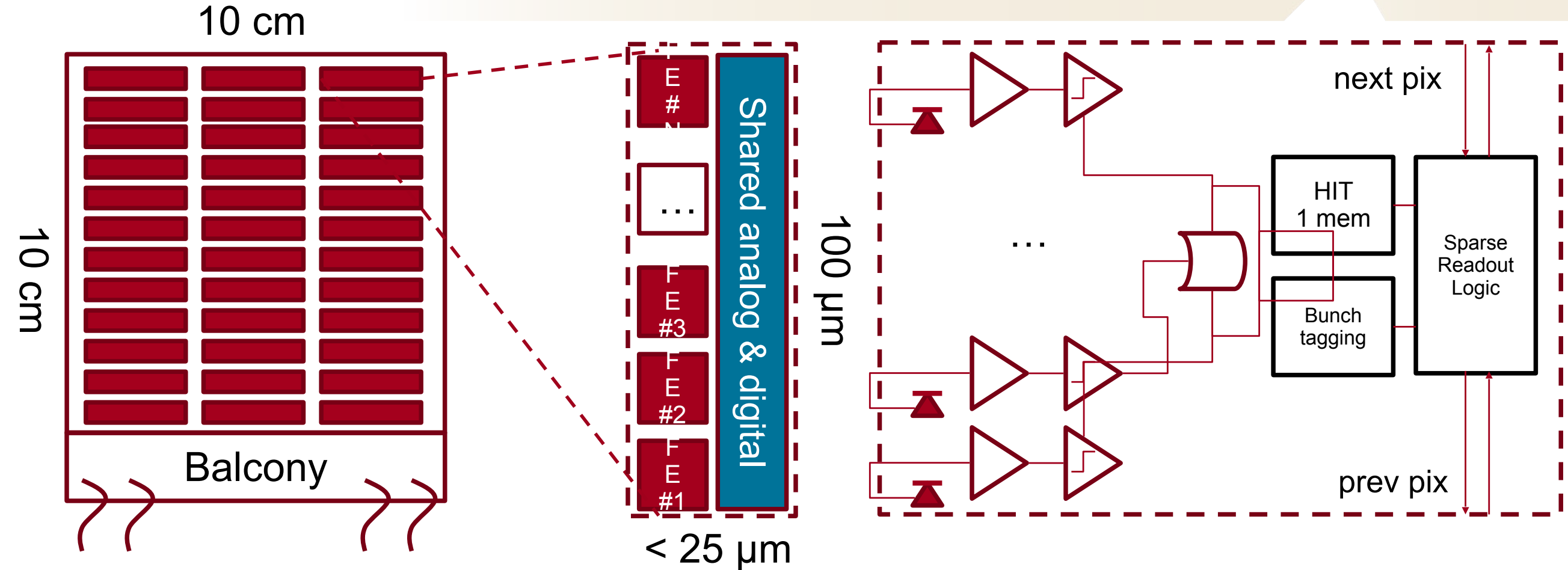
Bunch spacing: 554 ns



Description:

-  **Idle:** non vital resources kept in power saving mode
-  **Wake:** all resources get ready to run
-  **Integration:** analog processing in pixels active. No digital activity, balcony in power saving
-  **Readout:** zero-suppressed readout & data transmission. Matrix in power saving

Overall architecture



- Expected 1 hit/pixel/bunch train \rightarrow integrate charge through whole bunch train \rightarrow store 1 hit/pixel
- Segmentation of pixel front-end connected to common digital logic. See also *CLICTD* [1]
- Optimal segmentation of pixel front-ends will depend on sensor performance

L. Rota

[1] <https://cds.cern.ch/record/2643766/files/CLICdp-Conf-2018-008.pdf>

Power during integration phase

Phase:



- Avg power consumption reduced by power-cycling ... but **peak** current draw is not!
- Assuming $1\mu\text{A}/\text{pixel}$, current draw is $\sim 16\text{ A}$
- Resistance of metal lines not negligible over 10 cm \rightarrow significant voltage drop

Possible strategies:

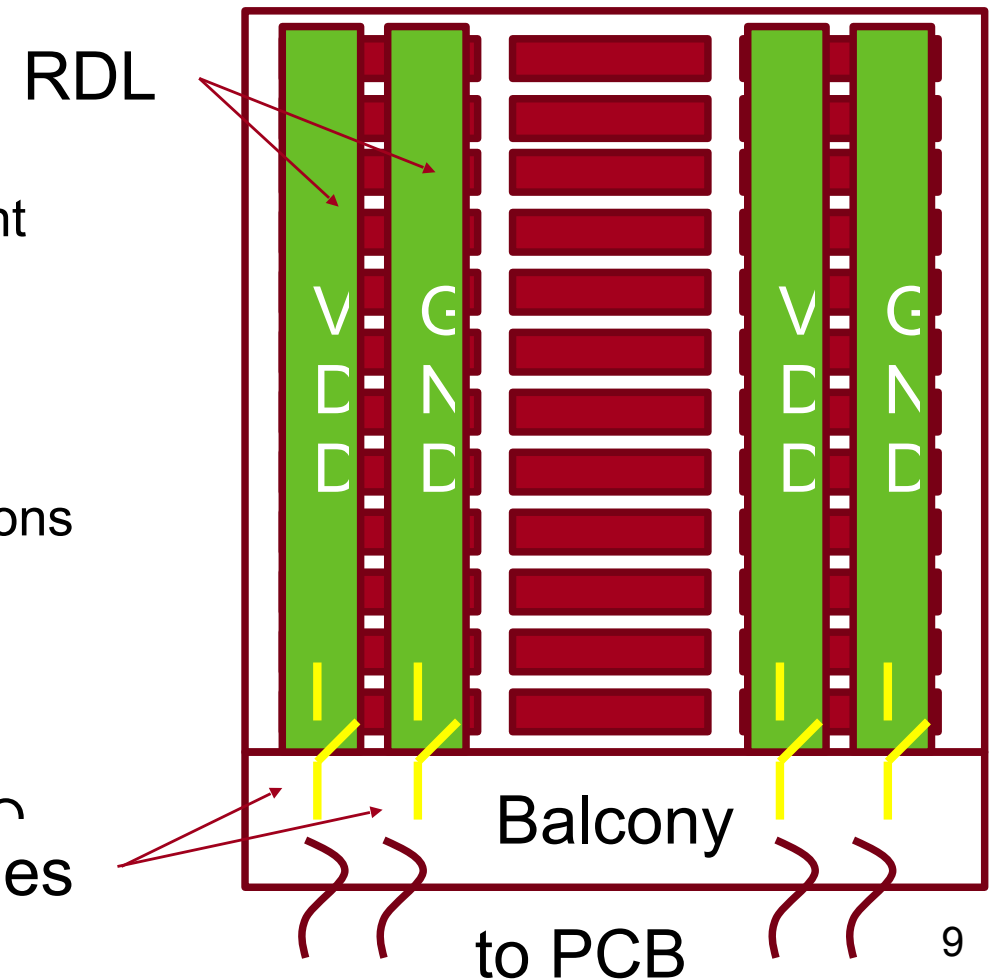
- Bypass caps distributed over sensor
- EMCal flat cable distributes power to all reticule bump connections
- Re-distribution layer with thick metal deposited on-top
- Discuss with foundry about having more/thicker metal layers

Need to investigate strategies on how to cope with shorts:

Add “switches” for each column/cluster \rightarrow if a short detected, DAC disables the column during initial power-up sequence

Switches

L. Rota



Power during readout phase

Phase:



Design an **asynchronous** readout logic with **zero-suppression**:

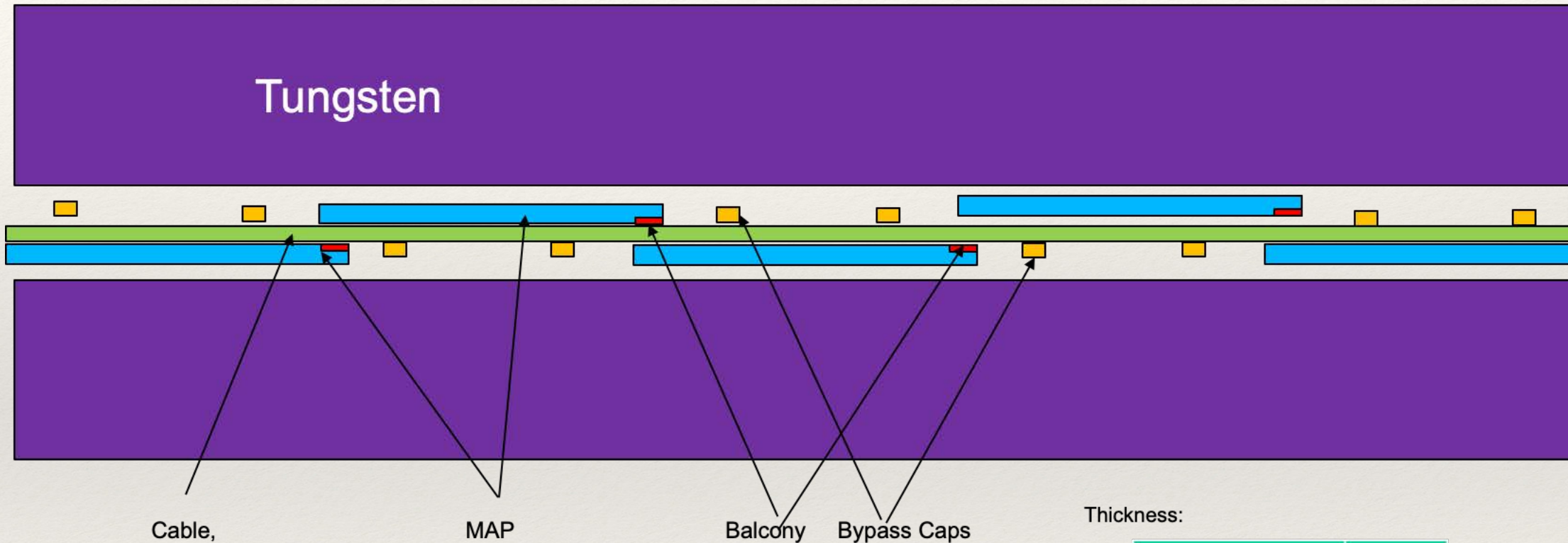
- Only pixels with HIT information are read-out by balcony
- Need to transmit data from pixel to balcony over ~10 cm lines, with large interconnection RC → minimize bit transitions → **power** ↓
- Remove clock → **power** ↓
- Handshaking between pixel and balcony ensures proper data transmission even with large on-die variations
- First simulations done, data throughput meets specs: ~200 ns to transmit one “hit” from pixel to balcony

Large area MAPS: next steps

- Join WP1.2 collaboration at CERN
- Design 1.5x1.5 mm² prototype with few pixels to test sensor + front-end
- Submission of first prototype in early 2022
- Study sensor performance on TowerJazz 65 nm process
 - TCAD simulations to optimize sensor design
 - Feedback from WP 1.2 measurements done at CERN
- Study bunch-tagging strategy
 - Analog-based: ramp, with low-res ADC in balcony (~8 bits)
 - Digital-based: local DLL for Time-to-Digital Conversion

Gap Structure with MAPS

Not to scale



ONE CABLE IN GAP DESIGN

Gap structure with MAPs on one cable (or pcb). Requires bump bonding

This may well need adjustment following more cable design

Thickness:

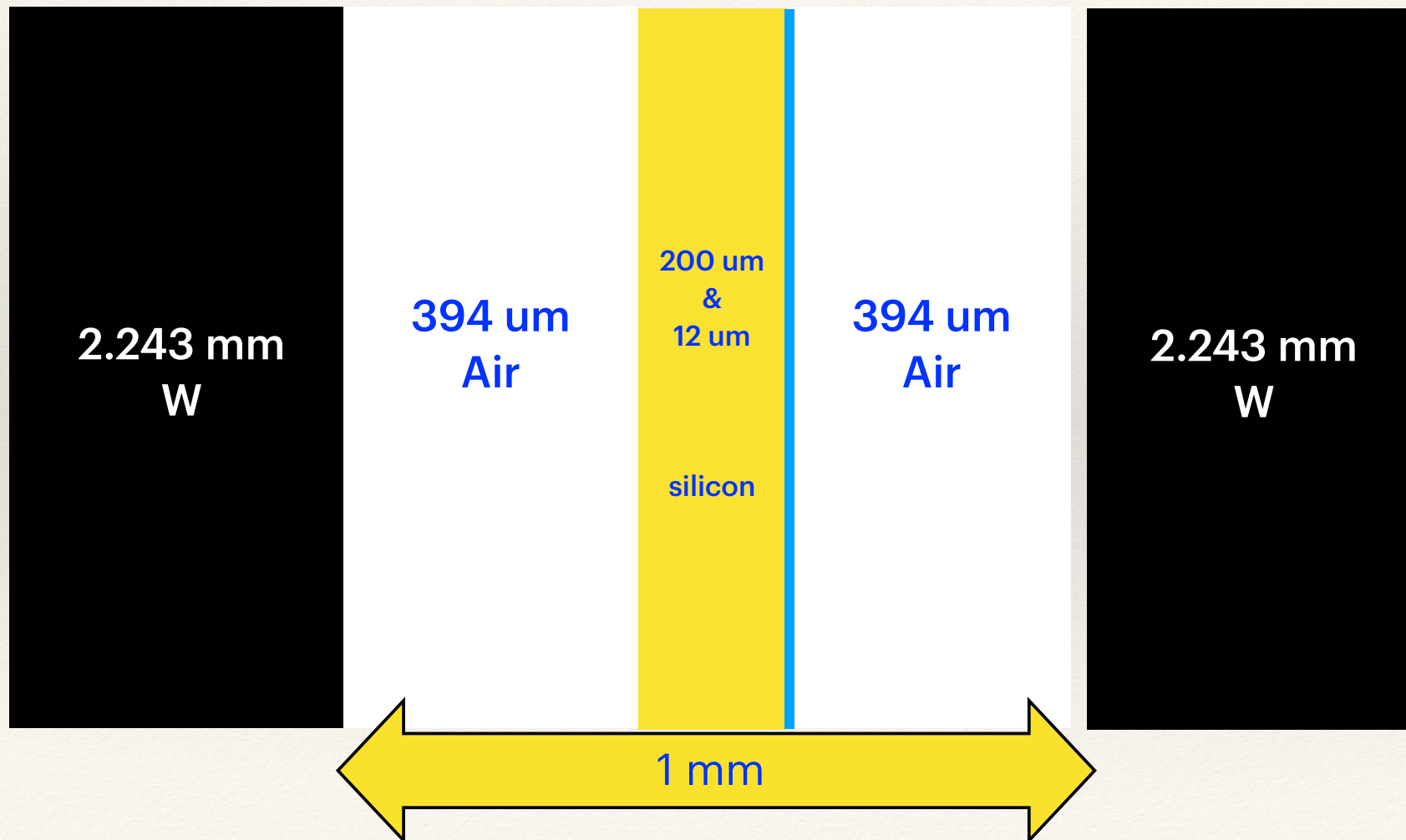
Middle Cable	400 μ
Top Sensor	200
Bottom Sensor	200
Bottom Cable	0
Total	800
Clearance with 1 mm gap	200

M. Breidenbach

Sampling Gap Simulation - SiD MAPS Digital ECal

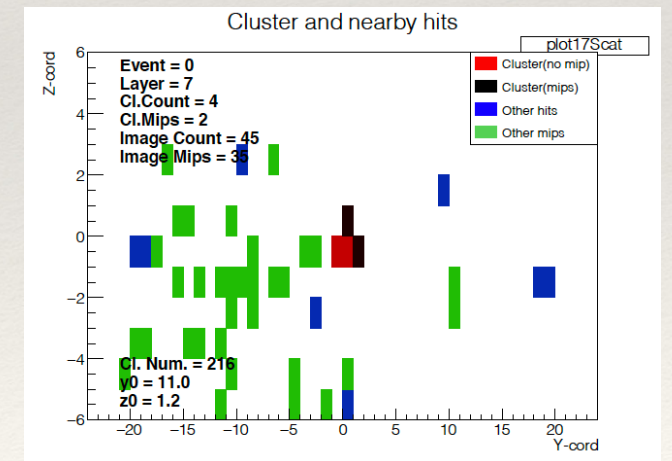
SiD Digital ECal based on Silicon MAPS J. Brau - 27 October 2021

Geant4 simulated silicon gap structures



Assumption:
Pixel threshold =
1 keV \approx 270 e's

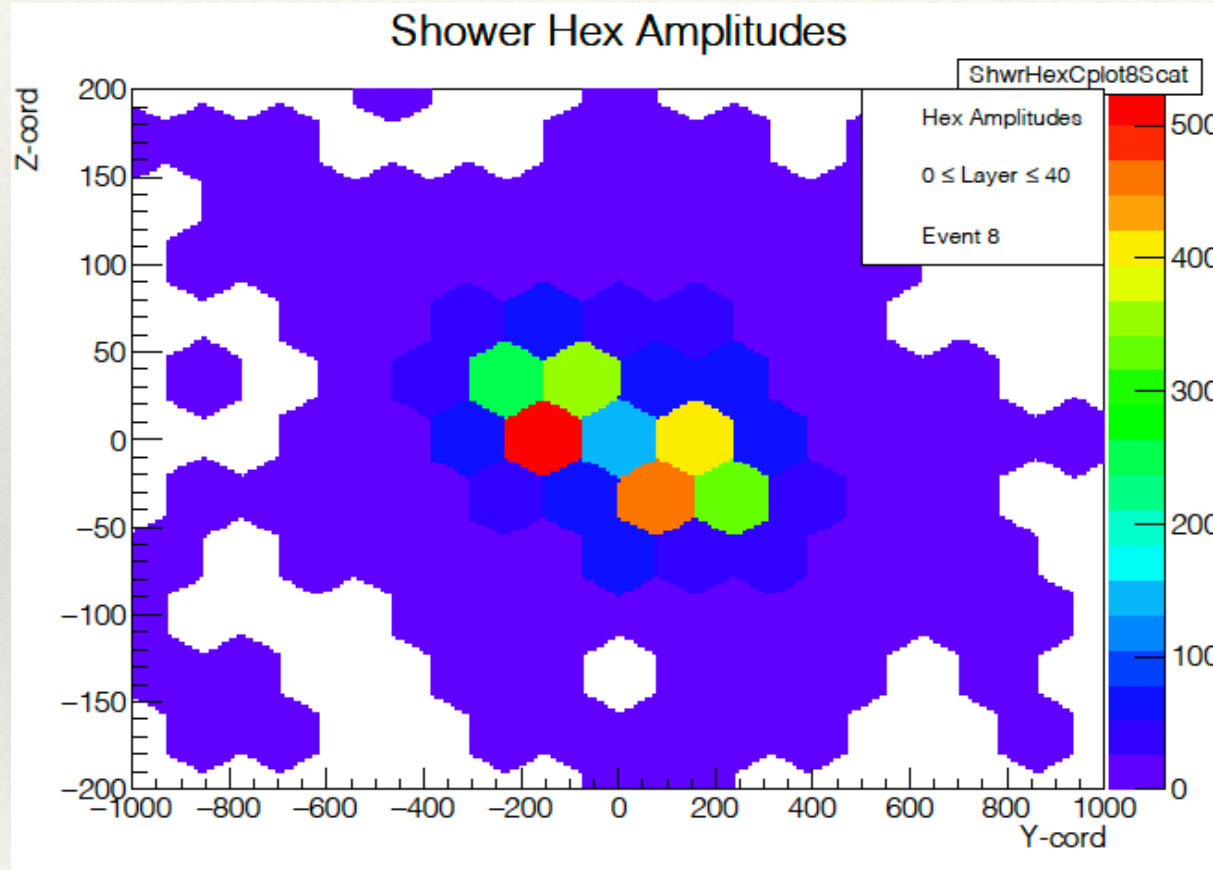
Future:
More detailed
gap model



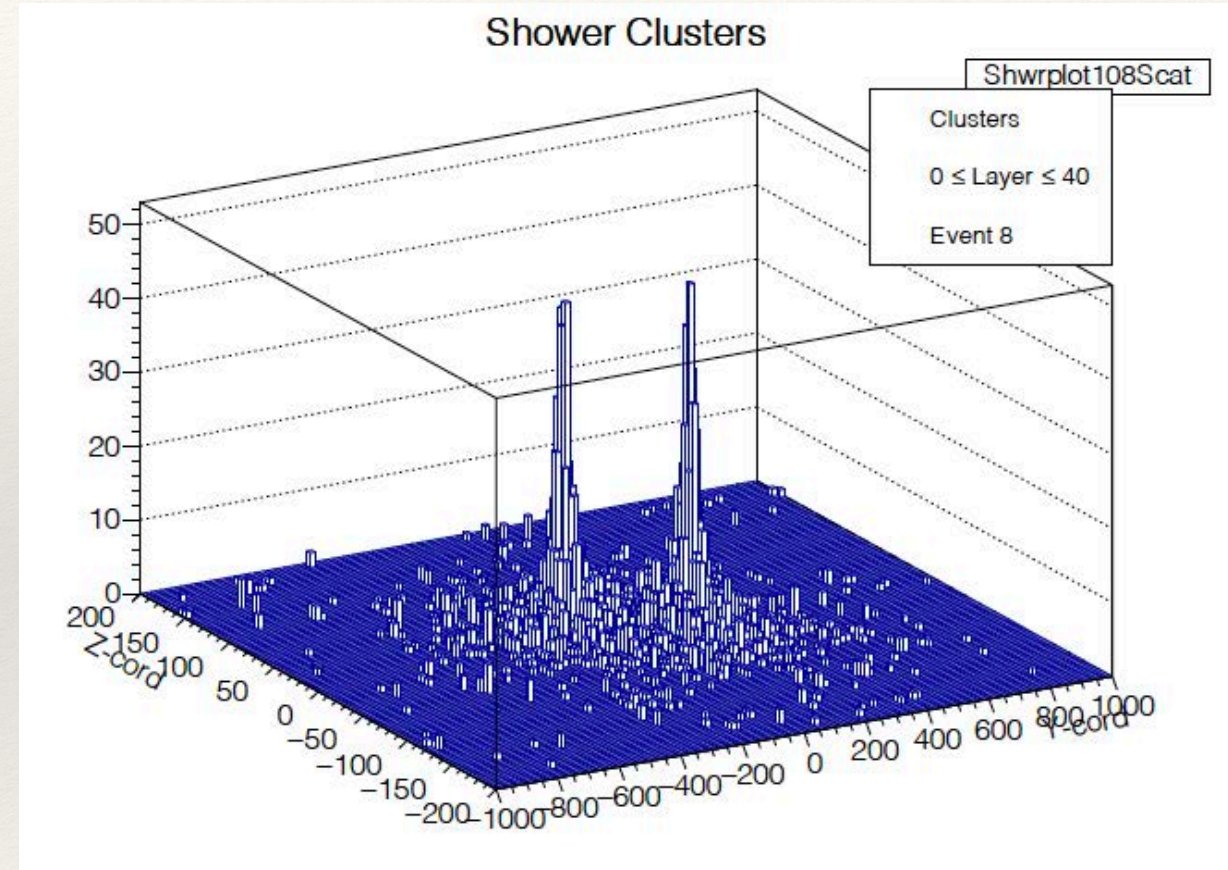
Typical hits distribution

Multi-shower of SiD MAPS compared to SiD TDR

40 GeV $\pi^0 \rightarrow$ two 20 GeV γ 's

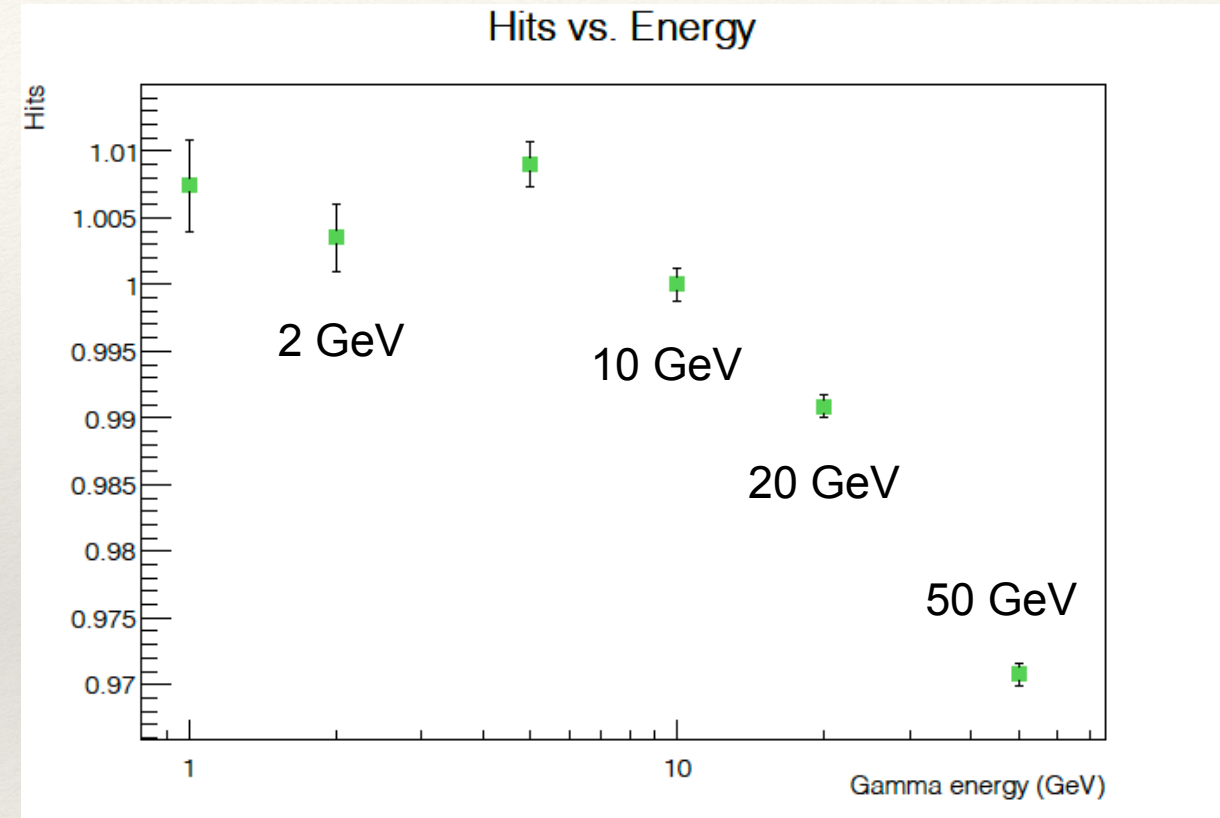
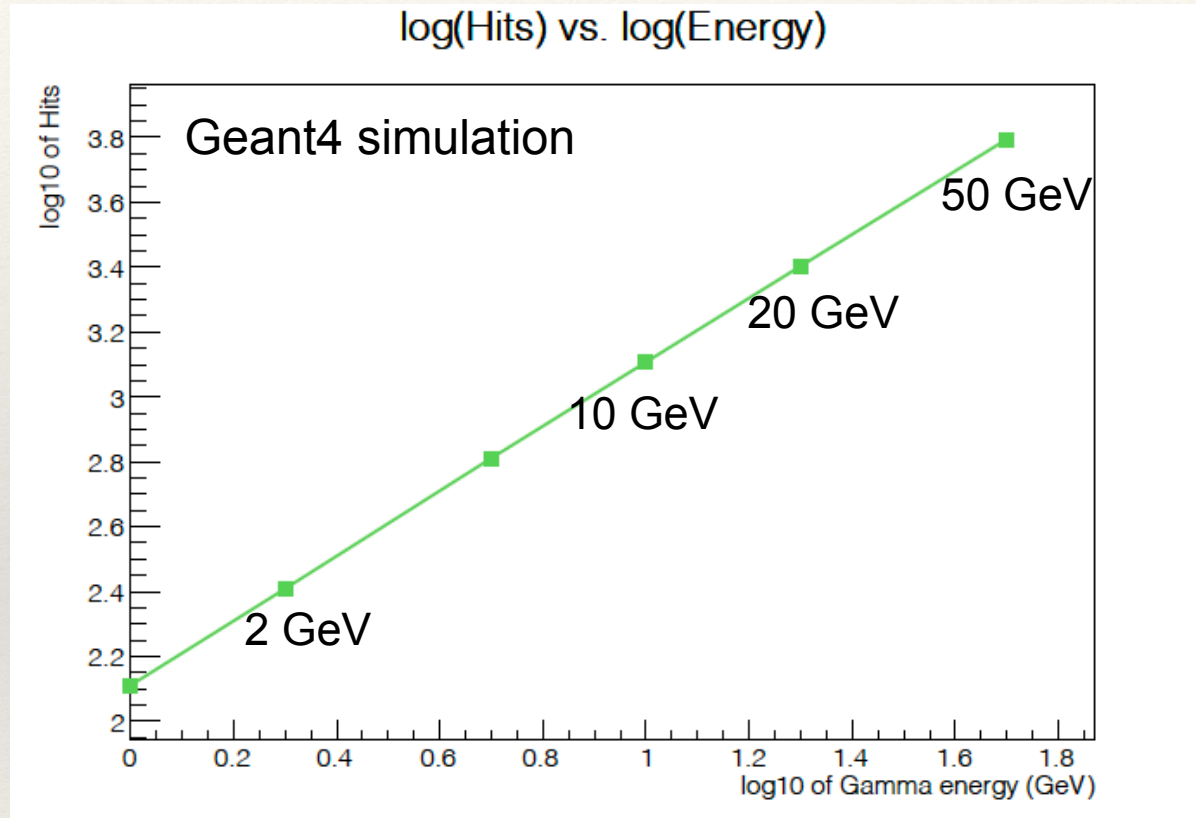


SiD TDR hexagonal sensors
13 mm² pixels



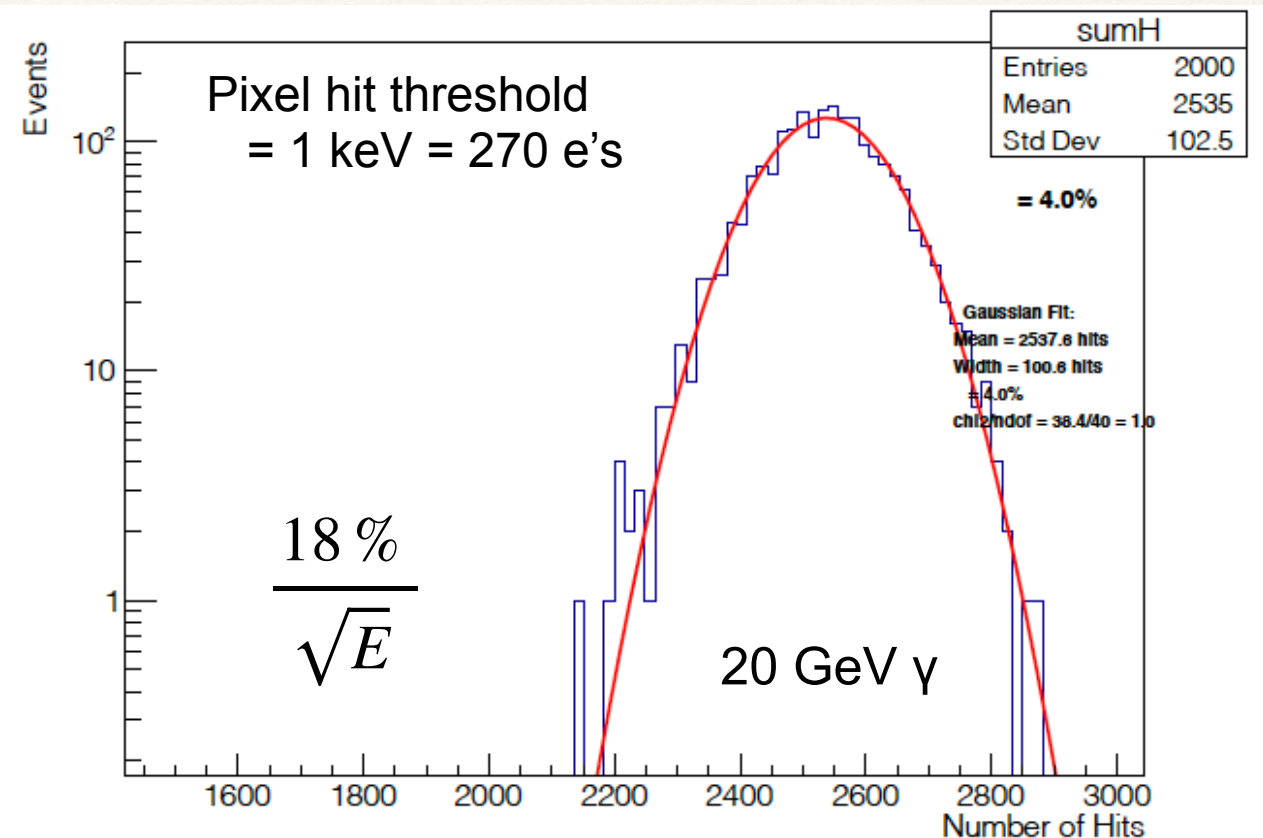
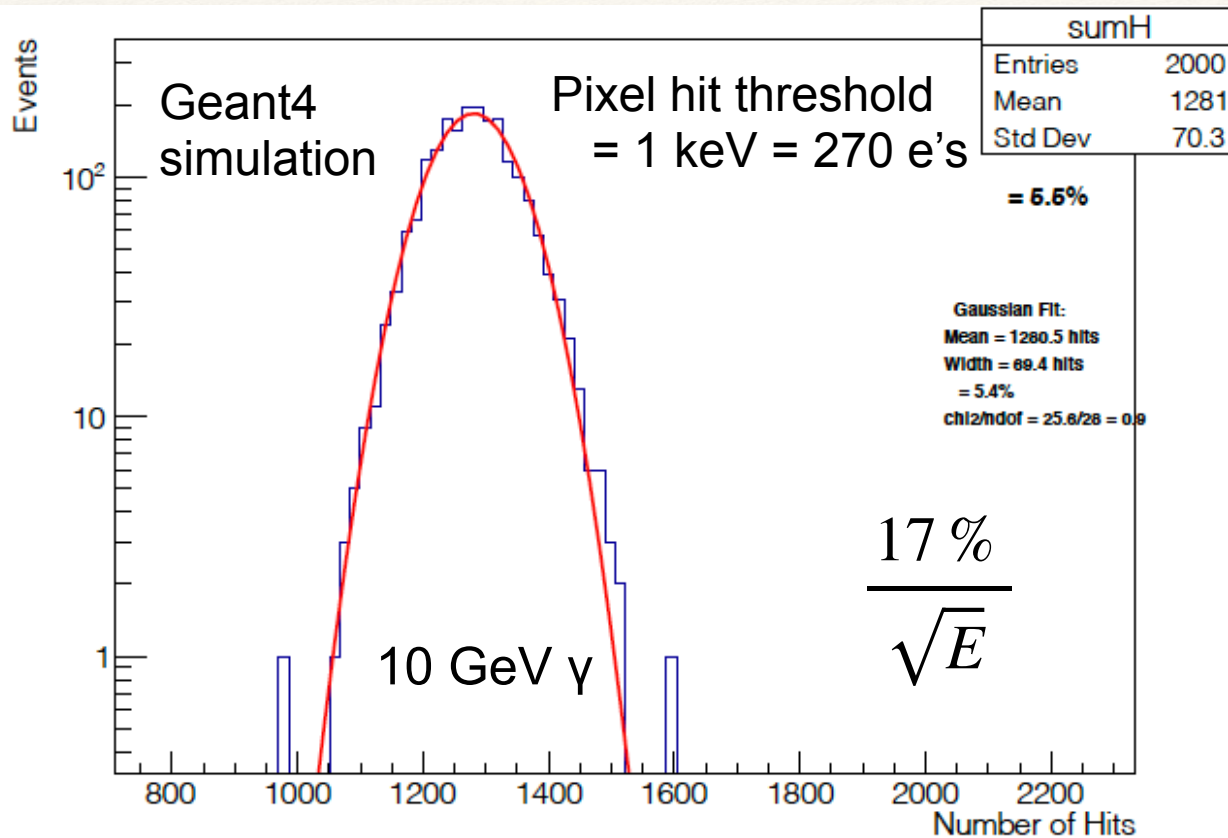
New SiD fine pixel sensors
25 μm x 100 μm pixels

Linearity of response (counting hits in γ showers)



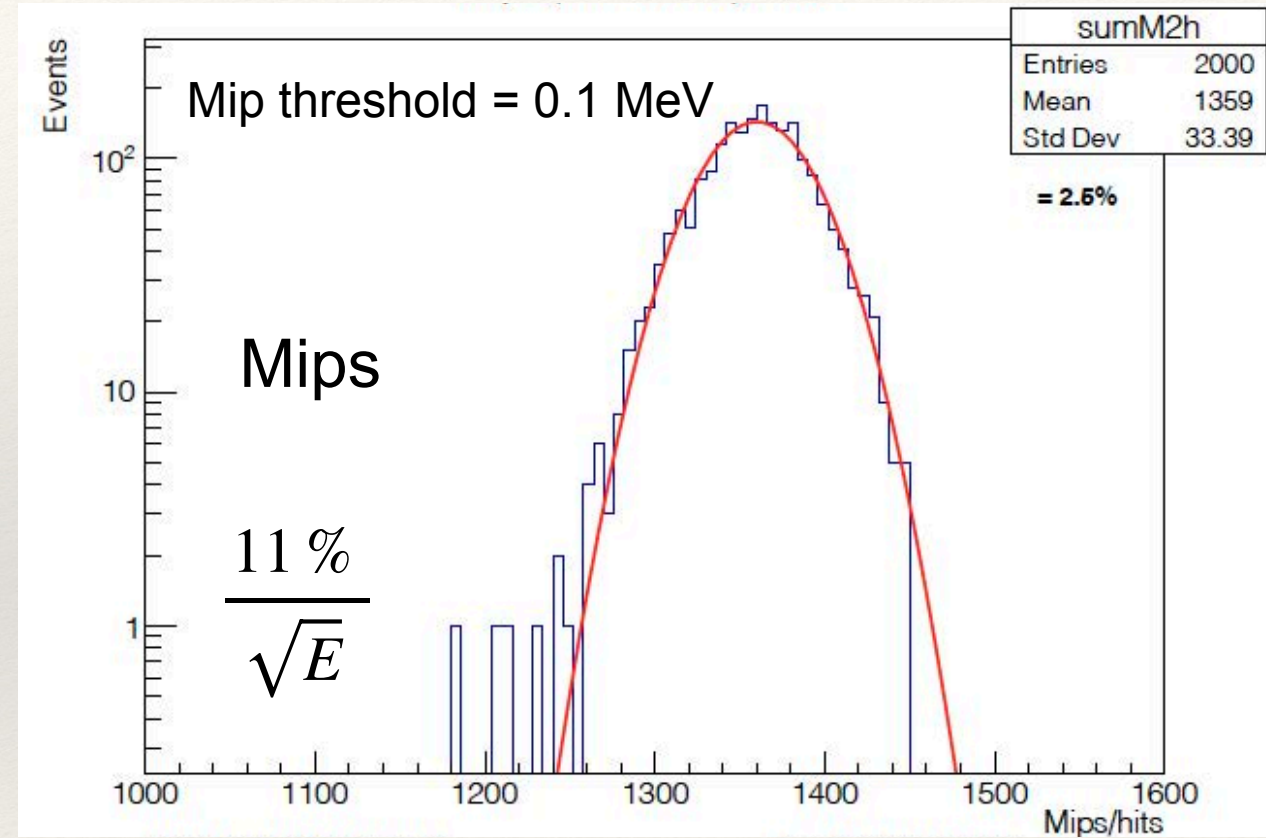
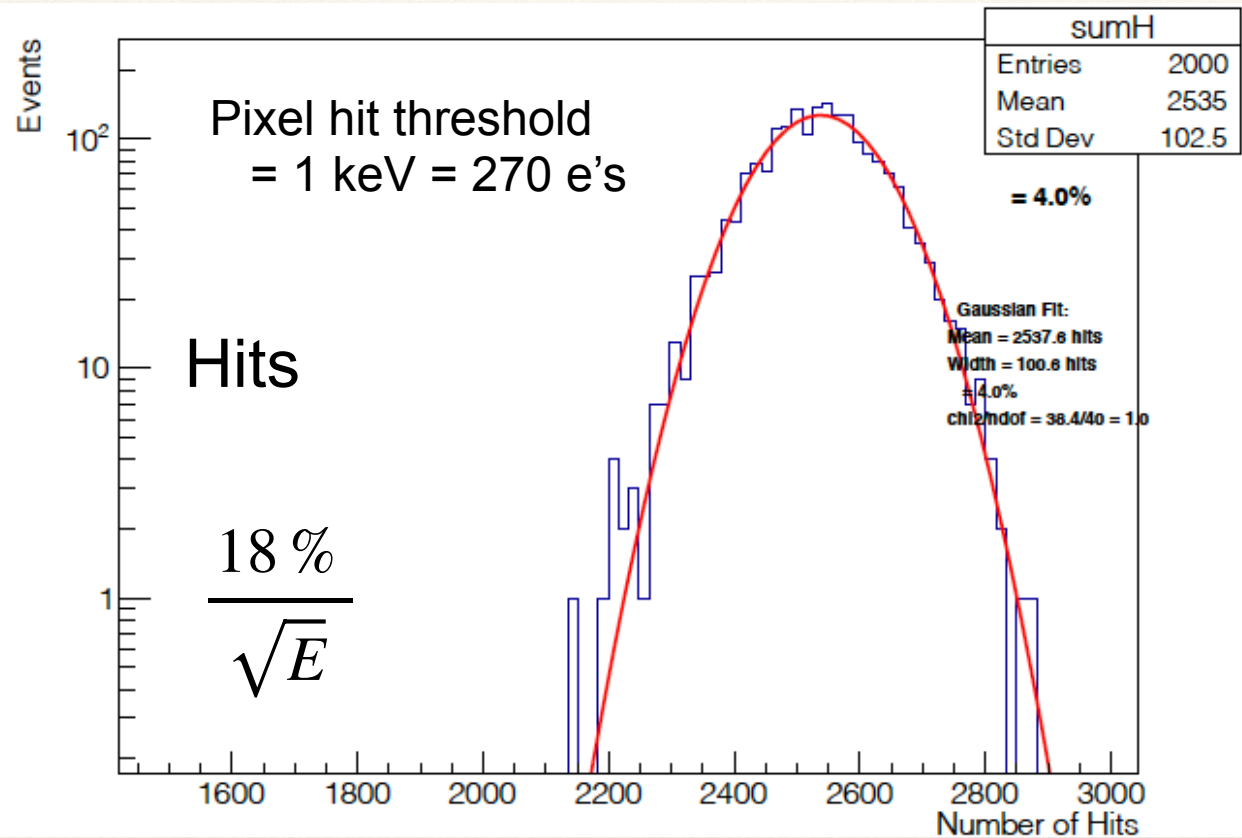
Non-linearity due to differing response and counting in thin ($0.7 X_0$) and thick ($1.4 X_0$) layers (and uncorrected leakage).

Hits resolution



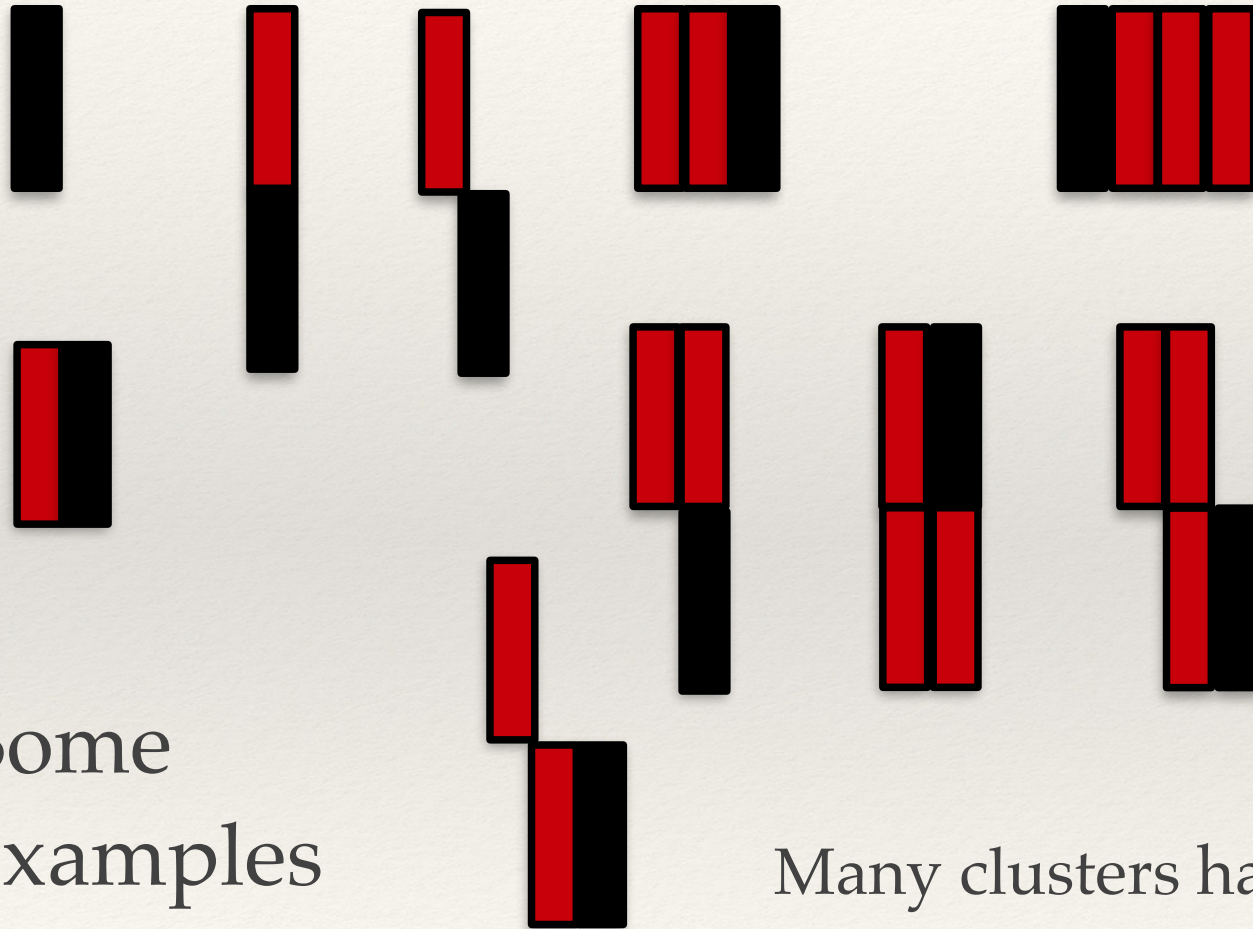
ILC TDR anticipates $\frac{17\%}{\sqrt{E}} \oplus 1\%$ for the SiD SiW ECal; **but we can do better.**

Pixel counts (hits & mips) - 20 GeV γ



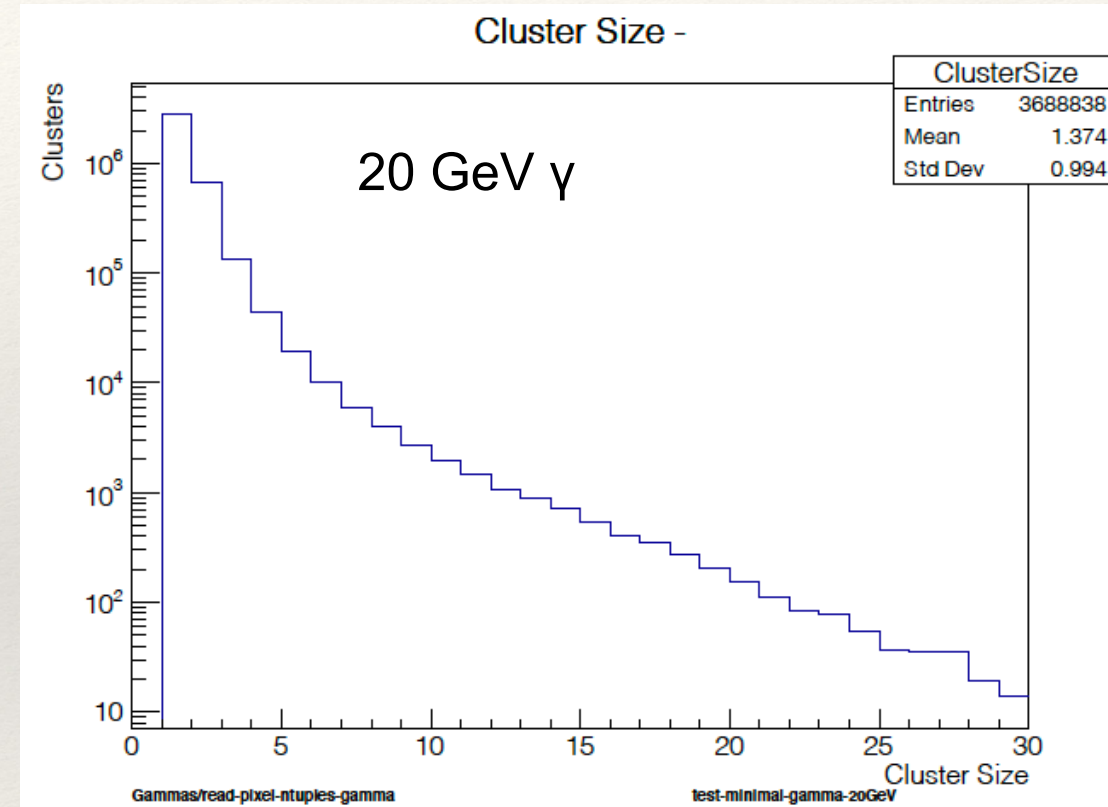
Ultimate goal is to count mips based on hit distribution.
 Potential to improve resolution compared to hit count.

Hits appear in clusters (size 1, 2, 3,...)



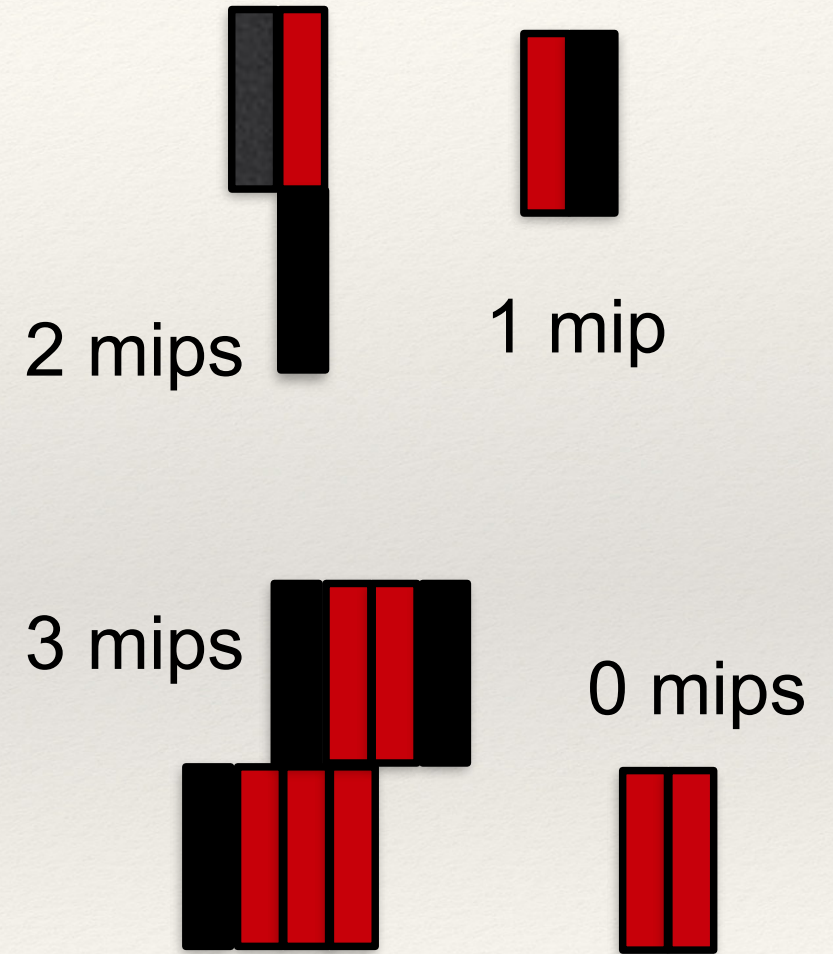
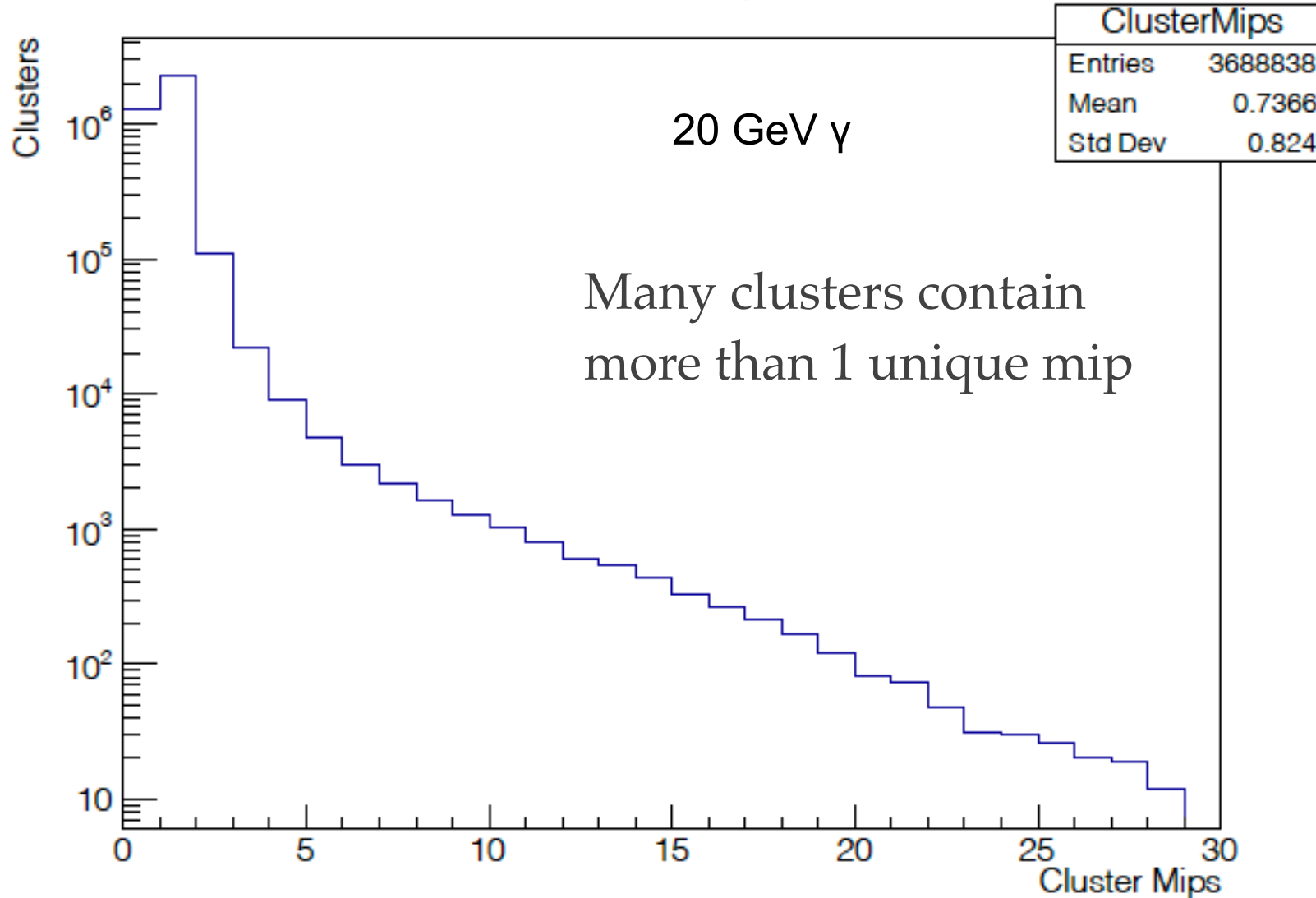
Some examples

Many clusters have 1 mip
(black - first appearance of mip)

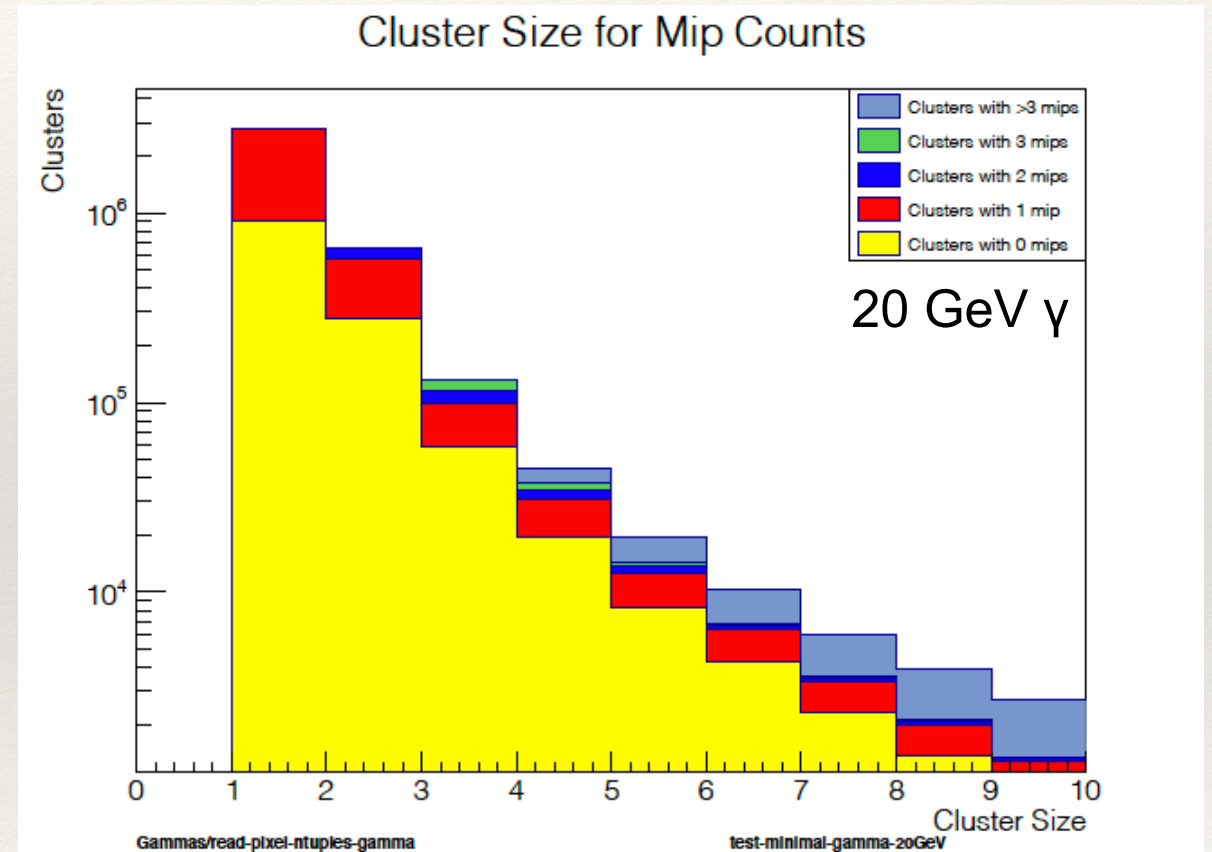
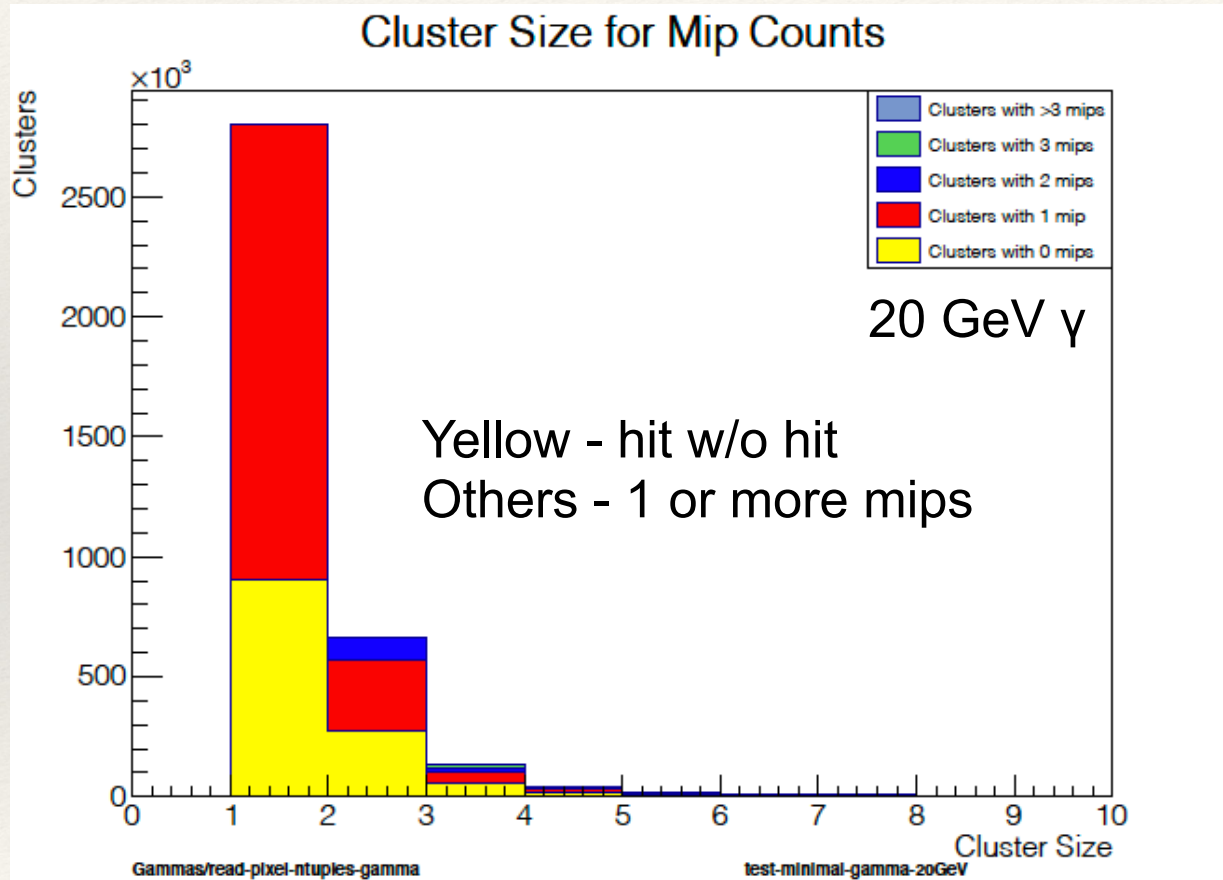


Mips per cluster

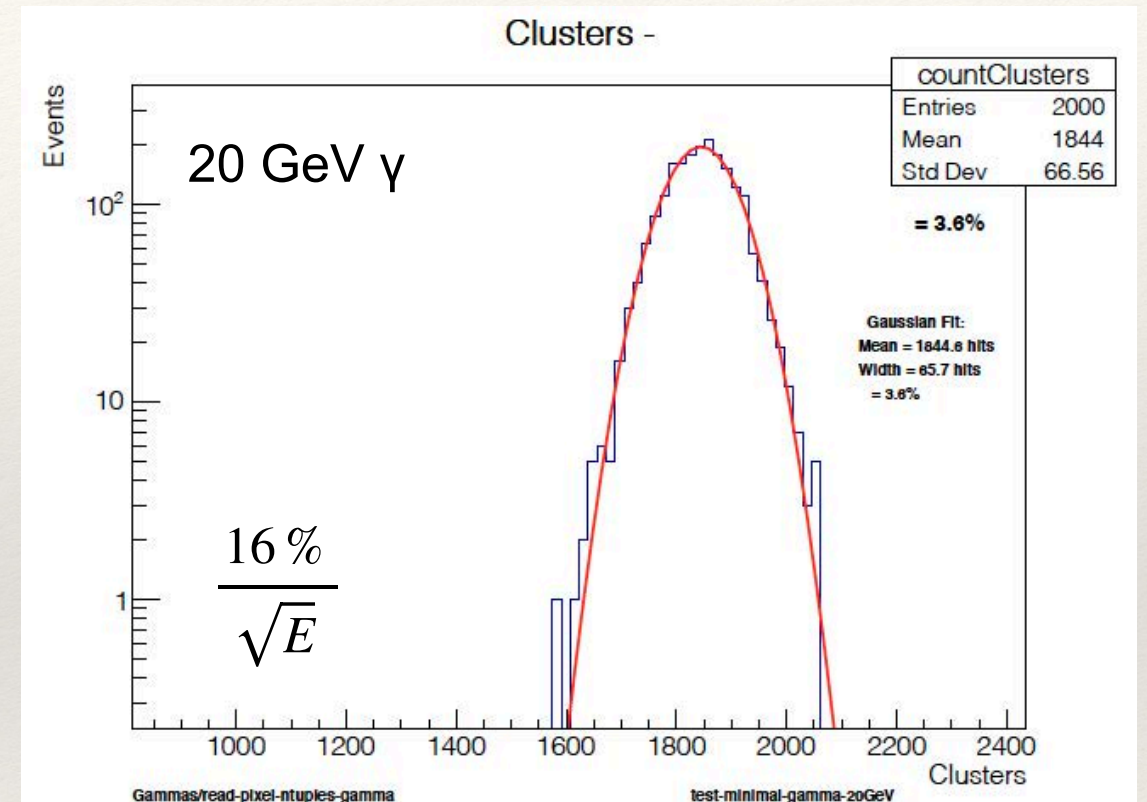
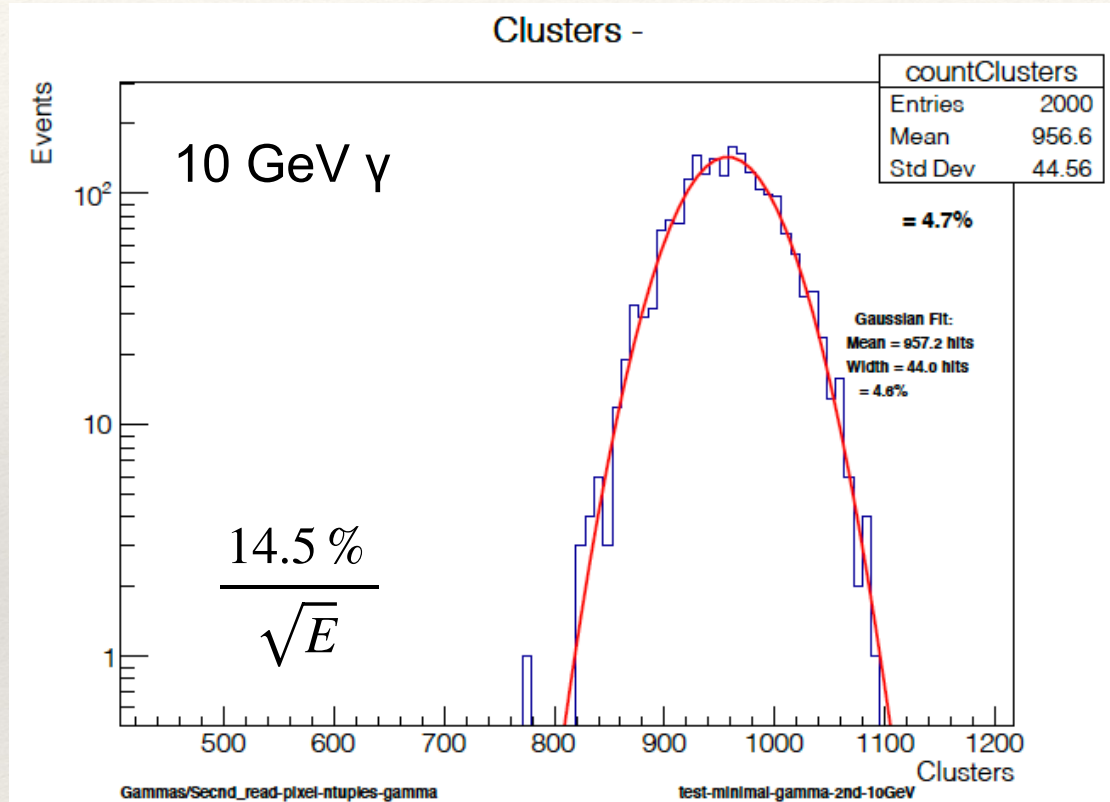
Cluster Mips -



Cluster summary (20 GeV γ)



Energy resolution from counting clusters



Improved compared to hit resolutions:

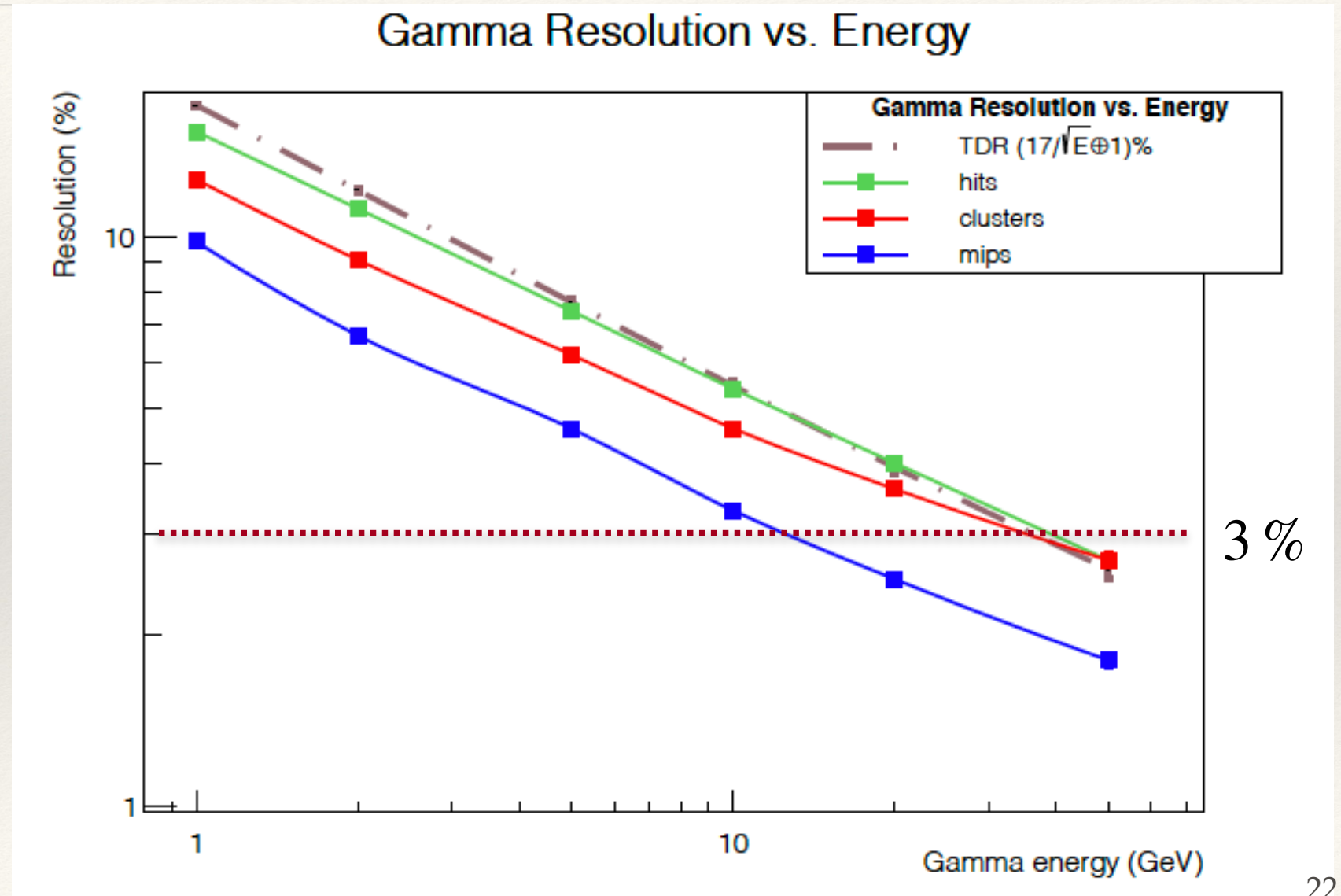
$$\frac{17\%}{\sqrt{E}} \text{ (10 GeV)}$$

$$\frac{18\%}{\sqrt{E}} \text{ (20 GeV)}$$

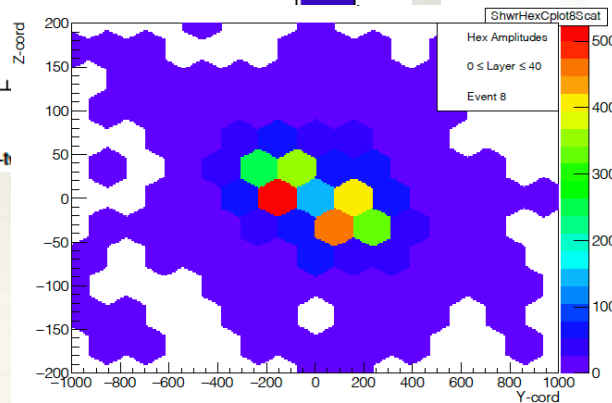
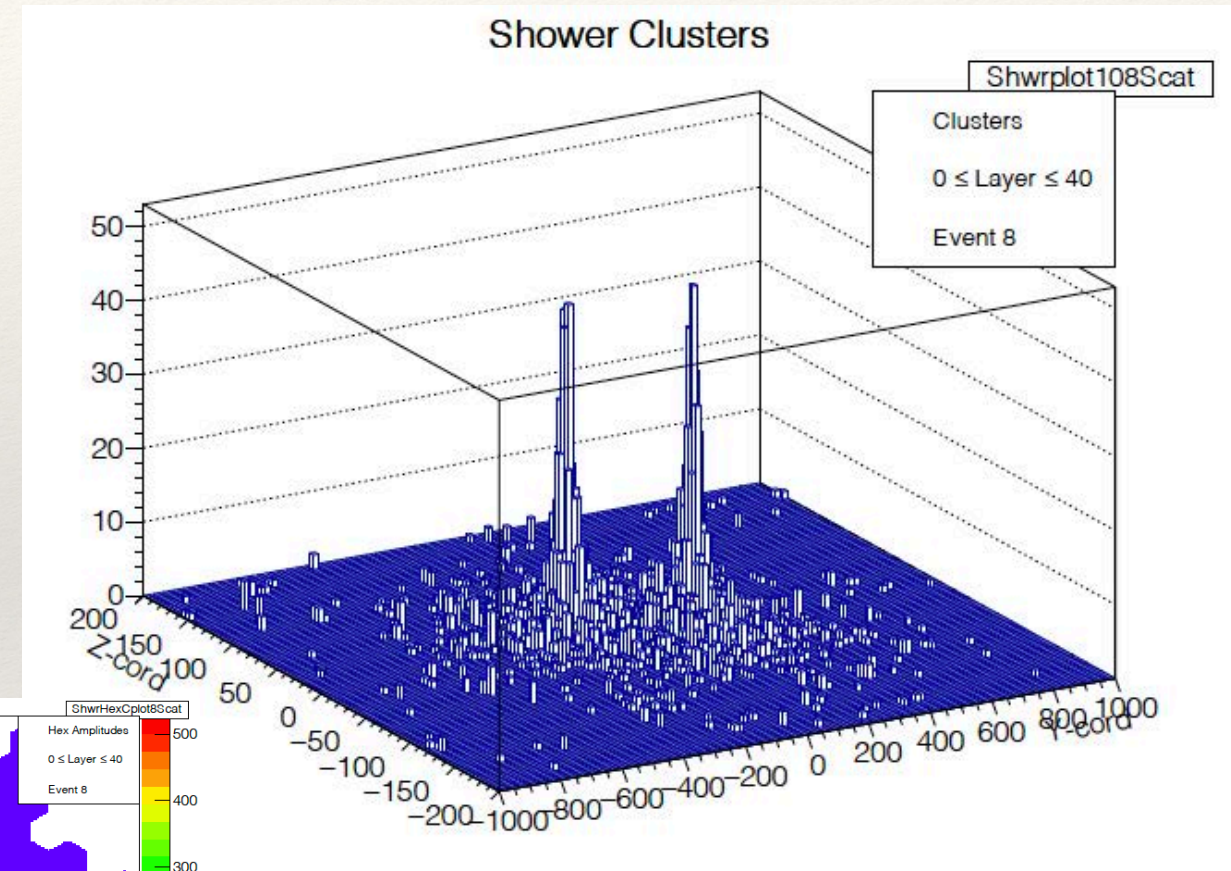
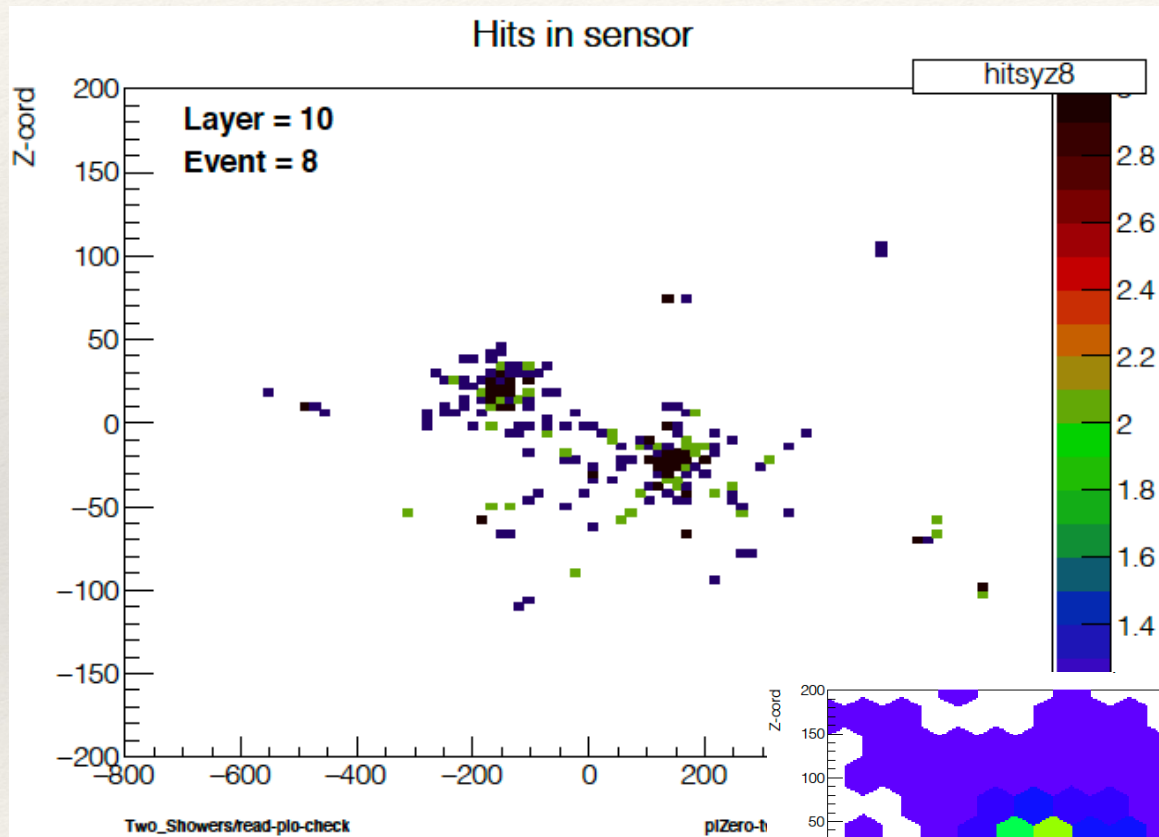
Resolution vs. Energy (hits/clusters/mips)

Cluster performance is simple cluster counting.

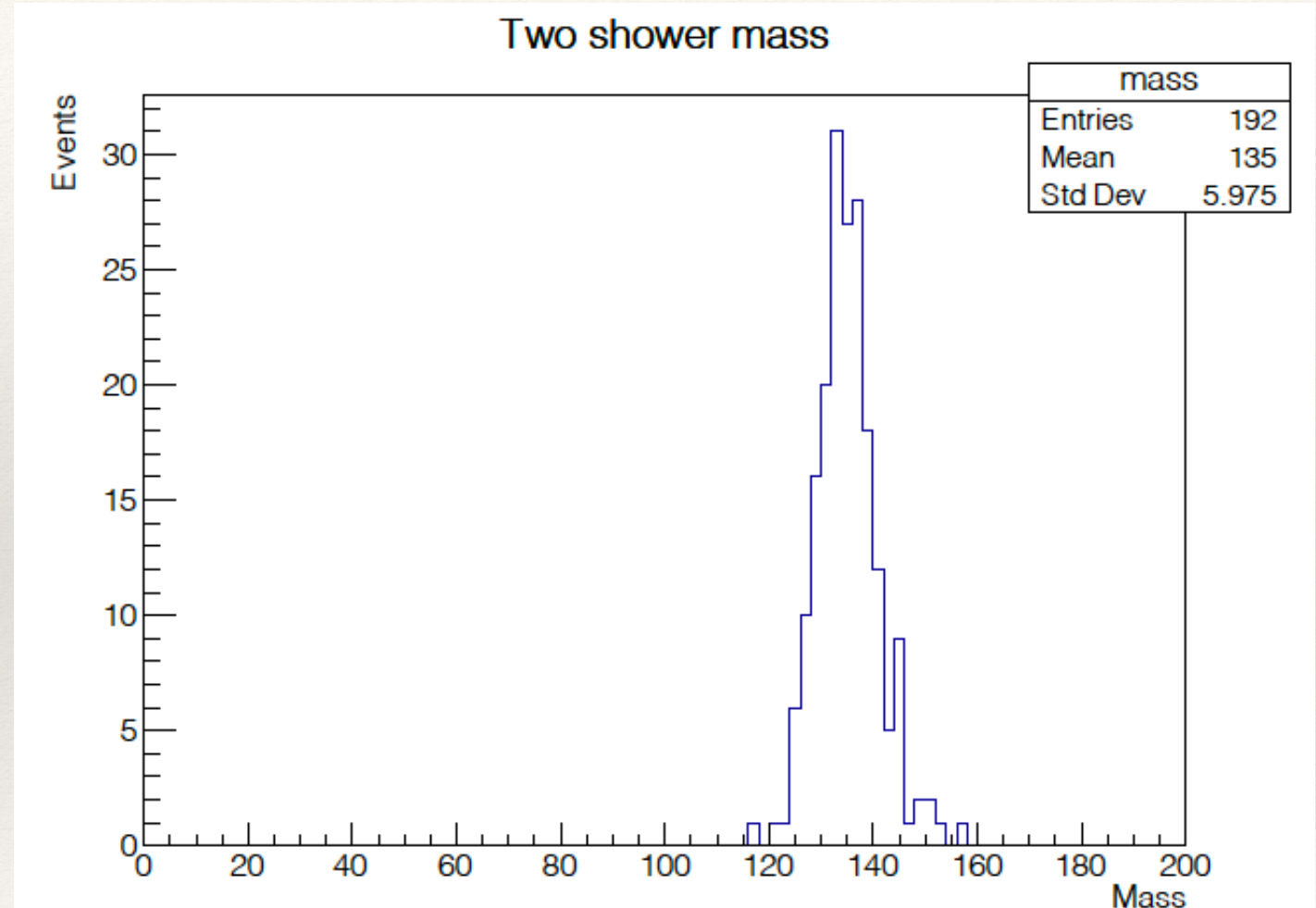
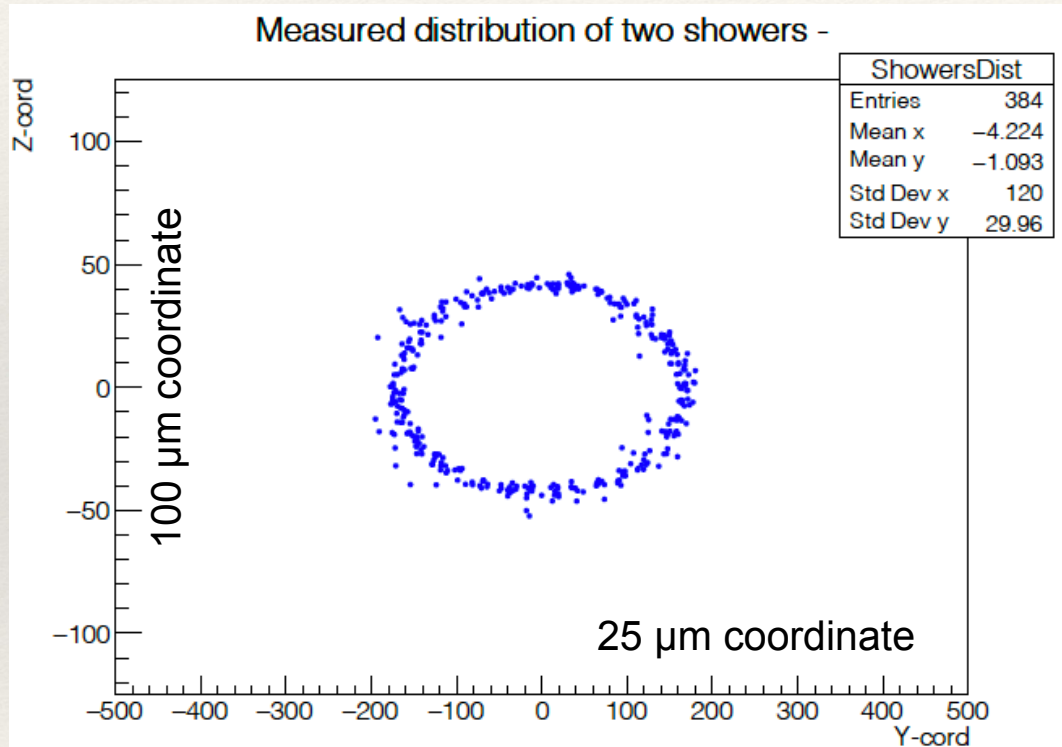
When cluster properties are taken into account the performance will improve, based on preliminary studies.



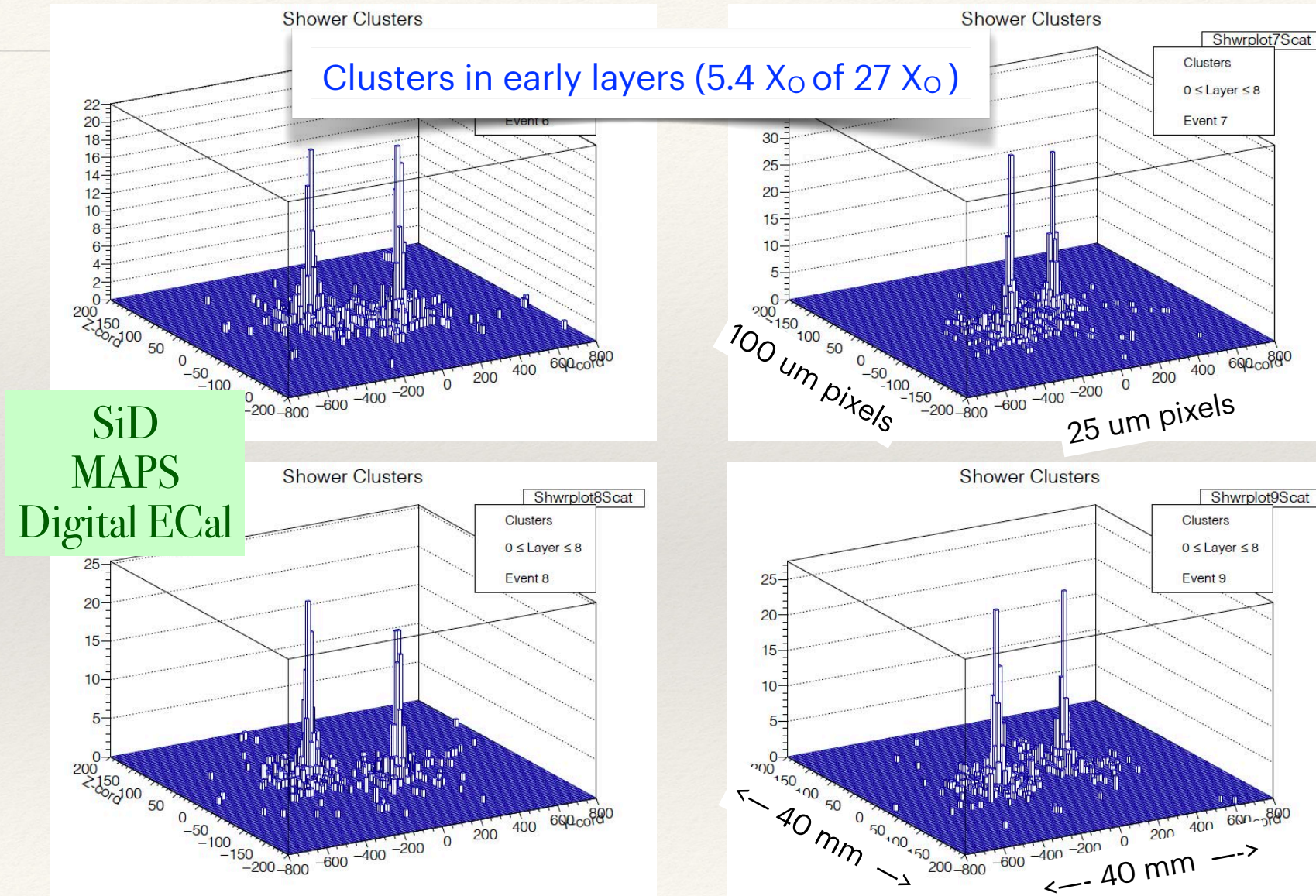
40 GeV $\pi^0 \rightarrow$ two 20 GeV gammas



40 GeV π^0 reconstruction



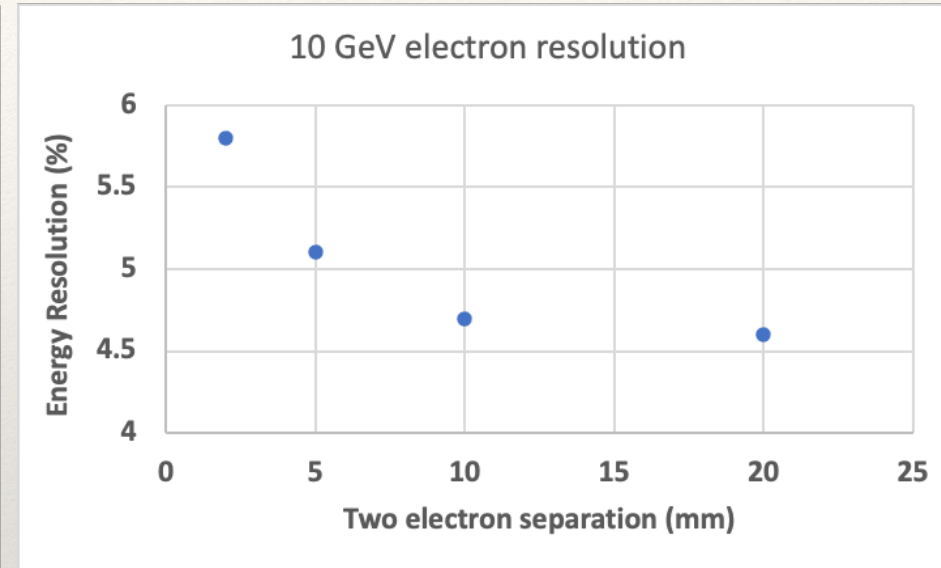
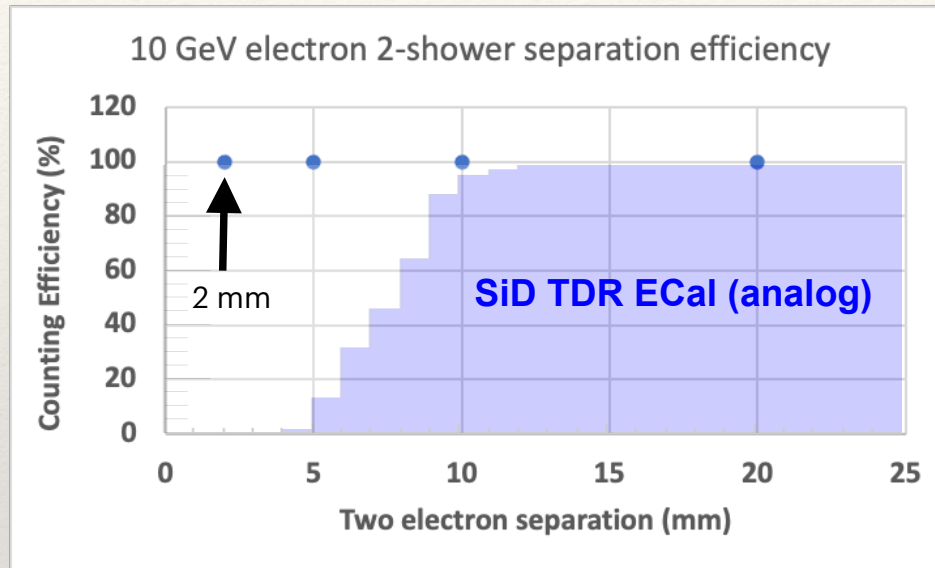
Two 10 GeV electron showers - 1 cm separation





Performance summary

Two nearby 10 GeV electrons in SiD MAPS ECal

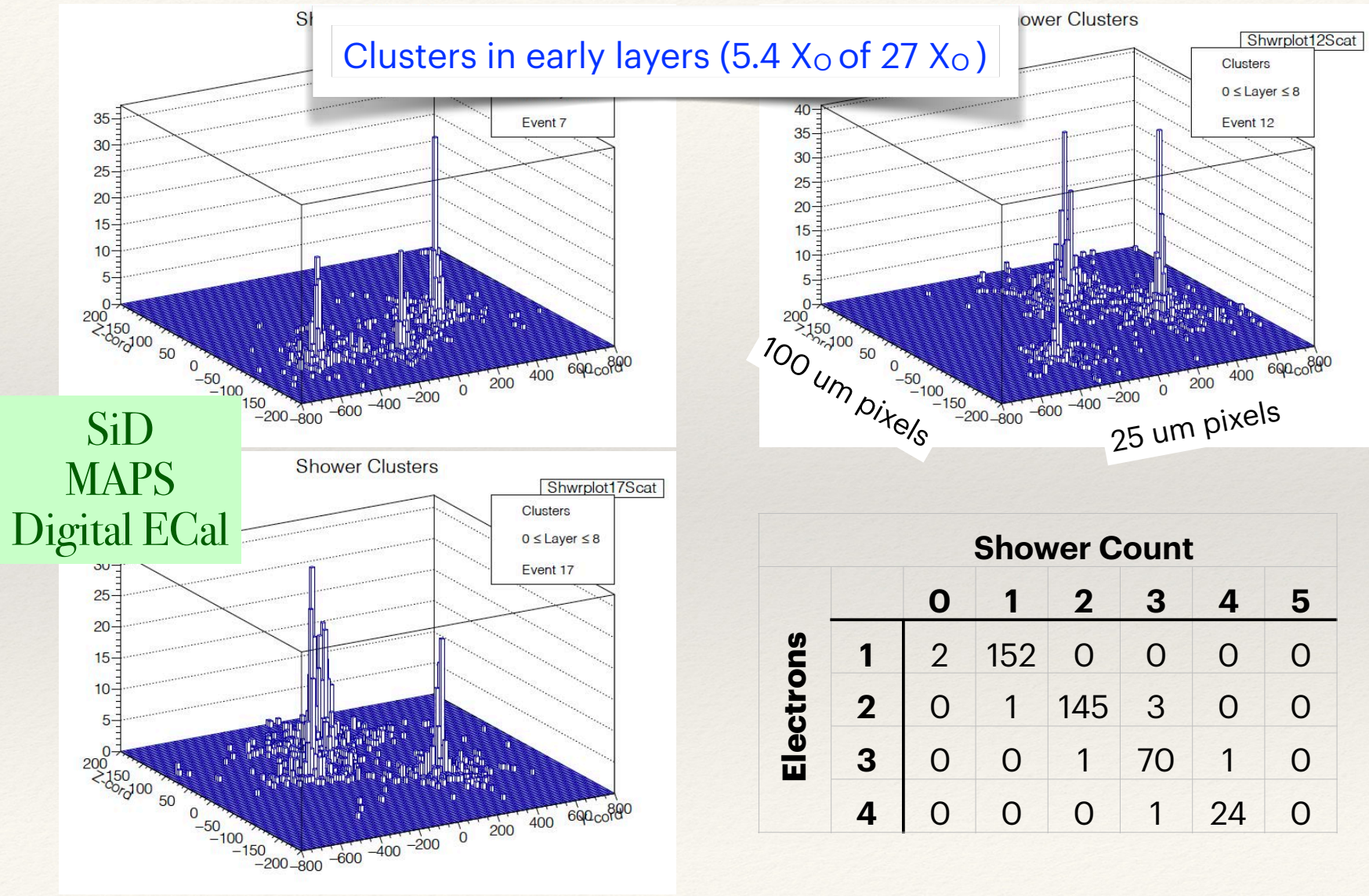


- ❖ Excellent performance!
- ❖ Note - very little optimization so far



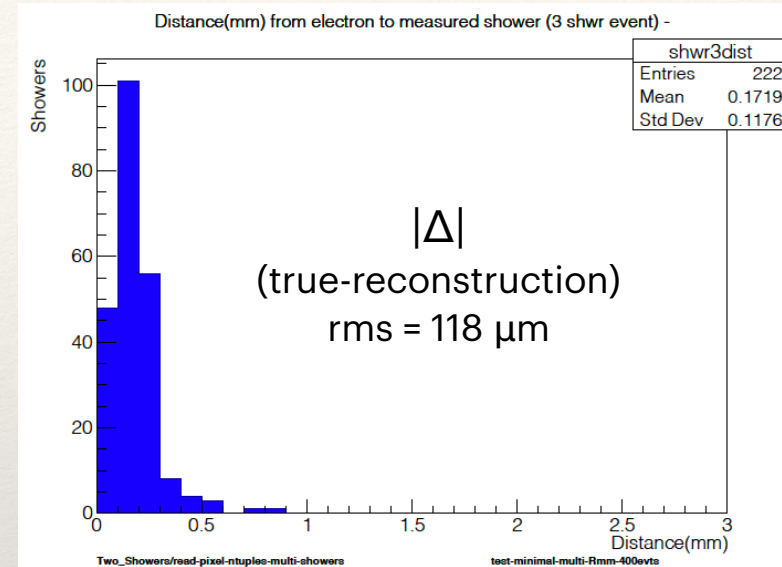
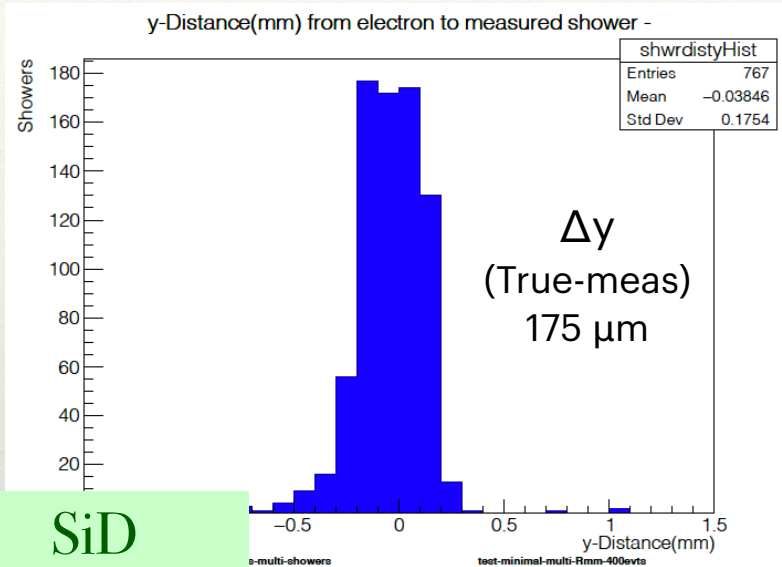
Counting showers: random number of electrons

Spatial distribution rms = 8 mm

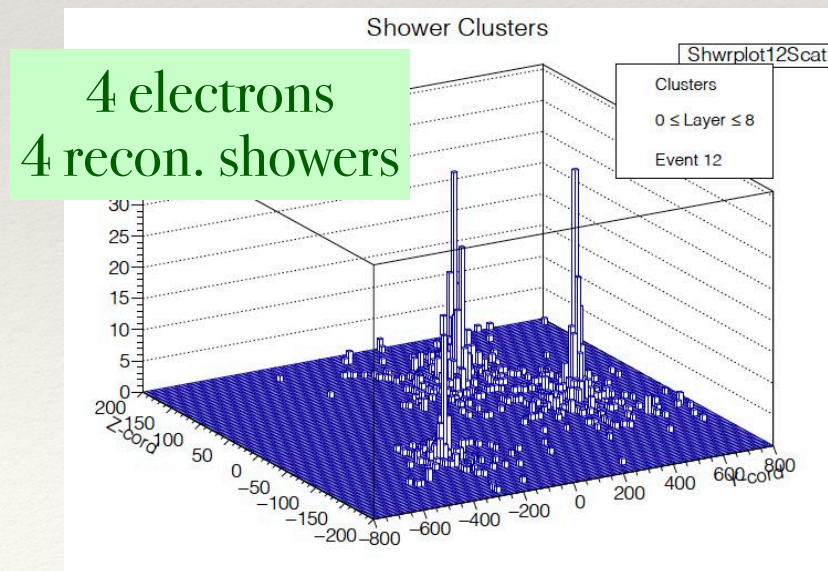
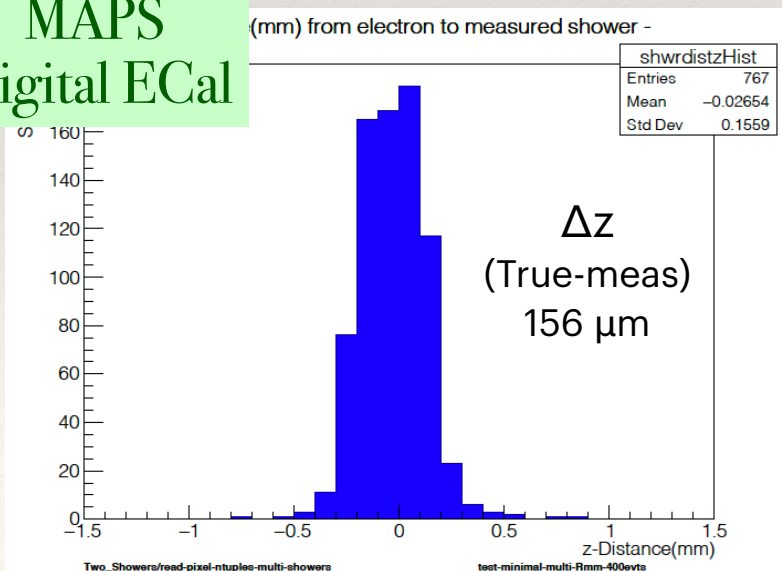




Reconstructing positions of Random number distribution of electrons



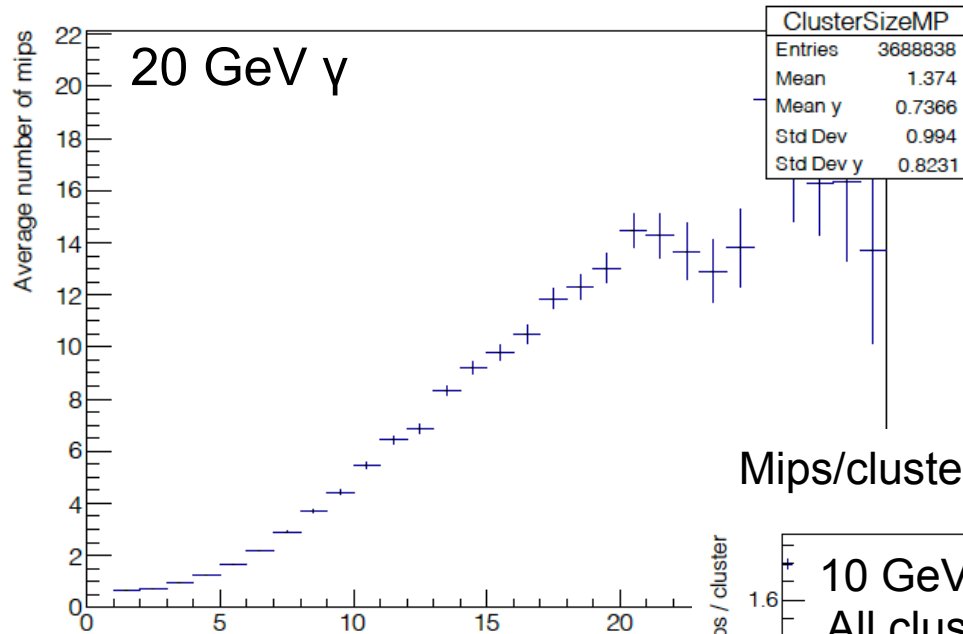
SiD
MAPS
Digital ECal





Mips/cluster and shower radius dependence

Average mips vs. Cluster Size

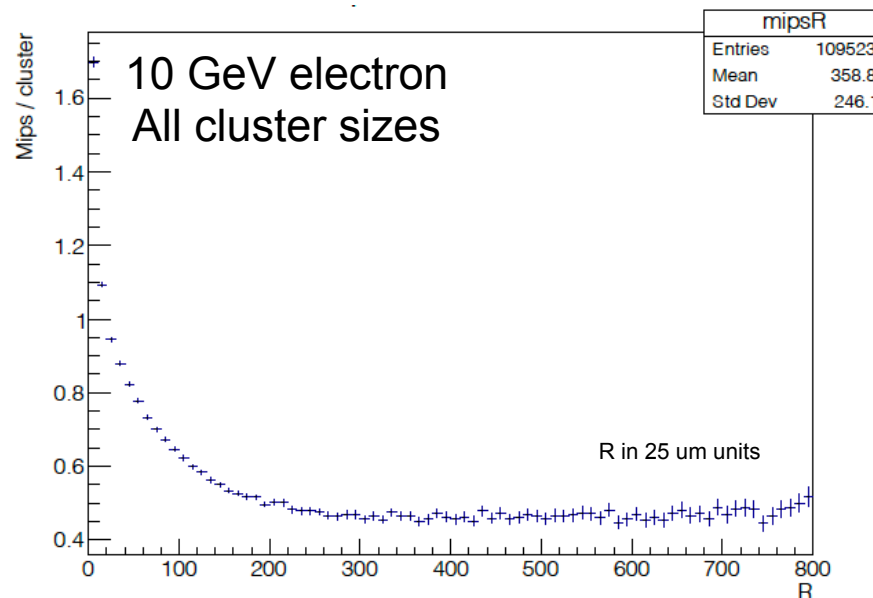


Cluster details “sense” number of mips:

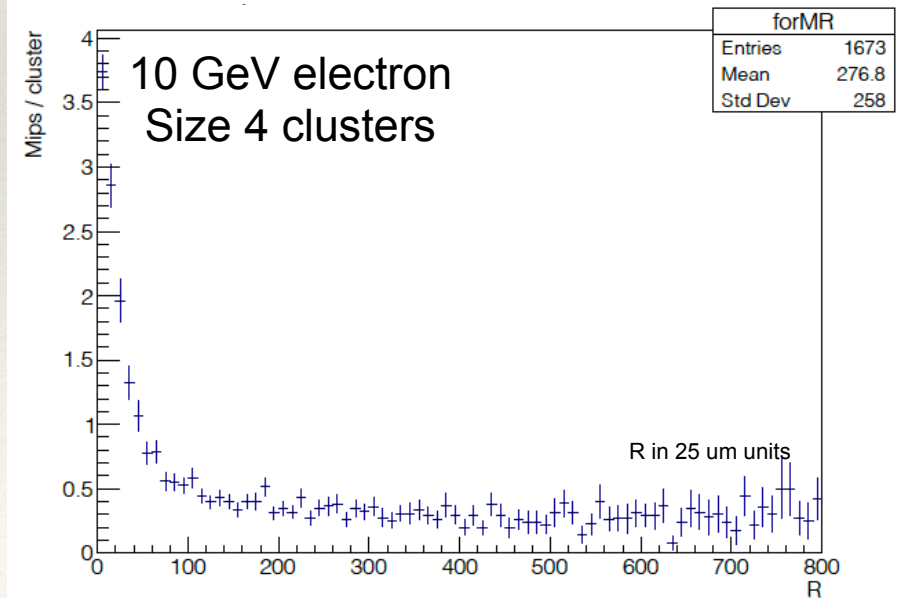
- Radius from shower axis;
- Longitudinal position (layer number);
- Cluster shape.

Analysis using these parameters improves cluster resolution in preliminary studies.

Mips/cluster vs. Radius from shower axis



Mips/cluster vs. Radius from shower axis





Ongoing studies - Sensor development and shower analysis

- ❖ Sensor development progressing.
- ❖ Shower performance studies advancing:
 - ❖ Various cluster features “sense” mip count in “large” clusters.
 - ❖ So far, each cluster is assumed to hold one mip, but cluster features show potential to improve this assumption:
 - ❖ Based on radial position in shower;
 - ❖ Based on longitudinal position in shower;
 - ❖ Based on shape of cluster;
 - ❖ THESE ARE ALL BEING INVESTIGATED, along with other aspects that show promise for improved precision.
- ❖ WE ARE LOOKING FOR COLLABORATORS - JOIN US!