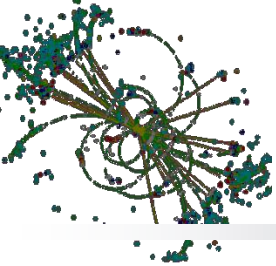


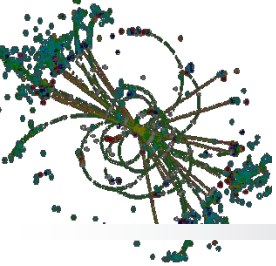
Chronopixel Silicon CMOS Sensor Development for the ILC

N. B. Sinev
University of Oregon, Eugene

In collaboration with J.E.Brau, D.M.Strom (University of Oregon, Eugene, OR), O.Baker, C.Baltay, C.Weber (Yale University, New Haven, CT)*

** Currently at BNL*

EE work is contracted to Sarnoff Corporation



Outline of the talk

- **Very brief reminder of Chronopixel concept:**
  - **Chronopixel is a monolithic silicon CMOS pixel sensor with enough electronics in each pixel to detect charge particle hit in the pixel and record the time (time stamp) of each hit.**
- **History**
- **Prototype 1 test results**
- **Prototype 2 features and test results**
- **Changes in prototype 3**
- **Sensor options discussion**
- **Some results of prototype 3 tests**
- **Radiation hardness tests**
- **Example of the sensor signals simulation**
- **Summary and plans**

History

- 2004 – talks with Sarnoff Corporation started.
  - Oregon University, Yale University and Sarnoff Corporation collaboration formed.
- January, 2007
  - Completed design – Prototype 1
    - 2 buffers, with calibration
- May 2008
  - Fabricated 80 5x5 mm chips, containing 80x80 50 μm Chronopixels array (+ 2 single pixels) each
  - TSMC 0.18 μm ⇒ ~50 μm pixel
    - Epi-layer only 7 μm
    - Low resistivity (~10 ohm*cm) silicon
- October 2008
  - Design of test boards started at SLAC
- September 2009
  - Chronopixel chip tests started
- March 2010
  - Tests completed, report written
- May 2010
  - contract with Sarnoff for developing of second prototype signed
- February, 2012
  - Submitted to MOSIS for production at TSMC. (48x48 array of 25 mm pixel, 90 nm process)
- June 6, 2012
  - 11 packaged chips delivered to SLAC (+ 9 left at SARNOFF, +80 unpackaged.)
  - Tests at SLAC started
- March 2013
  - Test results are discussed with Sarnoff and prototype 3 design features defined
- July 2013
  - Contract with Sarnoff signed
- April 2014
  - Design submitted for fabrication
- August 13, 2014
  - prototype 3 chips arrived at SLAC
- October 2014
  - Prototype 3 tests started
- 2016-2017
  - Chronopixel irradiation campaign

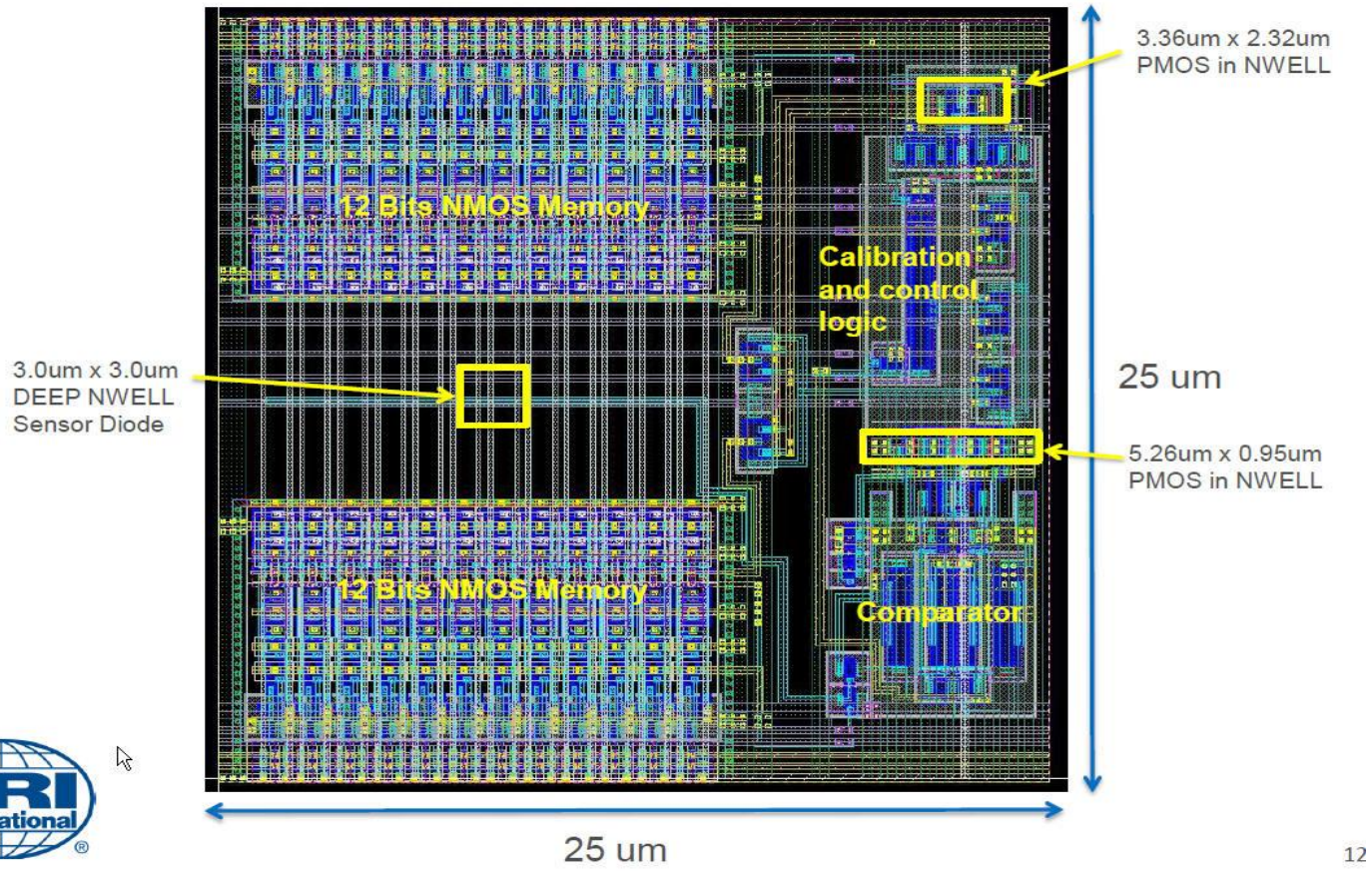
Prototype 1 summary

- Tests show that general concept is working.
- Noise figure with "soft reset" was within specifications (0.86 mV/35.7μV/e = 24 e, specification is 25 e).
- Comparator offsets spread 24.6 mV expressed in input charge (690 e) is 2.7 times larger required (250 e).
- Sensors leakage currents ($1.8 \cdot 10^{-8} A/cm^2$) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz.
- No problems with pulsing analog power.
- Pixel size was 50x50 μm^2 while we want 15x15 μm^2 or less.
- However, CMOS electronics in prototype 1 need to be encapsulated in deep p-well, otherwise n-wells of PMOS transistors will compete with signal diode n-well. This require special process which is not available for smaller feature size (less than 180 nm).
- Digital comparators offset compensation circuit limited our ability to reach required accuracy

Prototype 2 features

- Design of the next prototype was extensively discussed with Sarnoff engineers. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all electronics inside pixels only from NMOS transistors. It can allow us to have 100% charge collection without use of deep P-well technology, which is expensive and rare. To reduce all NMOS logics power consumption, dynamic memory cells design was proposed by SARNOFF.
- New comparator offset compensation ("calibration") scheme was suggested, which does not have limitation in the range of the offset voltages it can compensate (analog vs digital in 1st prototype).
- In September of 2011 Sarnoff suggested to build next prototype on 90 nm technology, which will allow to reduce pixel size to 25μ x 25μ
- We agreed to have small fraction of the electronics inside pixel to have PMOS transistors. Though it will reduce charge collection efficiency, but will simplify comparator design. It is very difficult to build good comparator with low power consumption on NMOS only transistors.

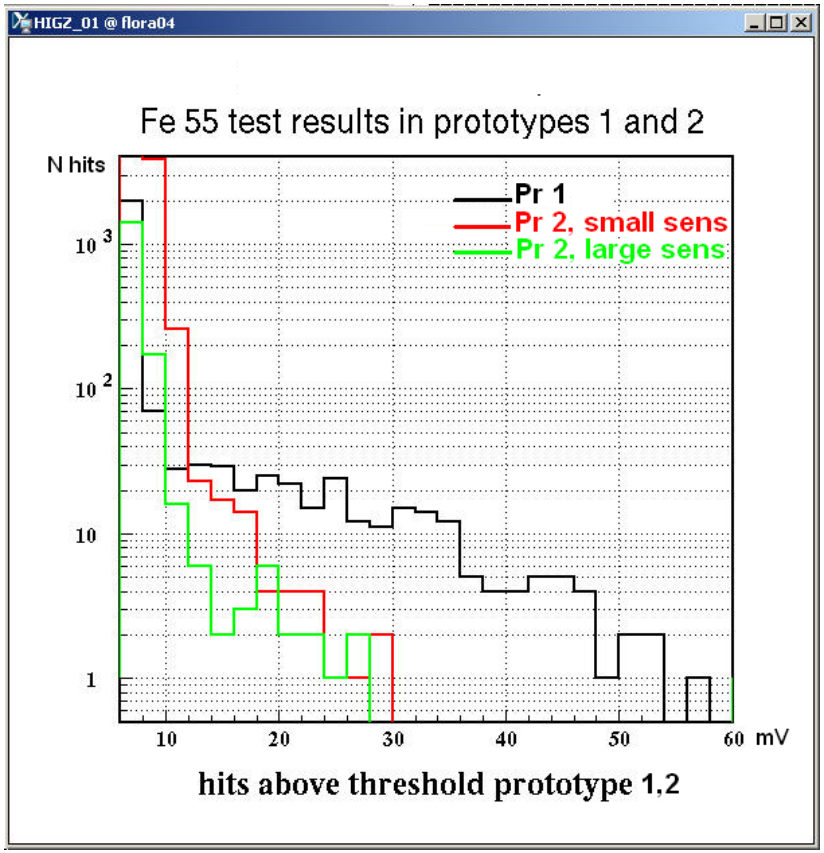
Prototype 2 pixel layout



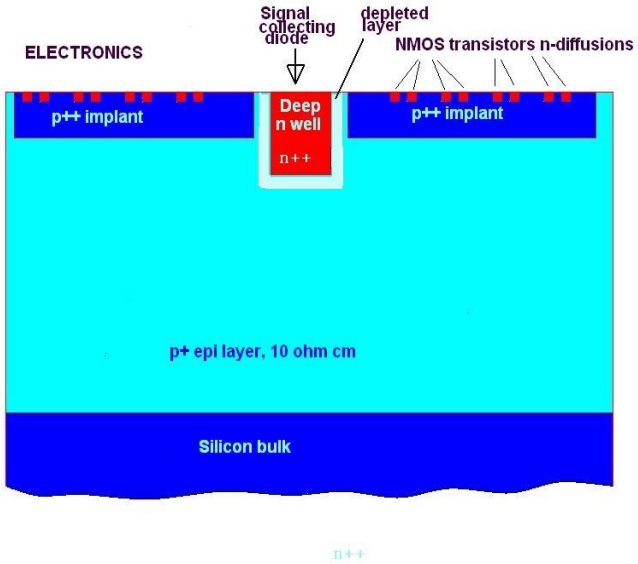
All N-wells (shown by yellow rectangles) are competing for signal charge collection. To increase fraction of charge, collected by signal electrode (DEEP NWELL), half of the pixels have it's size increased to 4x5.5 μ^2 .

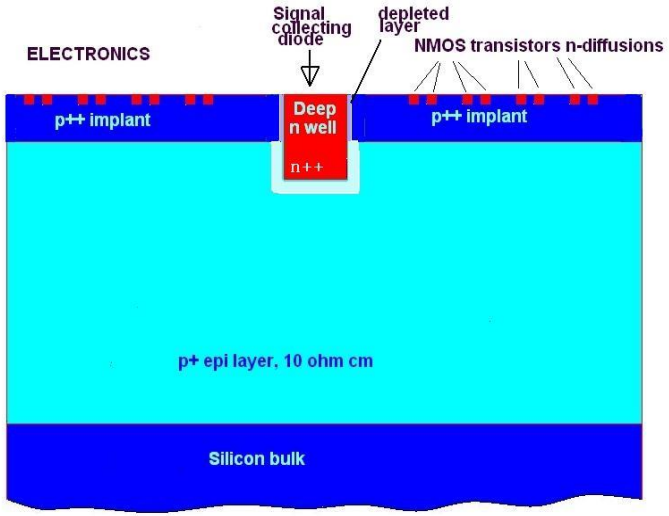
Prototype 2 test results – sensor capacitance

- Comparison of the Fe 55 signal distributions for prototype 1 and 2. Sensor diode size in prototype 1 was ~100 μ^2 Prototype 2 has 2 sensor size options – 9 μ^2 and 22 μ^2 ("small" and "large" on the plot) . The maximum signal value is slightly larger for sensor of smaller size, as one would expect, though we would expect larger difference in maximum signal values here. But capacitance of the sensor from this measurements (~9 fF) appeared much larger than our expectation (~1-2 fF).



What got wrong?





- We hoped, that pixel cross-section will look like what is shown on left picture. But it appeared, that in 90 nm design rules it is not allowed to have window in the top p++ implant around deep n-well, which forms our sensor diode. Resulting pixel cross-section is shown on right picture. Very high doping concentration of p++ implant leads to very thin depletion layer around side walls of deep n-well, which creates additional large capacitance.

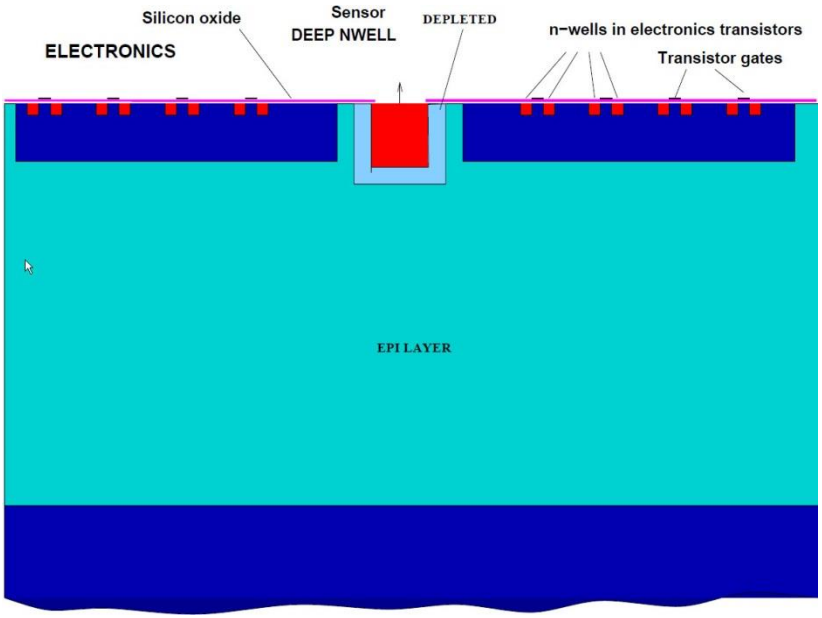
Summary of prototypes 1 and 2 tests

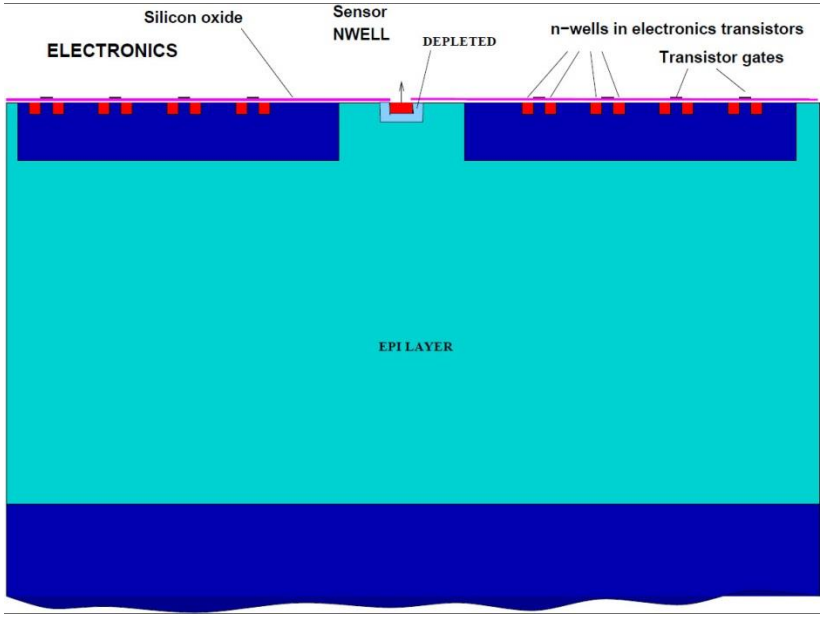
- **From both, first and second prototype tests we have learned:**
  - **1. We can build pixels which can record time stamps with 300 ns period (1 BC interval) - prototype 1**
  - **2.We can build readout system, allowing to read all hit pixels during interval between bunch trains (by implementing sparse readout) - prototype 1**
  - **3.We can implement pulsed power with 2 ms ON and 200 ms OFF, and this will not ruin comparator performance - both prototype 1 and 2**
  - **4. We can implement all NMOS electronics without unacceptable power consumption - prototype 2. We don't know yet if all NMOS electronics is a good alternative solution to deep P-well option.**
  - **5. We can achieve comparators offset calibration with virtually any required precision using analog calibration circuit.**
  - **6. Going down to smaller feature size is not as strait forward process as we thought. Sensor capacitance became an issue, limiting signal/noise ratio. And the main problem here seems to stem from 90 nm process design rules.**

Sensor options in prototype 3

- 6 different sensor options were implemented on the same chip – 8 column allocated for each option:
  - 1 – same as in prototype 2 – for comparison
  - 2 – deep NWELL diode in the window in P++ layer – this violate design rules, but the waver for design rules was accepted by TSMC
  - 3 – shallow NWELL diode also in the window – also violates design rules, but waver was accepted
  - 4 – "Natural transistor" (NTN) allowed by design rules to be in the P++ layer window – transistor is formed directly on P+ epi layer. Large source and drain diffusion areas, gate connected to both source and drain and form sensor output
  - 5 – also NTN but with 2 fingers, source and drain are narrow, gate also connected to both, as in option 4
  - 6 – same as 5, however gate is not connected to source and drain, but connected to external bias voltage.

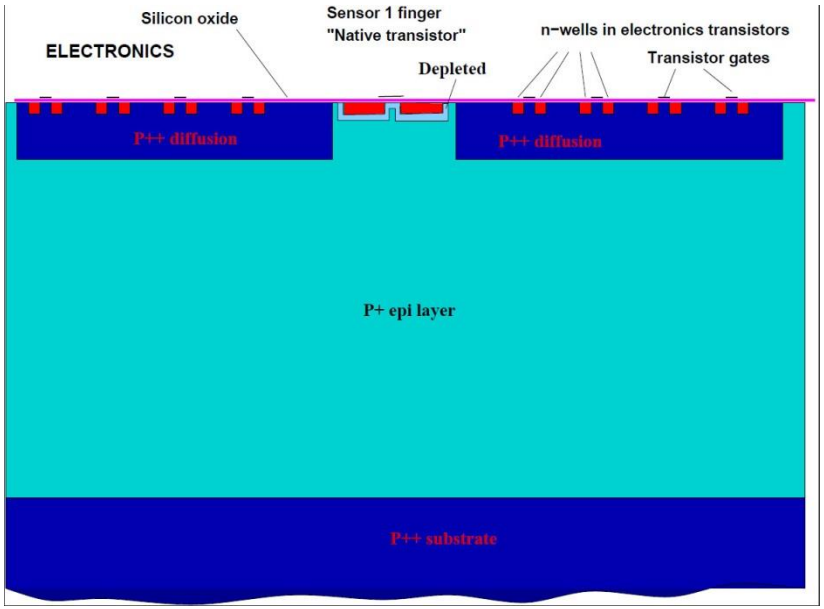
Options with NWELL diode – violating design rules

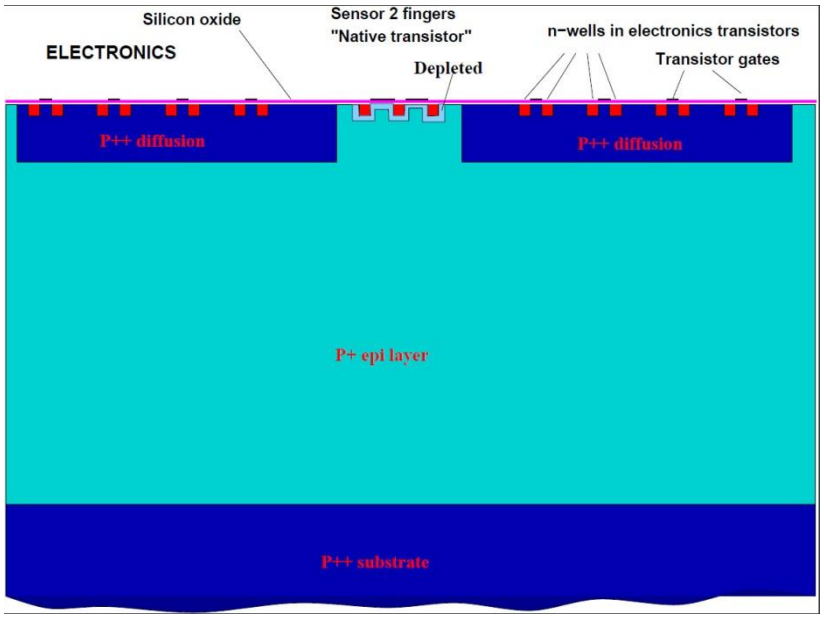




It will be interesting to compare deep and shallow nwells. Deep has larger area, so larger charge collection efficiency, however, larger capacitance. Shallow option has smaller area, but because P++ acts as charge reflector, the charge collection efficiency may be defined not by diode size, but by window size. It depends on how deep is P++ implant, of course.

Options with “Natural transistor”

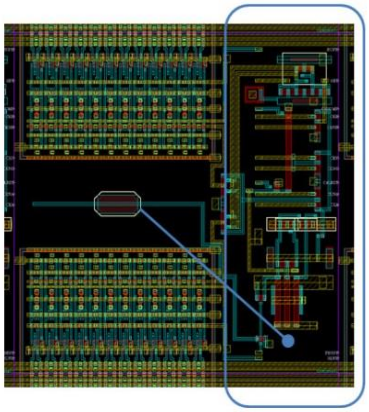




In 1 finger option the size of nwells forming source and drain is larger, so we can hope for better charge collection efficiency. However, sensor capacitance may be larger also. There is 2 2-finger options – one with gates connected to source and drain, another – to external bias. It will be interesting to see how these two options behave

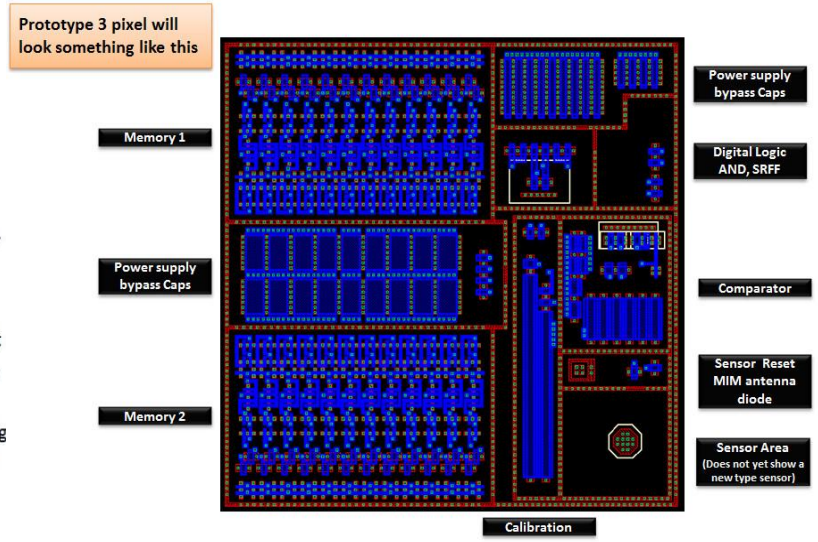
Difference in proto 2 and 3 layouts

Proto 2 Comparator and Sensor



- Re-layout comparator region
  - Try to put Nwells closer to each other
- Investigate alternate no-Nwell comparator possibilities
  - Time and area permitting
- Construct sensor with NTN (no Pwell)
- Move sensor to different location nearer to comparator
  - Currently located under MIM
    - Better chance for a light slot by moving it
  - Currently also located under time stamp data lines
    - Must move to prevent capacitive coupling of time stamp data lines to sensor metal line

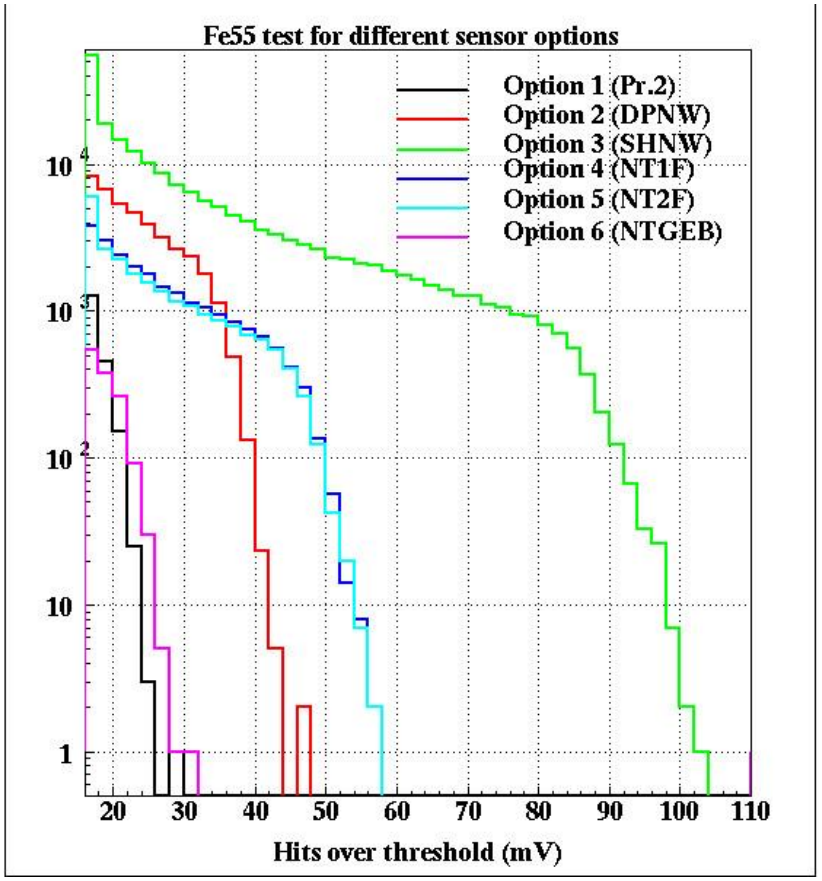
Pixel Active Devices Overview (Prototype 3 basic plan)



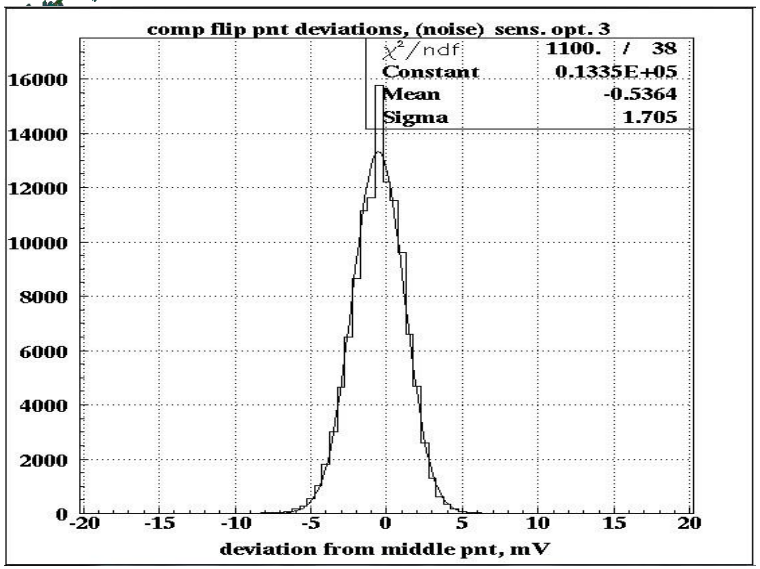
Here are 2 slides from SRI showing their plan to address prototype 2 crosstalk problems

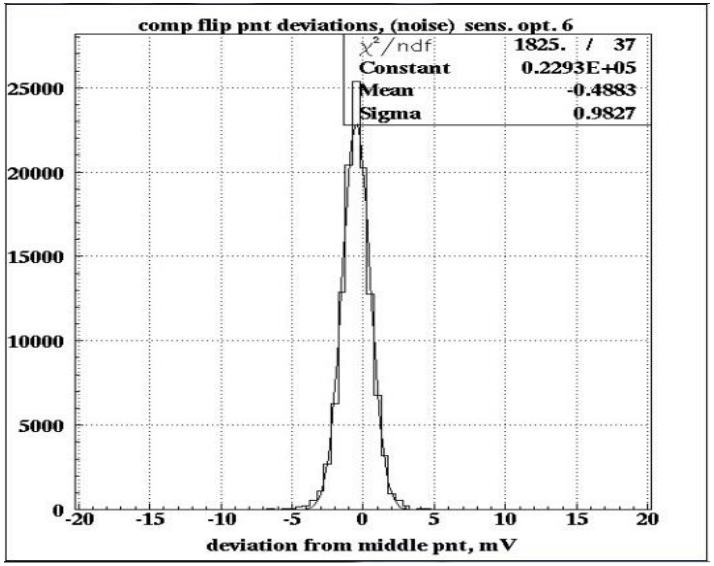
Fe55 test

- Method of measuring sensor capacitances consist in the observation of signal from radioactive source Fe55. It emits low energy (5.9 KeV) X-rays. Such X-rays are absorbed in the silicon, and all their energy goes into creation of electron-hole pairs. The energy to create one such pair is well known, and is 3.66 eV for Si. So, from maximum observed signal we can calculate capacitance. Taking into account, that Fe55 has about 10% of decays with energy 6.49 KeV, we can get following capacitances:
- Opt. 1 – 9.04 fF, opt 2 – 6.2 fF, opt 3 – 2.73 fF, opt 4 and 5 4.9 fF and option 6 – 8.9 fF



Sensor noise measurements





- **Plots above show noise measurements for sensor options with minimum capacitance (option 3, C=2.73 fF) on left, and maximum capacitance (option 6, C=8.9 fF) on right. Qualitatively they agree with expectation – larger capacitance – smaller noise, but they are larger, than expected from KTC noise formula. That means, that there are additional noise pick up, and table on the next page will give you estimated values of such pick up.**

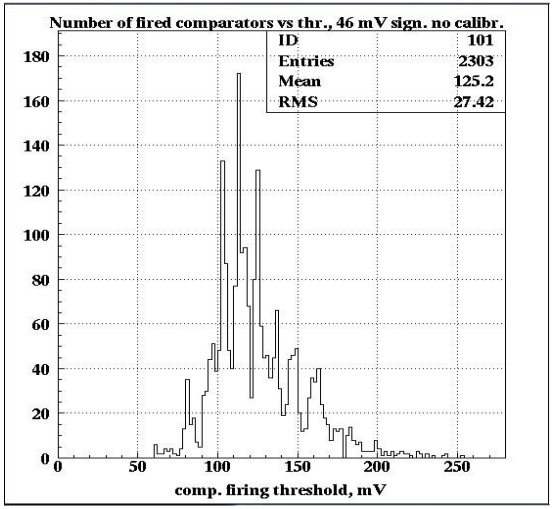
Noise observed vs expected

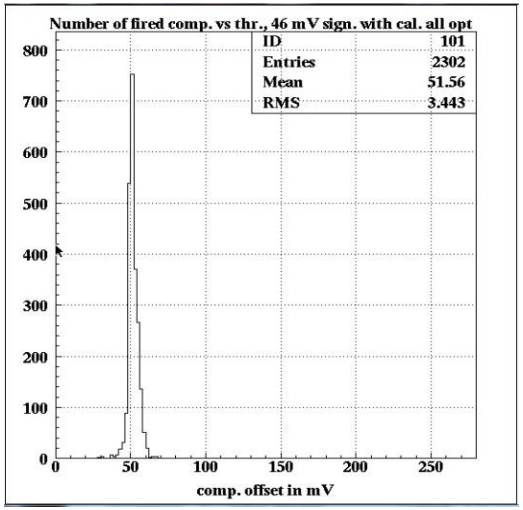
- Table at the right shows measured noise values (mV) for different sensor options, and comparison with expected values from KTC noise formula and computed from Fe55 test capacitances.
  Interesting to notice. that extra noise pick up is largest for smallest capacitance, which is not a surprise, if pick up occurs through capacitive coupling to the sensor. Option 1 seems does not follow this rule – it has largest capacitance, but not smallest pick up. However, it can be understood from the fact, that these pixels are closest to the sensor edge, where most pulsed control signals are formed.

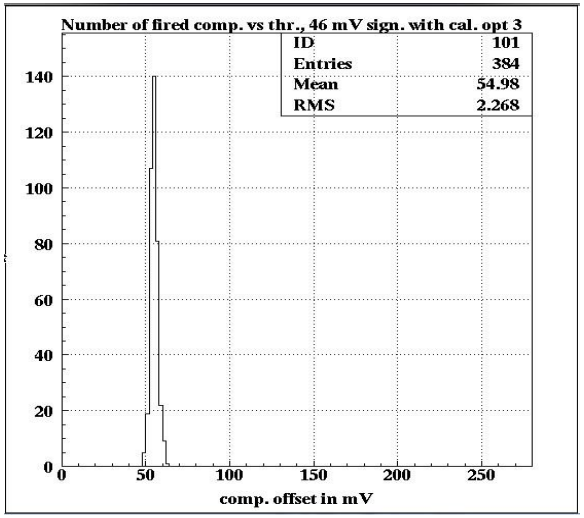
Option	sigma obs.	sigma exp.	Sqrt ($\delta^2_{ob} - \delta^2_{ex}$)
1	1.12	0.67	0.9
2	1.08	0.8	0.73
3	1.7	1.21	1.2
4	1.21	0.9	0.8
5	1.23	0.9	0.84
6	0.98	0.67	0.72

We hoped, that reduction in the photodiode reset pulse amplitude can reduce noise. However, recent tests have sown that it does not help.

Comparator offset compensation

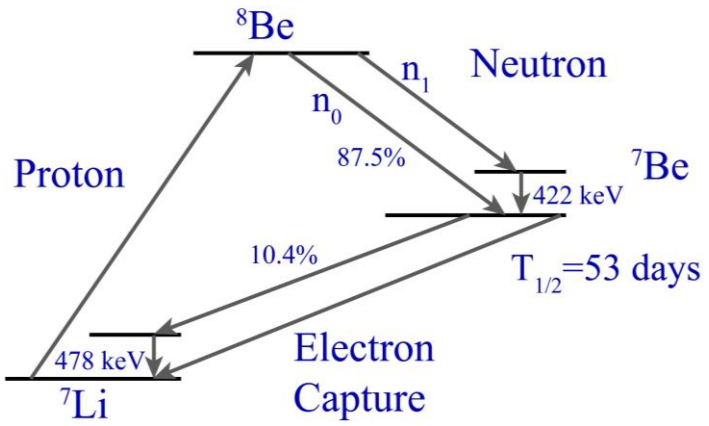






- **Left picture shows distribution of comparator offsets before compensation (we call it calibration), middle – the same after compensation for all pixels, right – after compensation for pixels with sensor option 3. From the fact, that signal of 46 mV fires comparators at slightly larger threshold, and that this difference is different for different sensor options we can conclude, that such calibration is affected by additional noise pick up.**

Neutron Irradiation Test



G.H.R Kegel et al, IEEE TNS vol39, No6 (1992)

- 4 MeV proton incident on ^{7}Li target to produce neutrons
- Proton beam current and neutron rate monitored during irradiation test
- Total number of neutrons created is eventually determined by radiation assay of target
- Chronopixel works after 10^{13} n_{eq}/cm^2

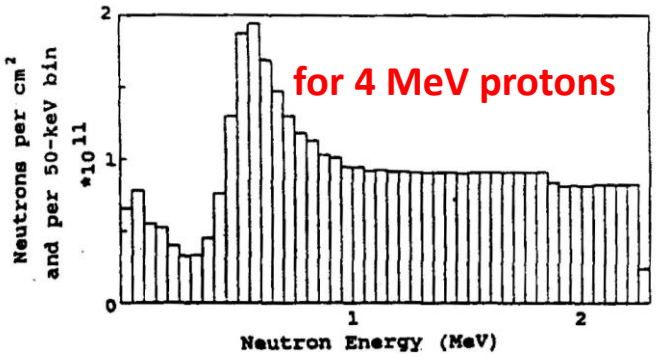
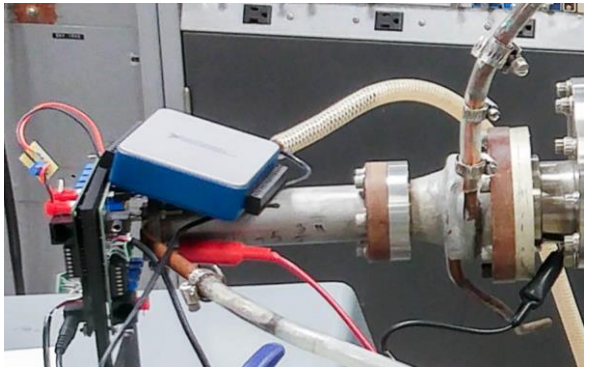


Figure 4. A calculated neutron energy histogram.



Lithium target

Total integrated dose test

Test resistance w.r.t. total ionizing dose received

1MeV protons

4 nA current
(large dose rate!)

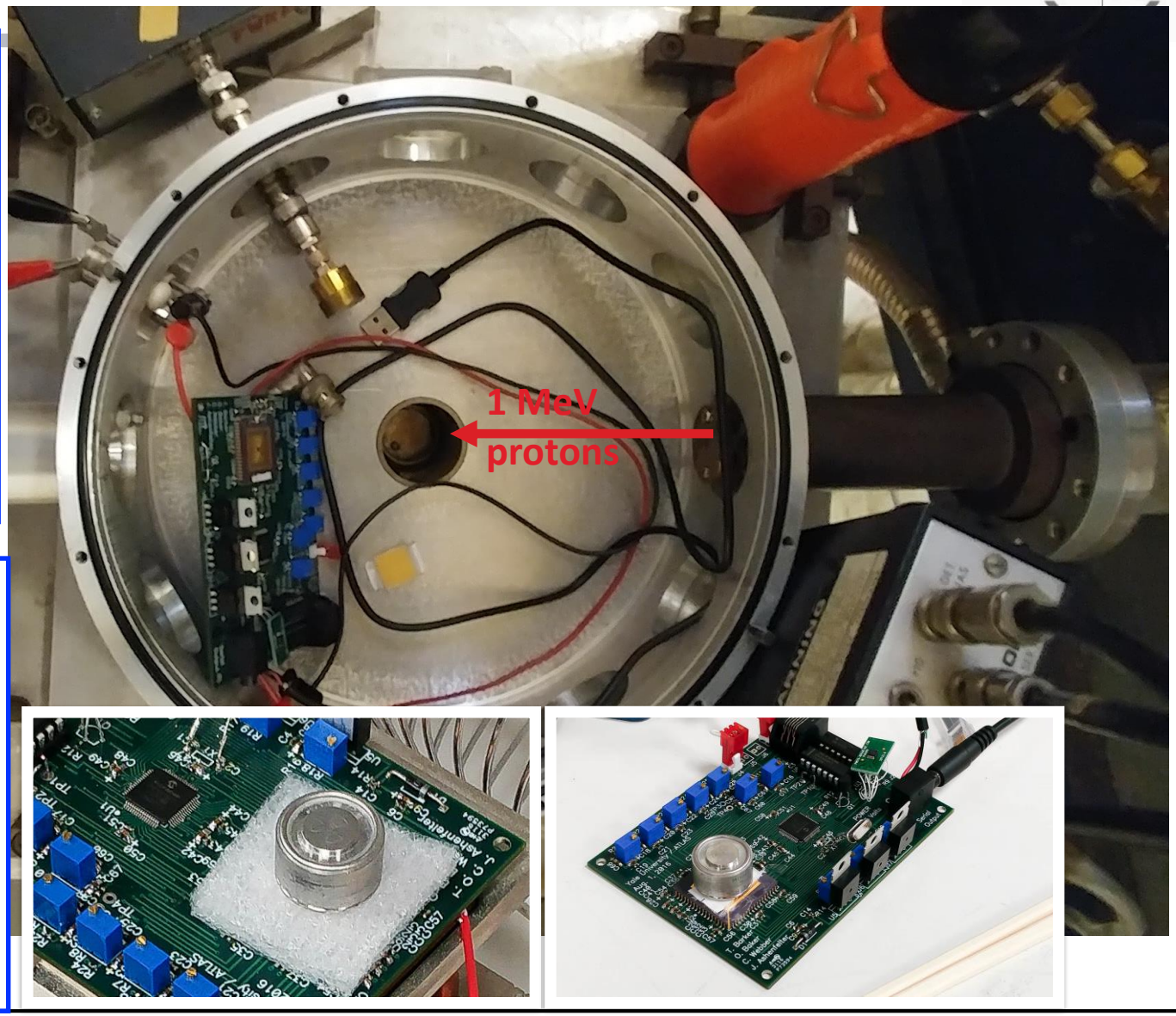
Energy deposited within first 8 µm of silicon
(≈ epi layer)

Multiple irradiation runs

After each irradiation run

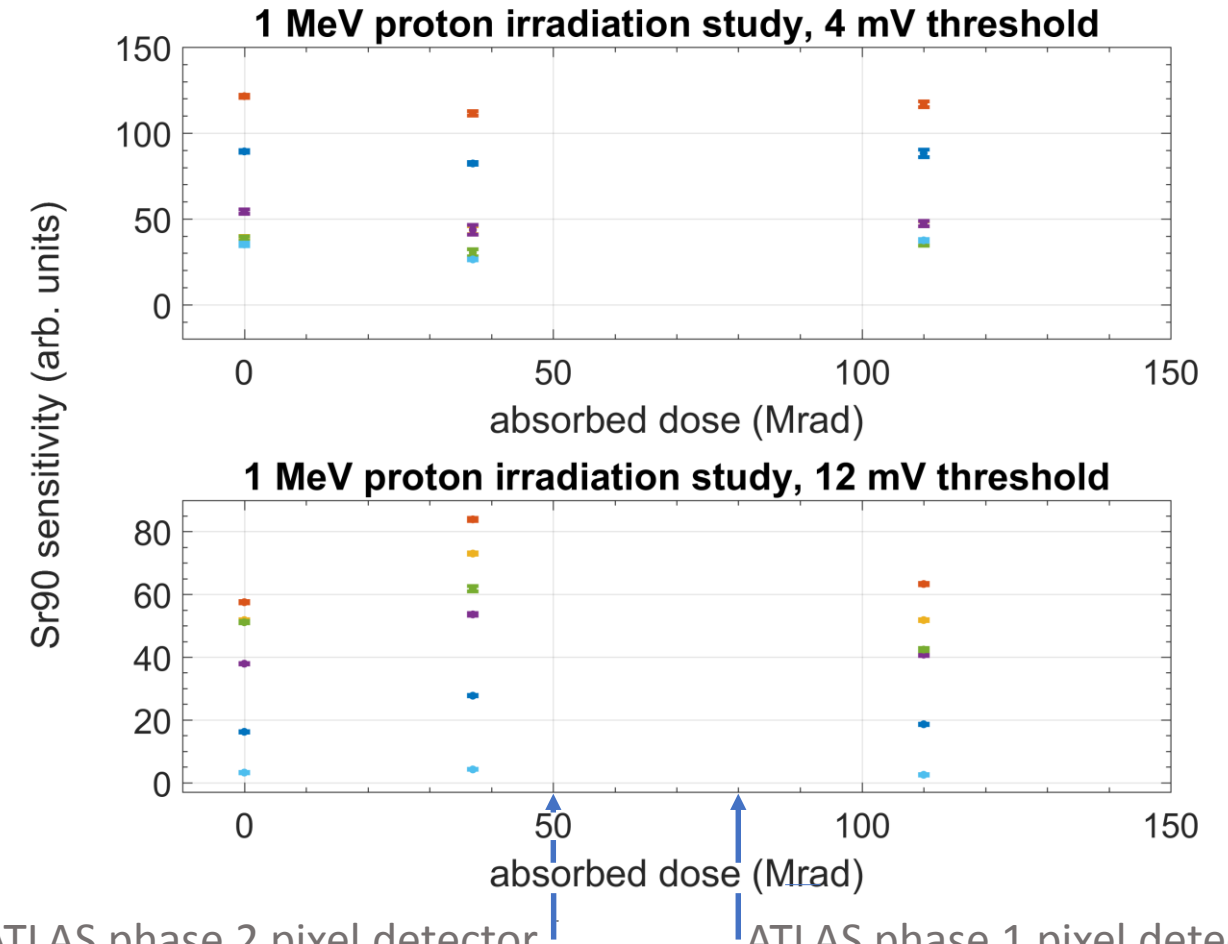
Anneal at 60°C for 80 min

Test for change in count rate using Sr-90 source ($t_{1/2} = 29$ yrs, 2.3 MeV β, minimum ionizing)

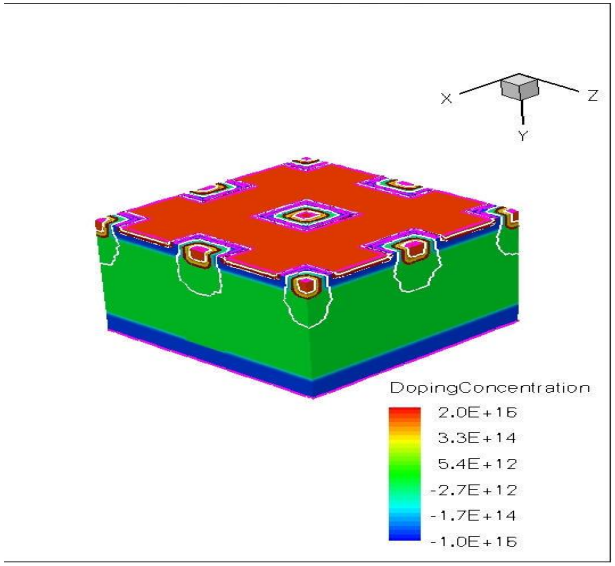


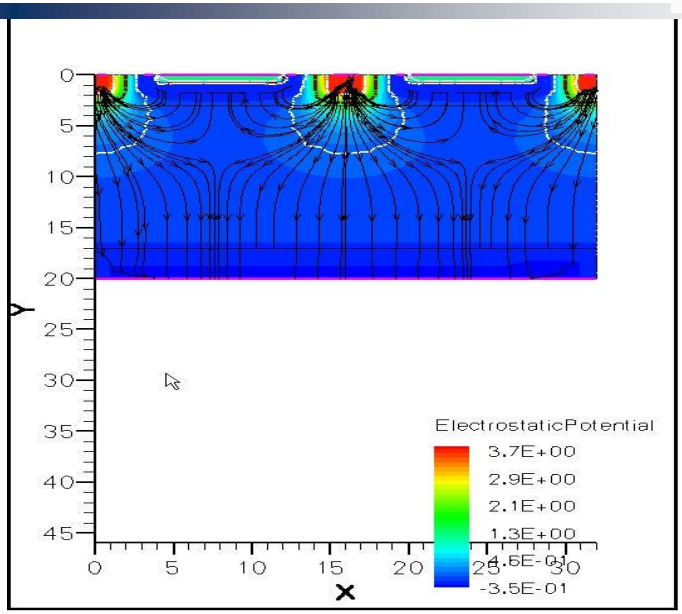
MeV proton irradiation results

- sensor type 1
- sensor type 2
- sensor type 3
- sensor type 4
- sensor type 5
- sensor type 6



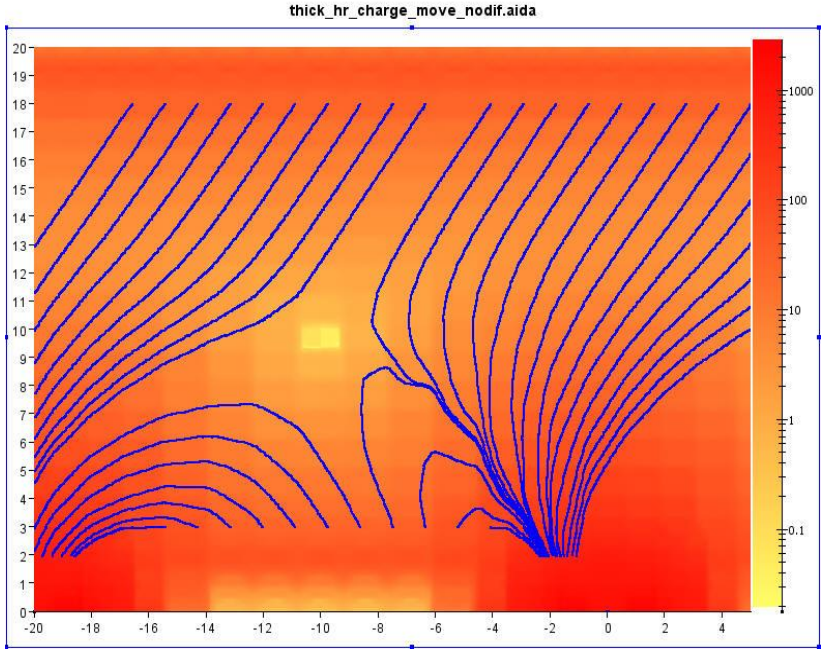
Charge carriers movement in Si

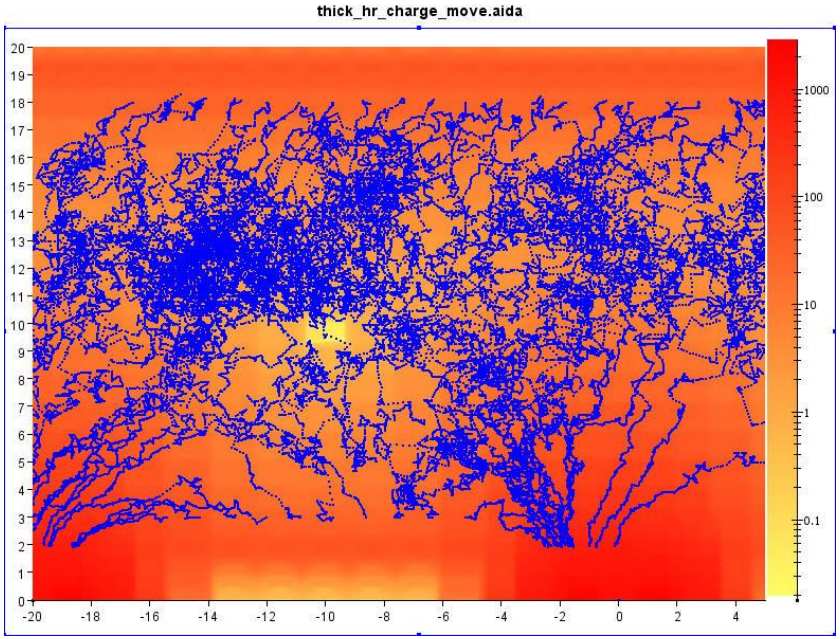




- **To simulate charge carriers movement inside silicon, we need to know electric and magnetic fields there and silicon parameters, such as carriers mobility, Lorentz angle, diffusion constants. To find electric field, I am using Tcad (dessis) simulation, same as used by semiconductor devices developers . Pictures above illustrate such simulations. On the left is doping concentration distribution. This is simulation input. On the right – electric field – this is output. Depleted regions are outlined with white line.**

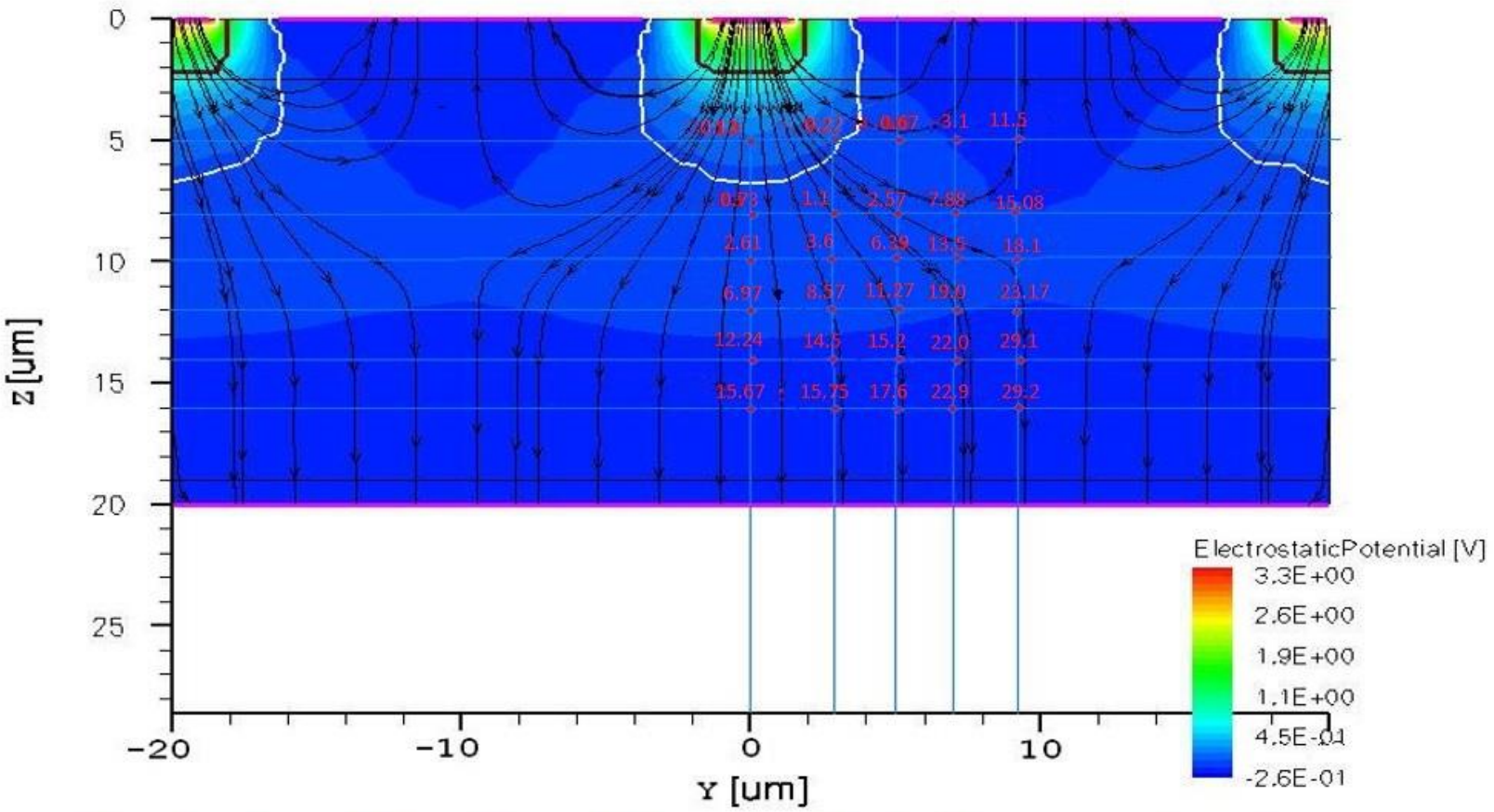
Charge carriers movement - illustration



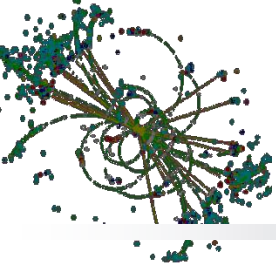


- **Illustration of charge carrier movement simulation. On the left diffusion was turned off, on the right – real movement, which includes diffusion. Background color shows the strength of electric field. Magnetic field of 5 Tesla is perpendicular to picture plane. (picture is upside down compare to previous slide).**

Is this sensor fast enough?



Carriers travel times from different points inside sensor (in ns)



ILC Chronopixel performance

Parameter	ILC Requirement	Prototype Tests
Detector Sensitivity	10 µV/electron	59 µV/electron
Detector Noise	25 electrons	29 electrons
Comparator Accuracy	0.2 mV RMS	0.2 mV RMS
Sensor Capacitance	10 fF	2.7 fF
Clocking Speed	3.3 MHz	7.3 MHz
Charge collection time	300 ns	30 ns
Readout Rate	25 Mbits/sec	25 Mbits/sec
Power Consumption	0.13 mW/mm^2	OK by estimate
Radiation Hardness	10^{11} neutrons/cm^2/yr	10^{13}neutrons/cm^2 or 110 Mrad

Summary and plans

- Chronopixel R&D have been successful, with many problems solved and proof that concept is valid.
- Looks like the problem with large capacitance of sensors in 90 nm technology is solved!
- Much more work is needed to fully understand details of sensor operations. We absolutely need to measure sensor efficiency for minimum ionizing particles.
- Cross talk issues were addressed in prototype 3 by separating analog and digital powers and putting small decoupling capacitors into each pixel. However, we still see some effect of cross talks. It is not a show-stopper, as effect is relatively small, but we need to think about minimizing it.
- For final design we need thicker epi layer (larger signal) and higher resistivity of it – larger depletion depth will increase charge collection efficiency. The challenge for final design is also chip size. Prototype 3 has ~1.2x1.2 mm^2 active area, we will need few cm^2 .