What do we need for EM shower studies ?

- Pedestal determination
- MIP calibration
  - Requires hold optimization
  - Requires gain-selection DAC optimization (autogain)
- Threshold optimization
  - → and conversion to MIPs

- Reminder: the optimization of the detector for cosmics is not optimal for real data taking
  - Extra masking (to avoid retriggers)
  - High thresholds (that will also impact in the optimal hold-values)

Data location

/eos/project/s/siw-ecal/TB2020-11/commissioning/data

bash-4.2$ ls -ltrh

drwxr-xr-x. 2 siwecal le 4,0K jun 17 2020 injection_20200610

drwxr-xr-x. 2 siwecal le 4,0K jul 12 2020 cosmics_202006_14slabs

drwxr-xr-x. 2 siwecal le 4,0K sep 16 2020 testbench_llr

drwxr-xr-x. 2 siwecal le 4,0K oct 15 2020 converted_data

drwxr-xr-x. 2 siwecal le 4,0K oct 23 2020 cosmics_202010_11slabs

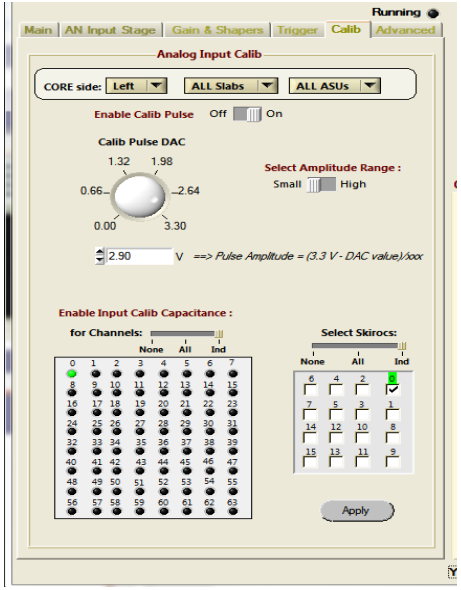
drwxr-xr-x. 2 siwecal le 4,0K jun 8 15:40 cosmics_202006_15slabs

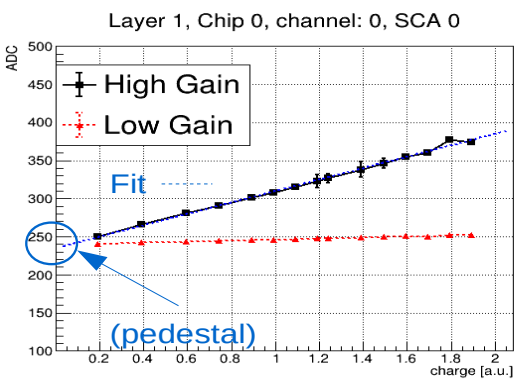
drwxr-xr-x. 2 siwecal le 4,0K jun 8 16:01 cosmics_202008_15slabs

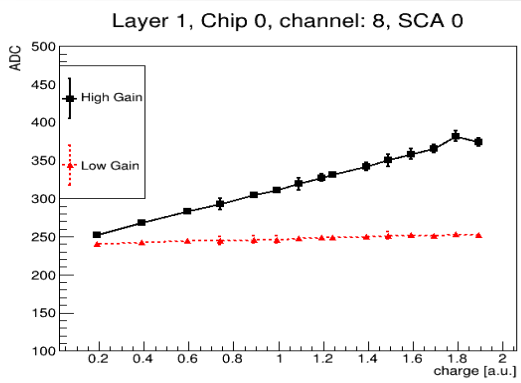
- New data to be stored in
  - **/eos/project/s/siw-ecal/TB2021-12/commissioning/data**
- Software (data conversion, etc)
  - https://github.com/SiWECAL-TestBeam/SiWECAL-TB-analysis
  - Branch slboard_TB2020

Pedestal

- Usually estimated with autotrigger checking the spectrum of the non-triggered cells
- Is this the actual pedestal?
- The SL-board is able to inject (in all modules at once) signals in the in_calib







- Semiautomatic procedure to calibrate sca 0-3 for all channels of all 15 SLABS
  - Low gain and high gain
- Possibility to compare pedestal with fit method with pedestal obtained with “hit bit = 0”
- And also with a external generator

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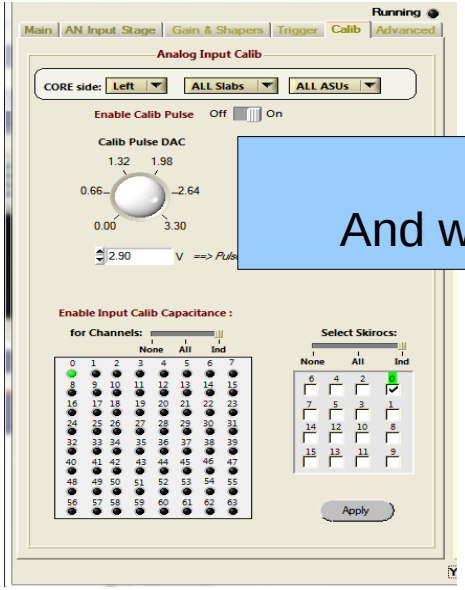

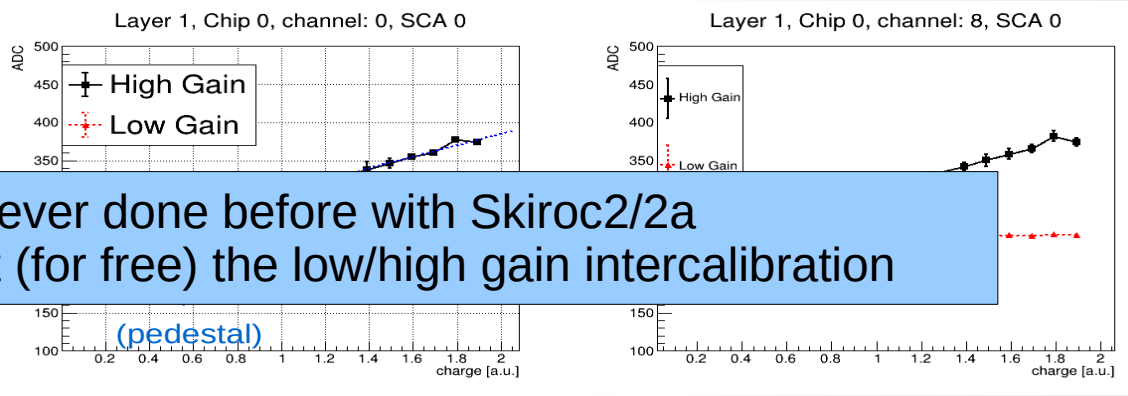

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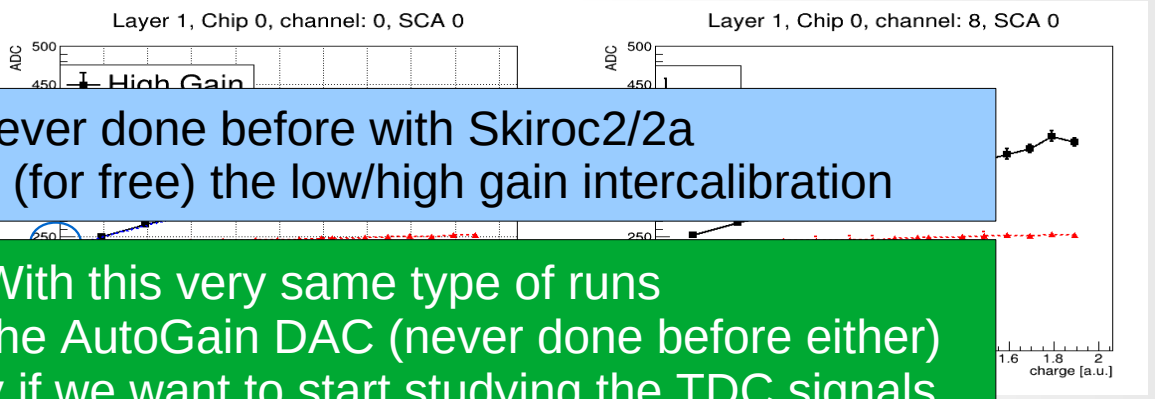

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With this very same type of runs
we calibrate the AutoGain DAC (never done before either)
→ mandatory if we want to start studying the TDC signals

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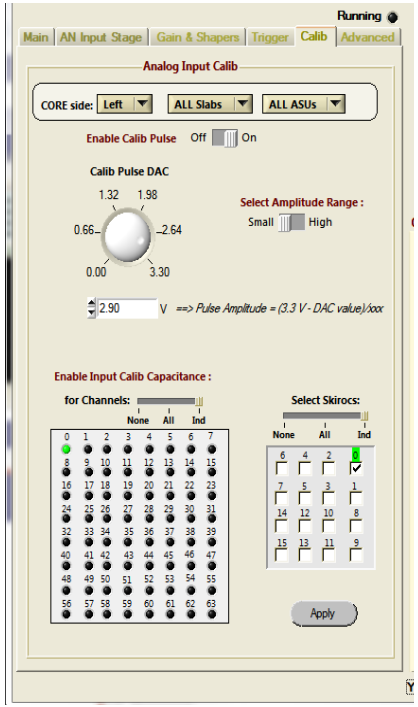
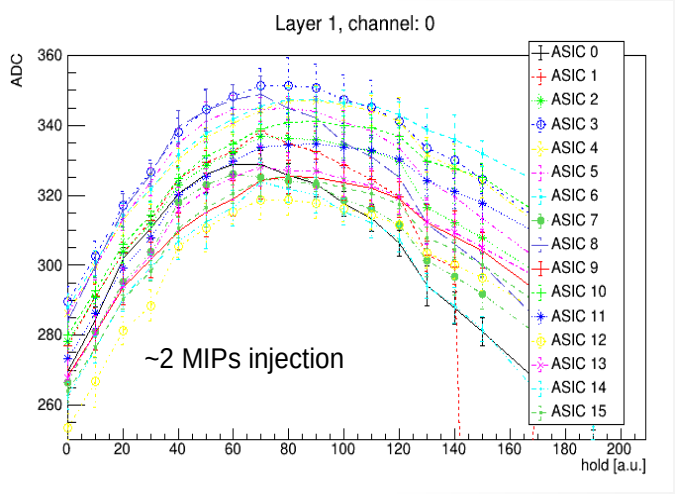
Holdscans

- Only done with “fake” signals
  - Could this be validated with cosmics ? (we require to have only few channels per chip enabled)
  - Depends on threshold?





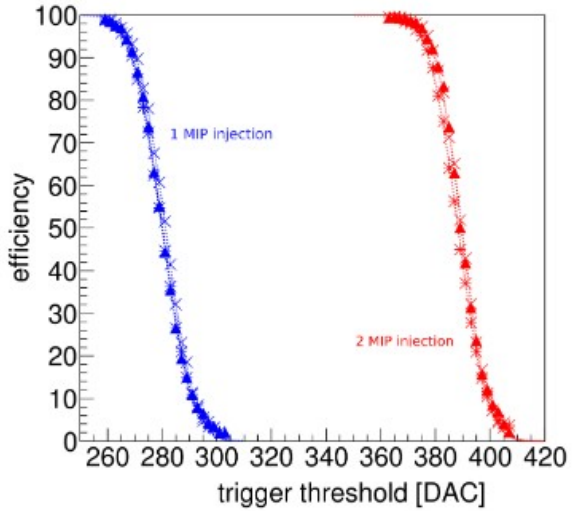
- Semiautomatic procedure to calibrate the hold of all chips

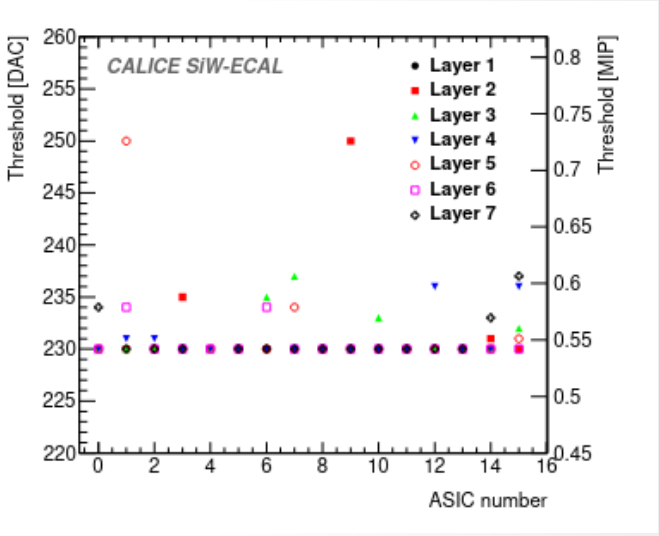
Calibration of the injection system

- We inject a charge from a pulse generated via hardware… (tuneable DAC)
  - Is this signal similar to real signals?
  - What are the values in DAC that correspond to MIPs?
  - Can we use cosmics for that?

Threshold optimization

- We are optimizing the thresholds only using noise.
- Only (?) with s-curves with signals we can properly determine the real position of the threshold
  - Or with high statistic runs with particles in different angles (showers?)





- The S/N calculated with the left plot (injection, testboard) was validated with dedicated runs at beam test…
  - We managed to do it for only few chips and the central boards. We extrapolated the analysis to the rest.
  - These results are “improvable” (being polite with myself)

My proposal

- Dedicate a fair amount to injection tests
  - Holdvalue optimization (scan of different holds)
  - Linearity + pedestal estimations (scan of different input charges)
  - Scuves with different size of external signals (to estimate the S/N and the real position of the threshold)
- Validate / calibrate the signal injection
  - With an external pulse generator ?
  - With cosmics (a very long run that allow to select “perpendicular” tracks) The MIP in ADC should correspond to the ADC of an unknown value of the Calib Pulse DAC
- Check the pedestals with cosmics (very long run that allow to select “perpendicular” tracks)
  - And provide a first MIP calibration

- All this has to be validated at beam test
  - 1-2 days of setup
  - 5- days scans / optimization of settings + position scan
  - 3 days for showers at different energies → since we will have only 1 tungsten configuration
  - 4 days of TLU integration + finishing previous runs

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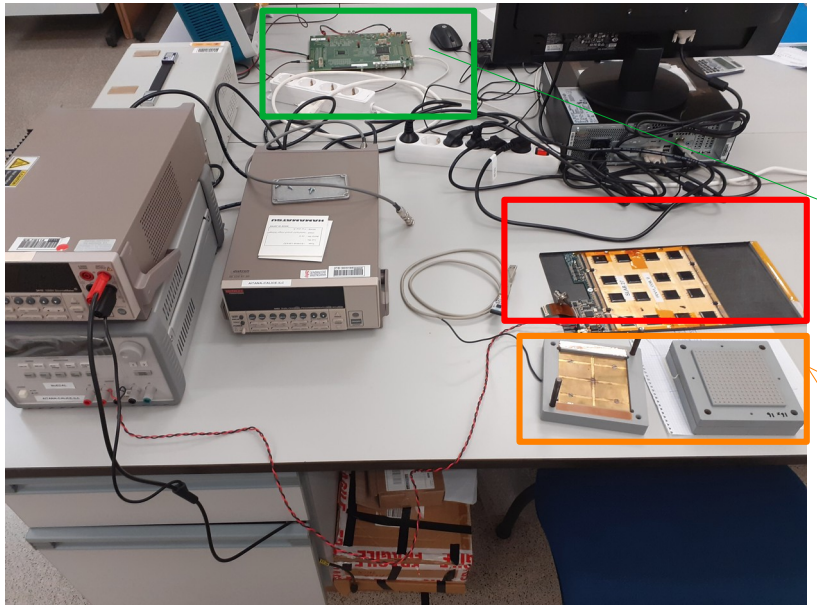
Simulation DD4HEP

- Very similar to 2017 but…
- No aluminum cover in front of the slabs
- Different thickness of the carbon frame
- Not glue but cupper-scotch for the wafer-HV kapton gluing
- New HV kapton.. is the same thickness ?
- Some modules have
  - 320um wafers
  - Or 500um wafers
  - Or a mix...

CALICE has landed in Valencia



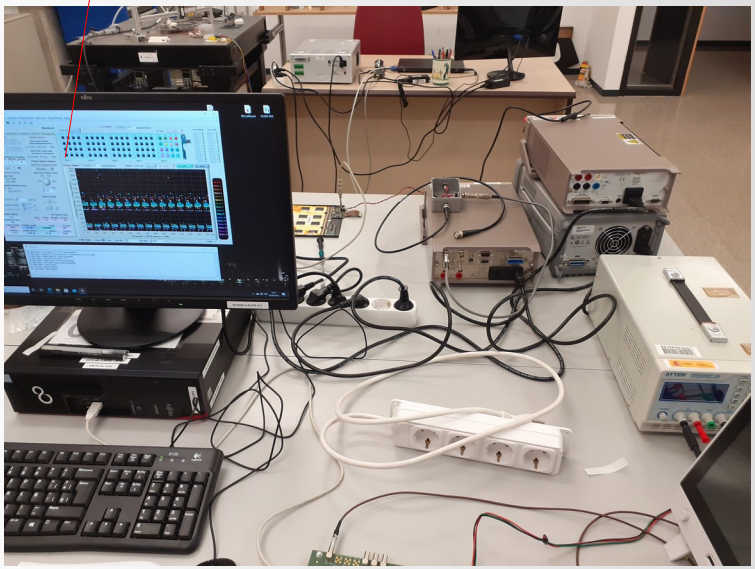
SUNG KYUN KWAN UNIVERSITY(SKKU)

IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis

OMEGA Microelectronics

LLR

LPNHE PARIS



- A full readout module (Chip-on-board) with DAQ (hardware and sofwtare)
- A wafer test bench
- Baby wafers for testing
- An ASIC testboard (and hardware)
- + cables, connectors etc...

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