TDC optimization for the SiW-ECAL ASIC Sk2a

Jaume Navarro, Adrián Irles
AITANA group at IFIC - CSIC/UV

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Stephane Callier

Motivation

- Interest in timing is a trend
- Innovative solutions with fast sensors and dedicated electronics being investigated now
- But what can we do today ?
- SK2a
  - With an ASIC developed for power pulsing and for beam test
  - And already installed in ~half of the existing slabs

SK2a

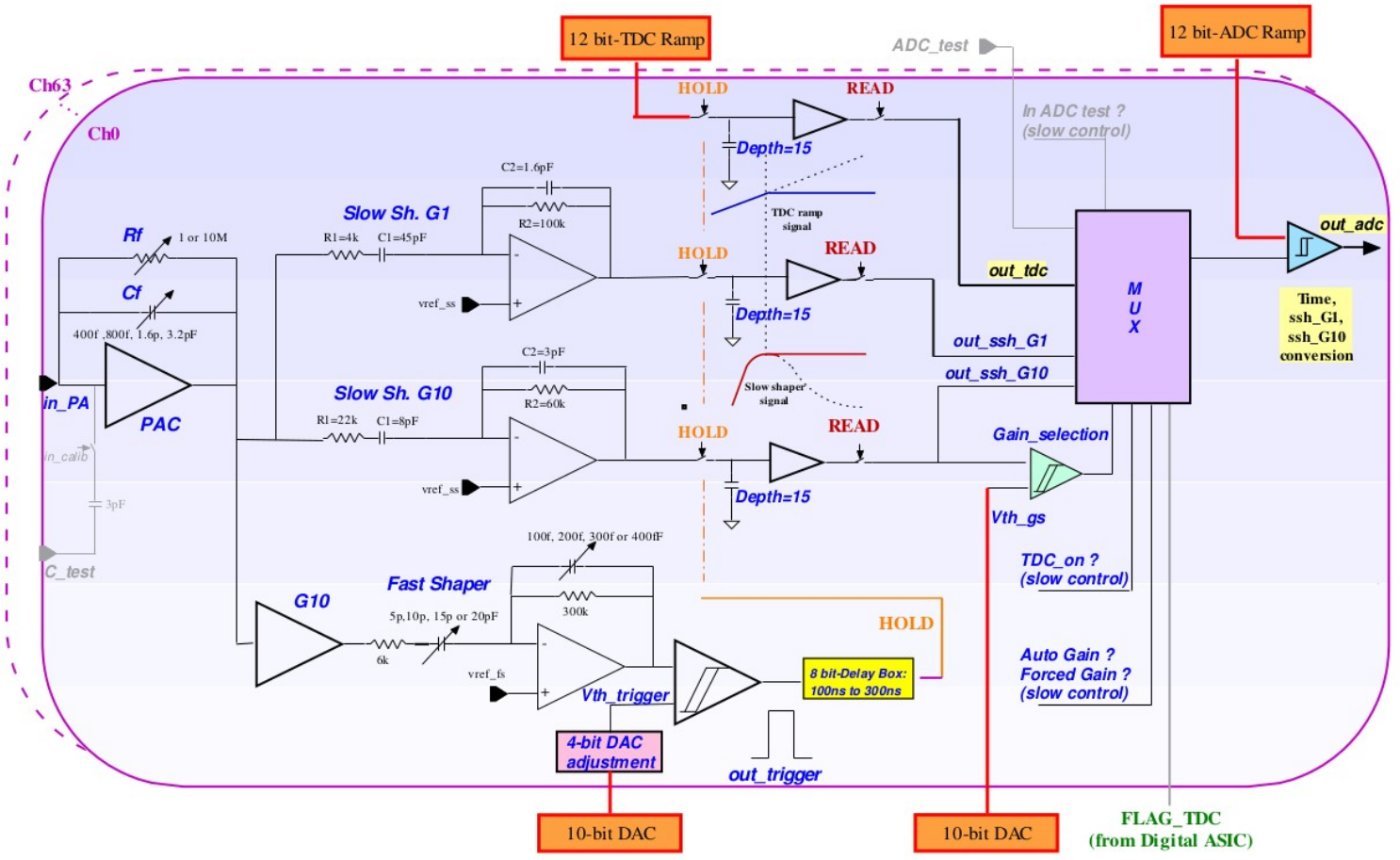


Figure 3 – SKIROC2: analog part simplified scheme

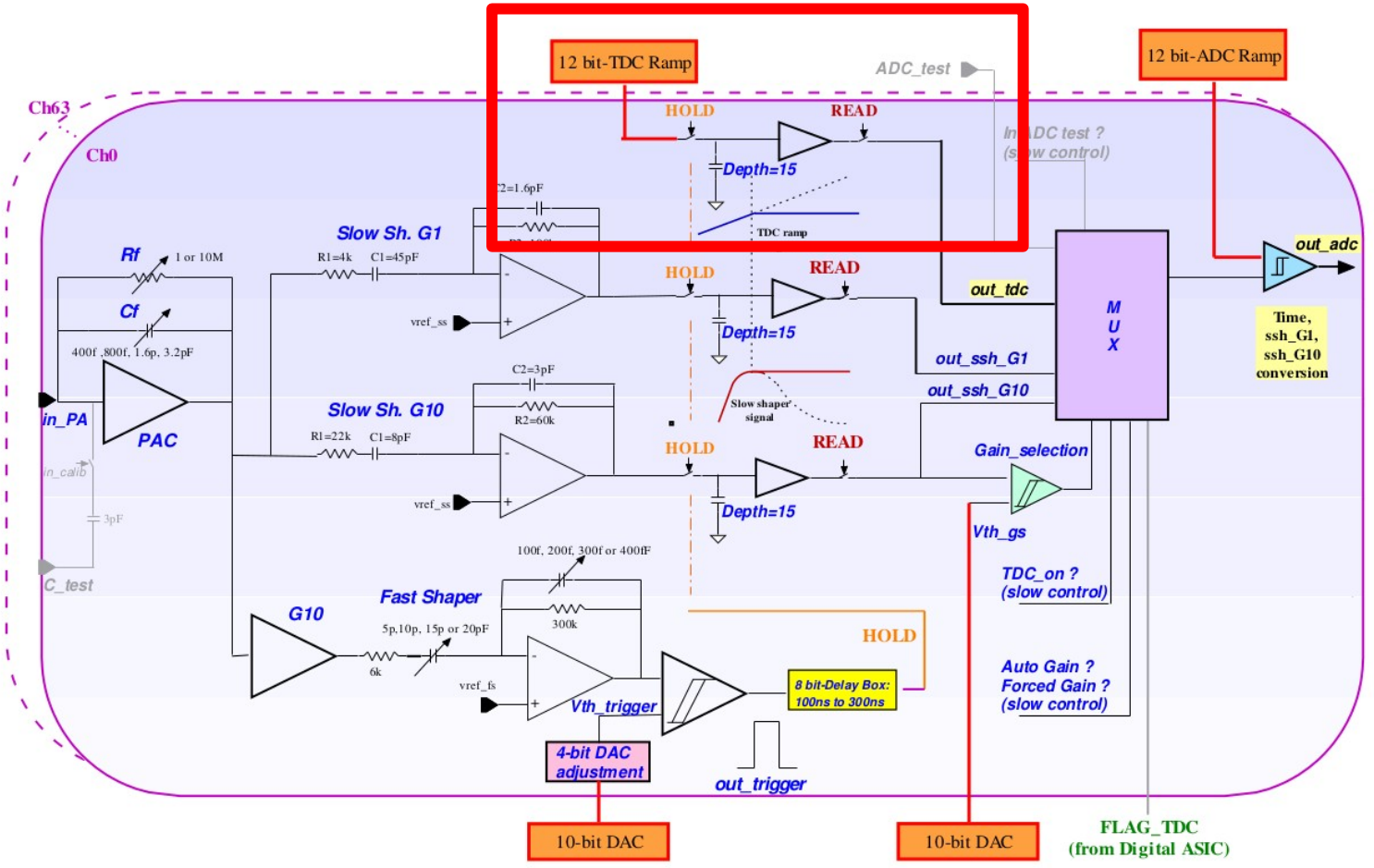


Figure 3 – SKIROC2: analog part simplified scheme

SK2a

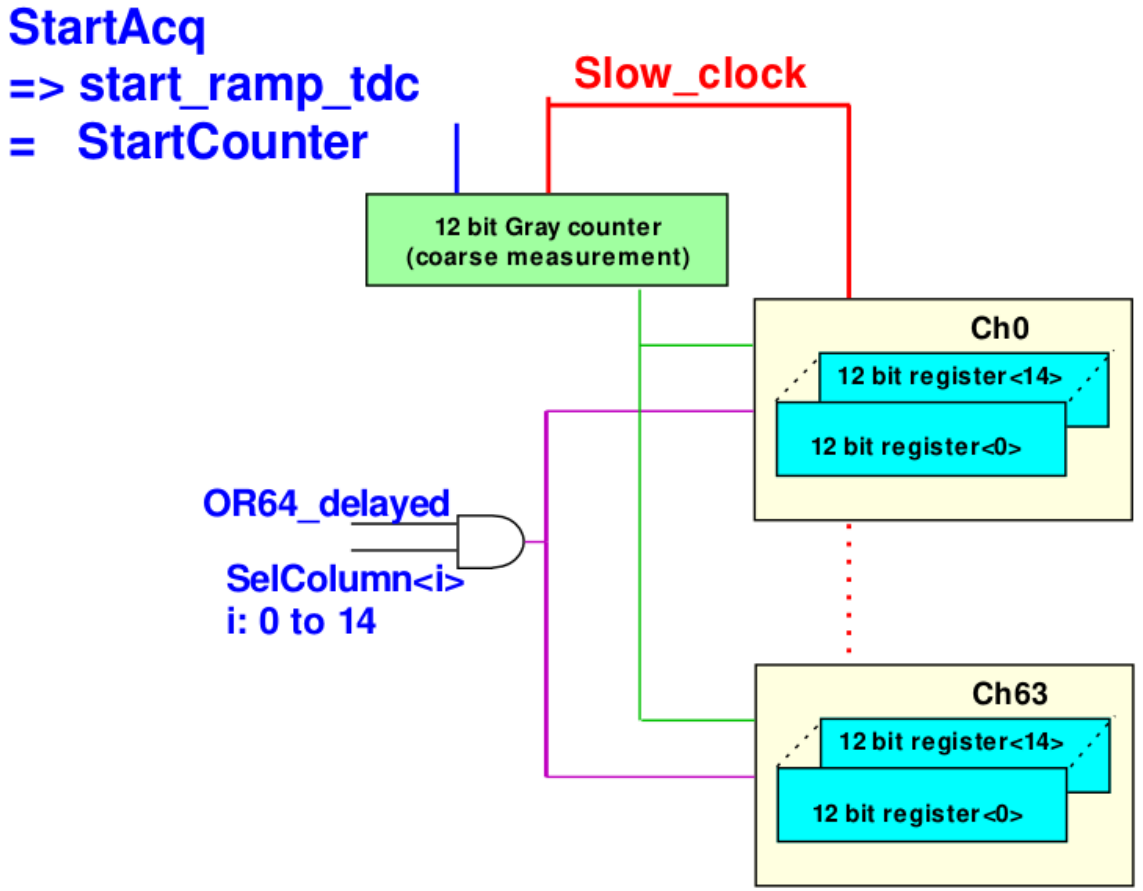
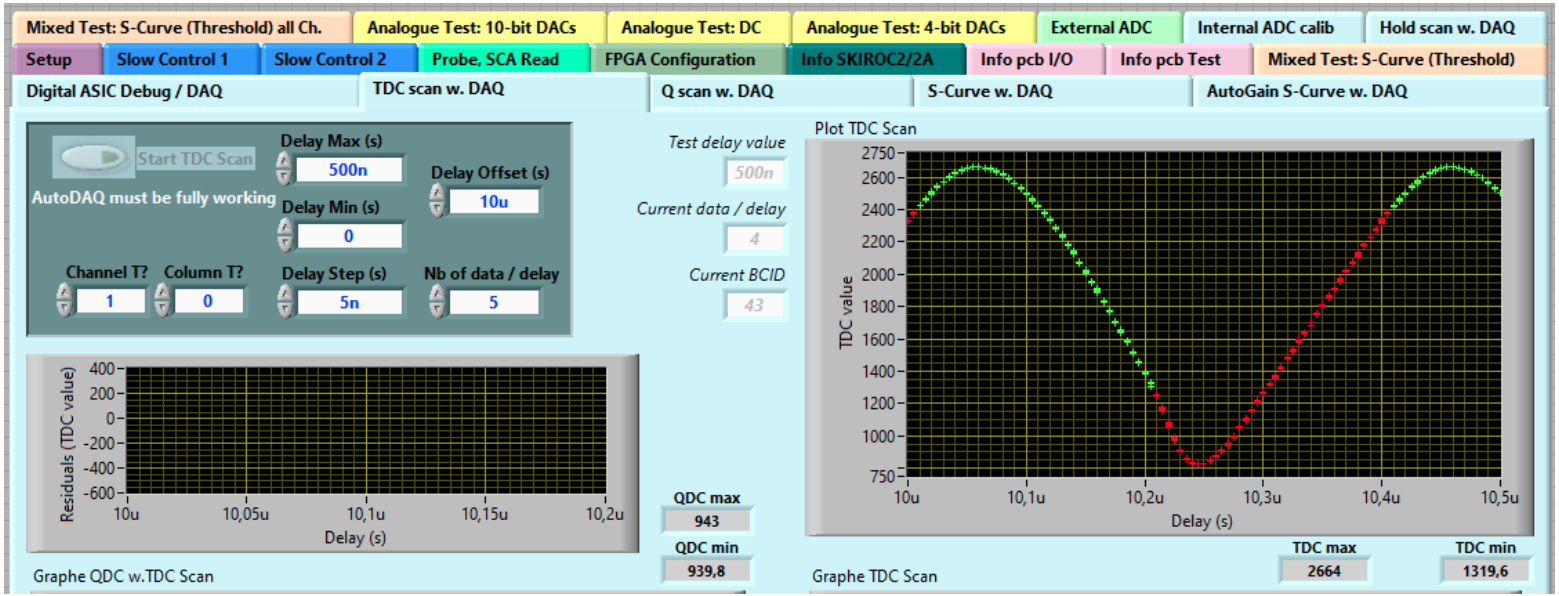


Figure 14 – Coarse measurement

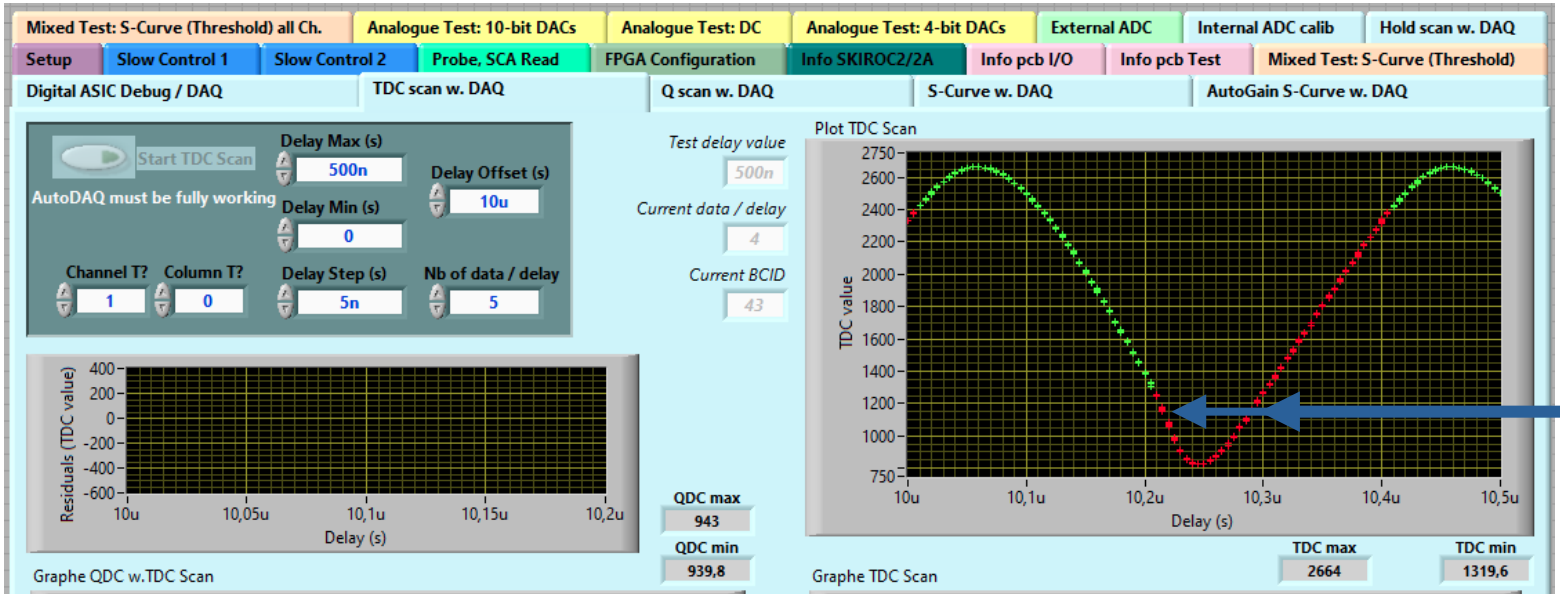
- Slow clock 5Mhz
  - 200ns
- Two ramps
  - For odd / even bcid

Sk2a



- In the default configuration the TDC gives **ambiguous readings**
- **Green / red = odd / even**
- **Dynamic range of ~1900 TDC counts**
- Tests done by S. Callier using a SK2/2a testboard

Sk2a



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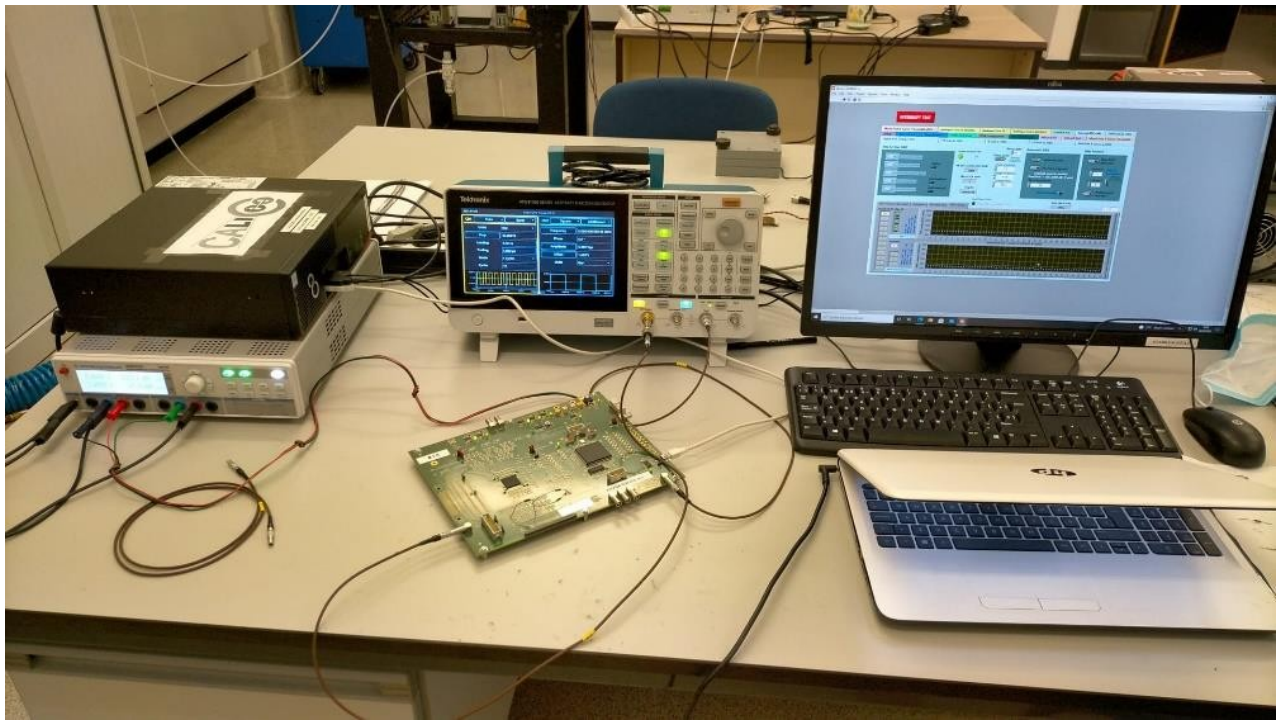
Measurements at IFIC

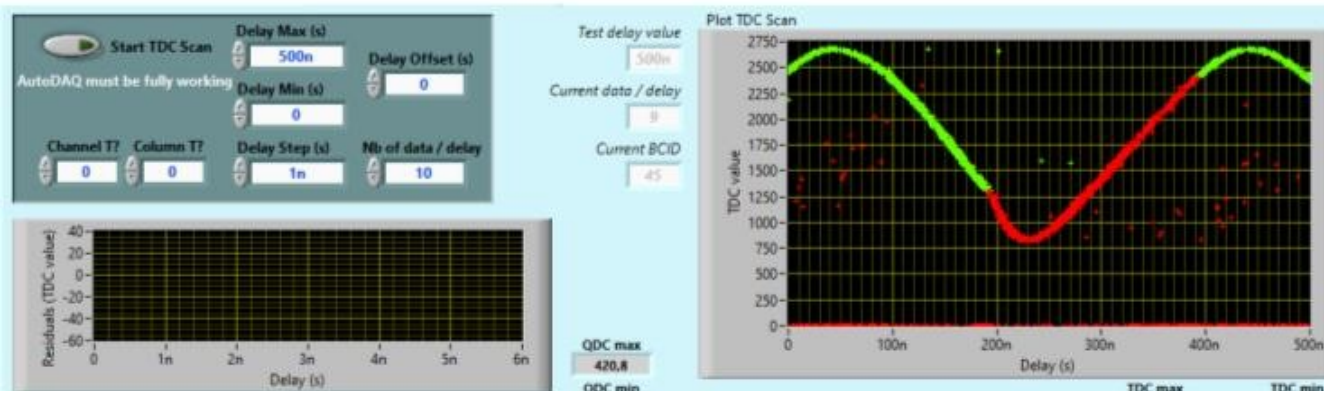
Studies at IFIC

- Omega borrow (and sold afterwards) a SK2a testboard
- Jaume Navarro joined AITANA group for a 2 months internship
  - From ETSE (engieering school of UV)



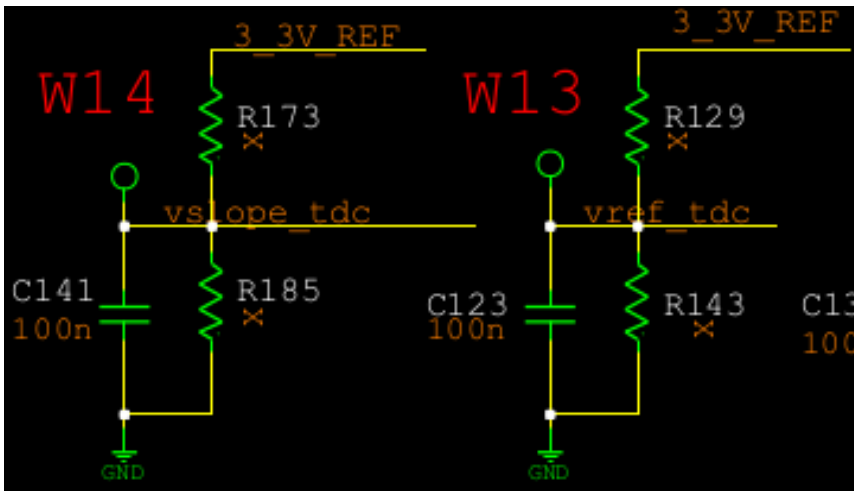
TDC tests at IFIC

- We first prepare the setup
  - The board and the instructions are “physicist-proof” and we managed with only little help from S. Callier
- Jaume learned how to use the setup (and added some modifications to use a different pulse generator)
- First step: repeat Stephane’s measurements.
- Jaume tested that the results were the same for different conditions:
  - Different channels, sca,
  - Different pulse size (from ~1 to ~10MIPs)



TDC tests at IFIC

- To optimize the TDC measurement, Stephane proposed to play with the physical configuration of the TDC in the SK2a




```
ib_curtdc : 150k to GND
ib_tdc_up : 10k to GND
ib_tdc_down : 8k to GND
vref_tdc_down : 1k to VBG, 60k to GND = (2,45V)
vref_tdc_up : 24k to VBG, 26k to GND = (1,2 V)
vslope_tdc : 6k to VBG, 19k to GND = (0,6 V)
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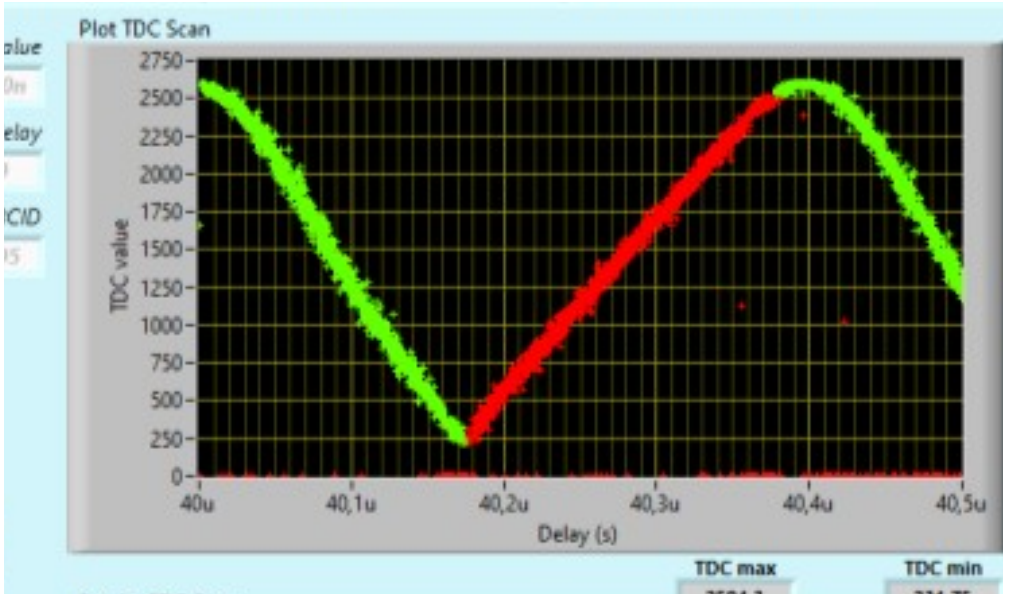
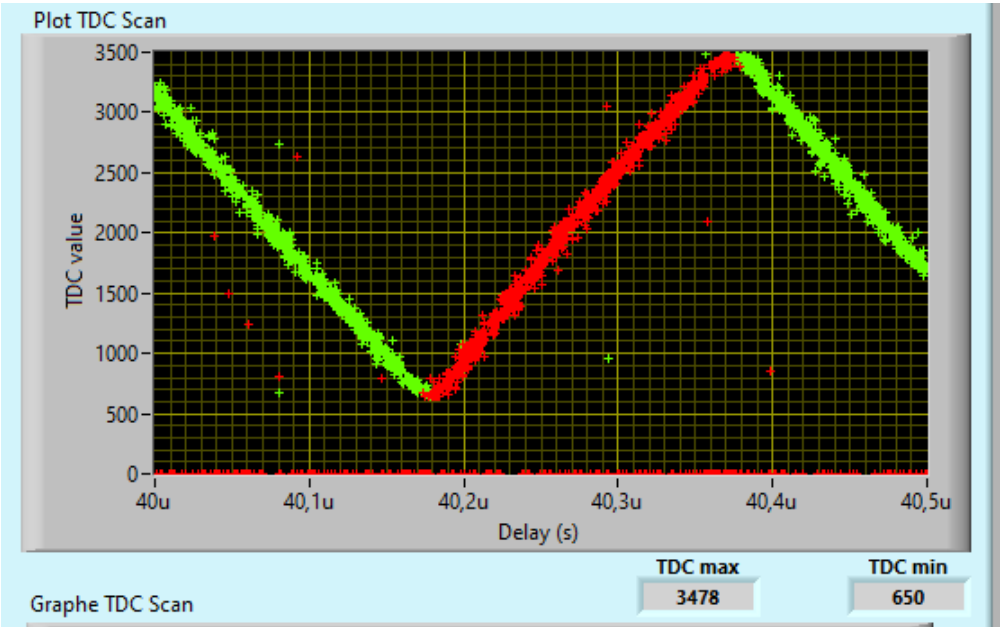
- We did a systematic study varying the resistance of the different circuits
  - Using the “hole-through” old-fashioned resistances that we found in a dusty closet at IFIC

TDC optimization (solution 1)





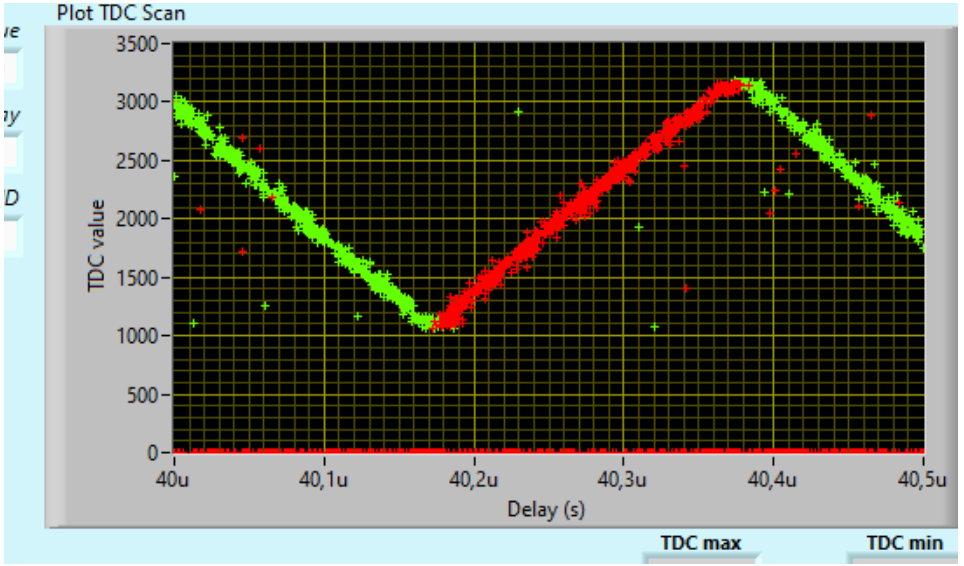
Vref_TDC_up=11k (to VBG)
Vref_TDC_down=56k(GND)

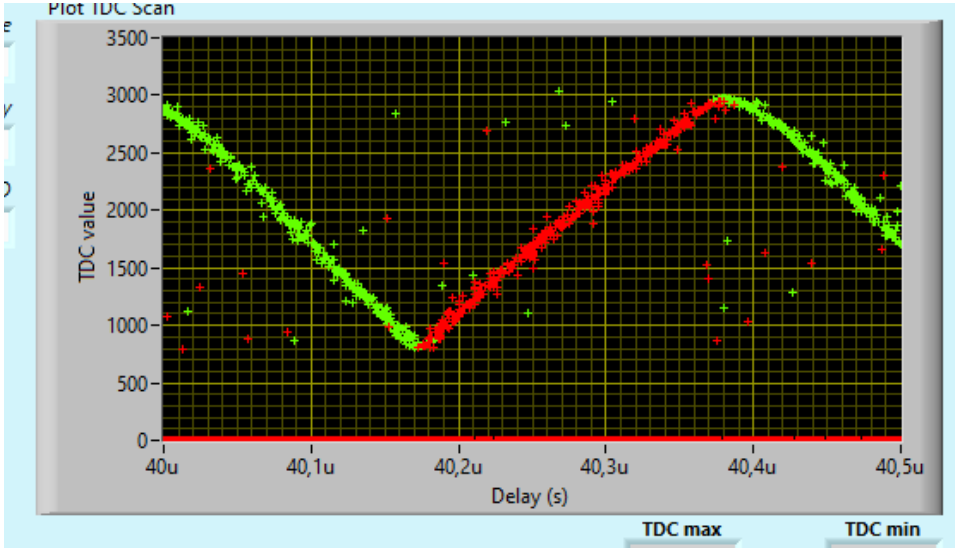
Dynamic range of ~2250 counts

Vref_TDC_UP=11K(TO VBG),
Vref_TDC_DOWN=56K(to GND),
Ib_TDC_UP=15K

Dynamic range of ~2800 counts

TDC optimization (solution 2)





Vref_tdc_up=11k VBG,
vref_tdc_down=56k TO GND,
vslope_tdc=15k TO GND

Dynamic range of ~2000 counts

Vref_tdc_up=11k VBG,
vref_tdc_down=56k GND,
vslope_tdc=39k GND

Dynamic range of ~2000 counts

Summary

- We found a couple of sets of configurations that solve the ambiguity in the TDC measurement
- Done in the SK2a testboard
- Not possible in the CHIPS already in the existing slabs
- But foreseen in the new FEV2.0 design (see next talk by Jerome)