Status of electronics development for new long SLAB

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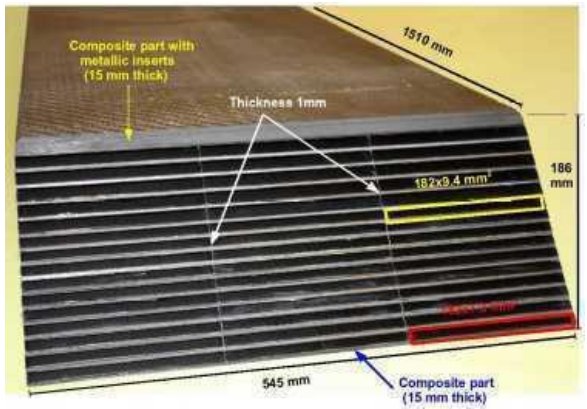
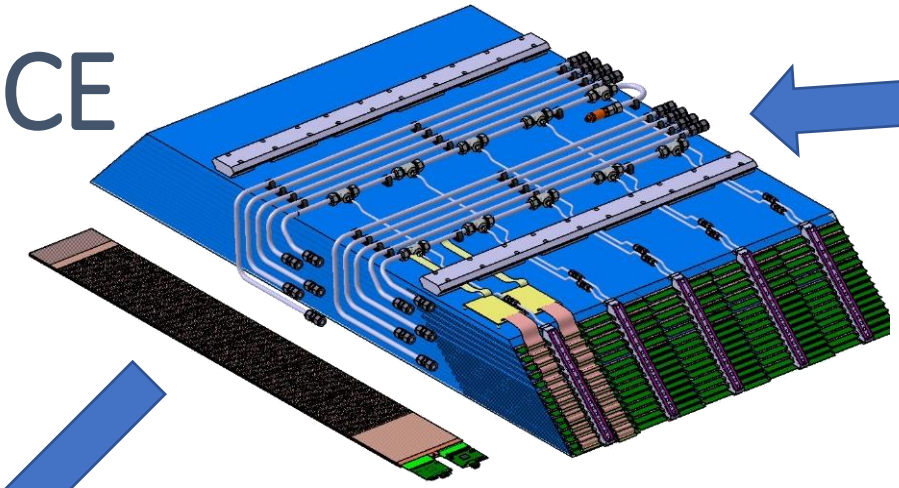
CALICE WEEK 8-10 September 2021

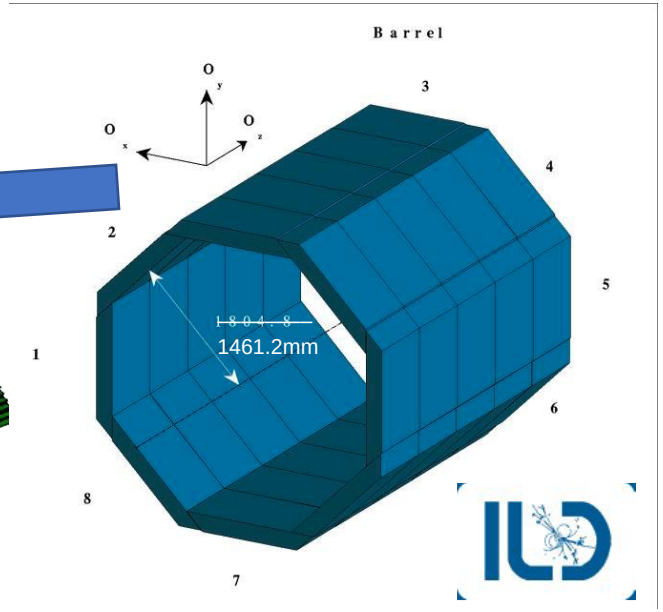
Previously in CALICE



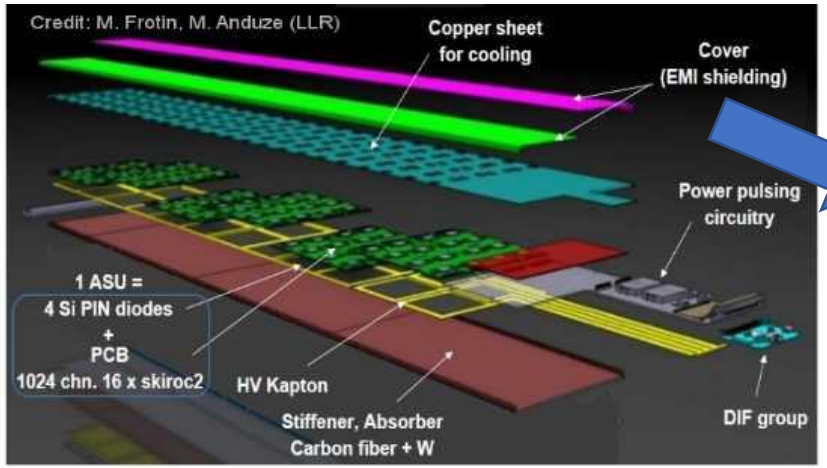
(13-15 double layers)



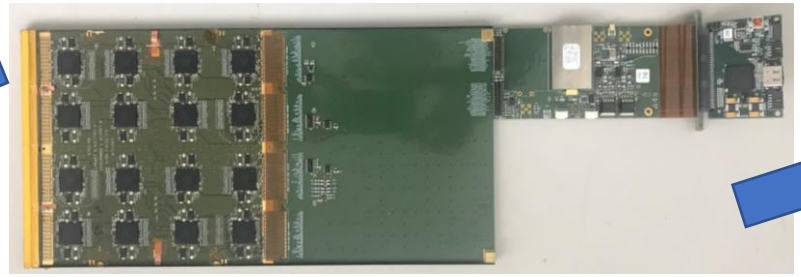
Module (5 columns x 13-15 alveoli)
Double long slab per alveolus



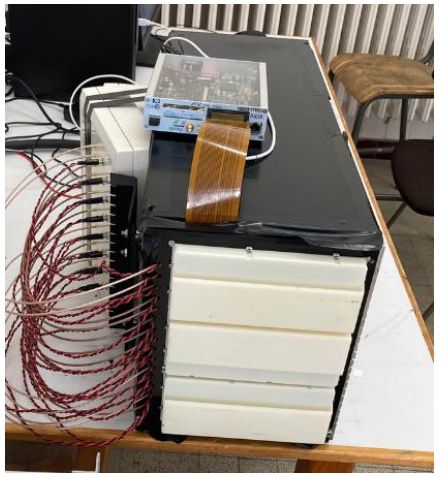
ILD & SiW-ECAL barrel
(8x5 modules)



Assembly of long SLAB (8-12 boards)



Short SLAB (4 x 6'' wafers)

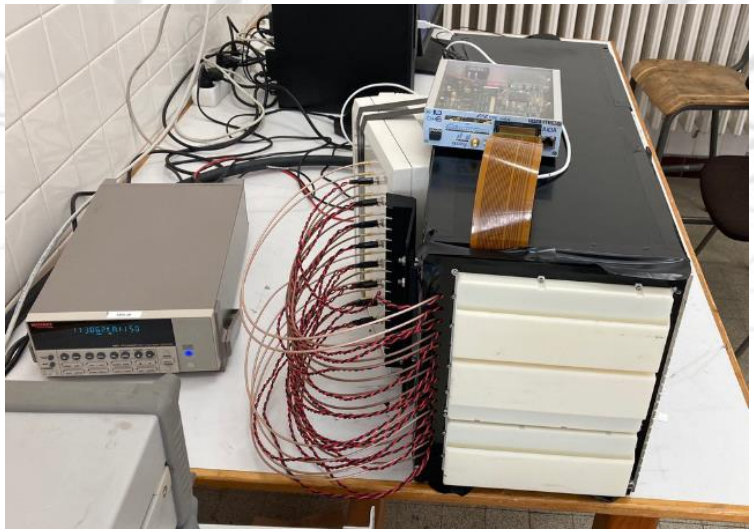


SiW-ECAL prototype (15 layers)

Status of electronics

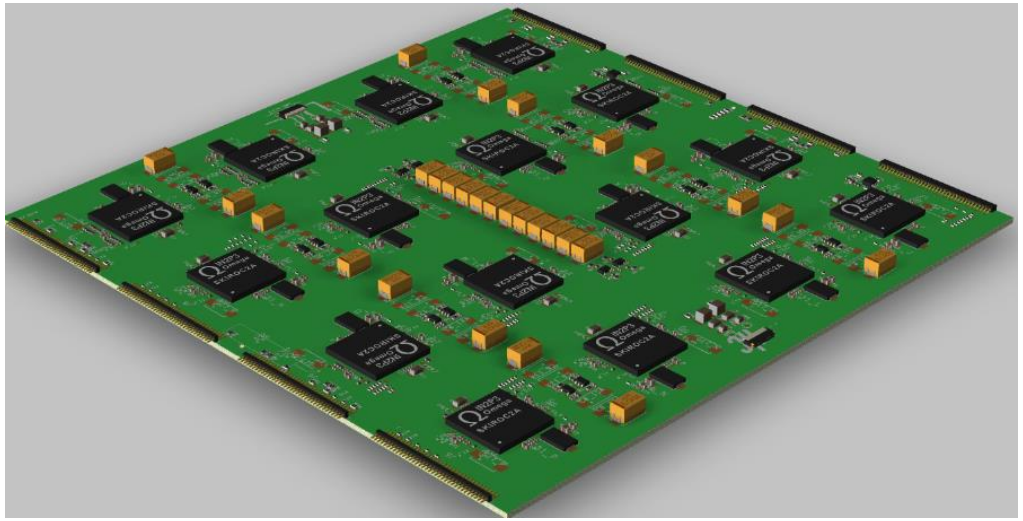
- Ready since 2 years for beam test with 15 layers in the same stack.
- New DAQ from IJCLab
- Design electrical long SLAB
  - LV power supply voltage drop
  - HV connection need to be redesign for reliability
  - Measure MIP with 4x4 pixels wafer per board

→ Need new front-end board



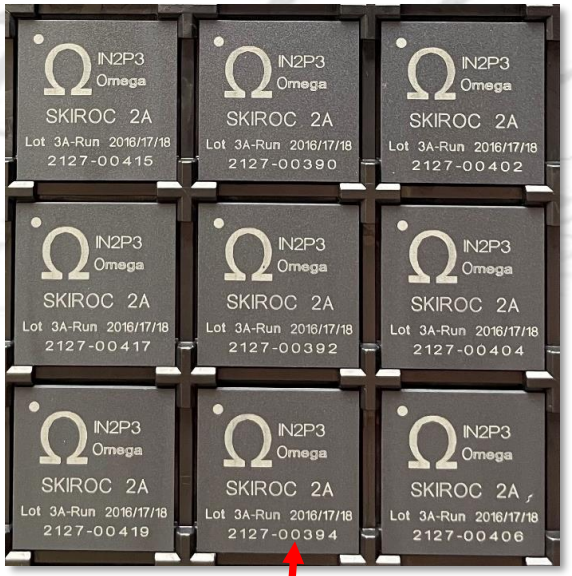
Design new front-end board (FEV2.0)

- Dedicated and designed for long SLAB
- Upgrade LV power distribution
  - 1 analog LDO per chip
  - 1 digital LDO per 4 chips
  - Optimize capacitance for power-pulsing
- Upgrade buffer for slowcontrol
- Change HV distribution for wafer
  - Add HV filter per wafer
  - FEV drive HV instead of kapton
- New HV kapton
  - 1 per FEV instead of 1 per SLAB



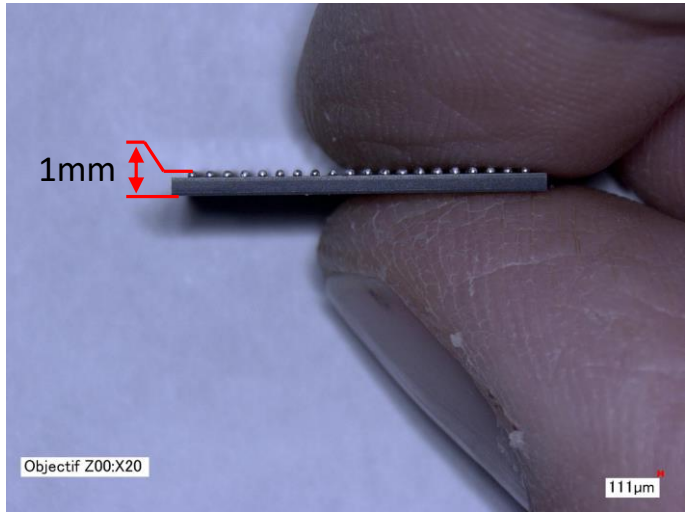
PCB must be receive in September, but 1st test probably delayed due to international shortage component

New packager for SKIROC2A (NCAP)



Unique ID per chip

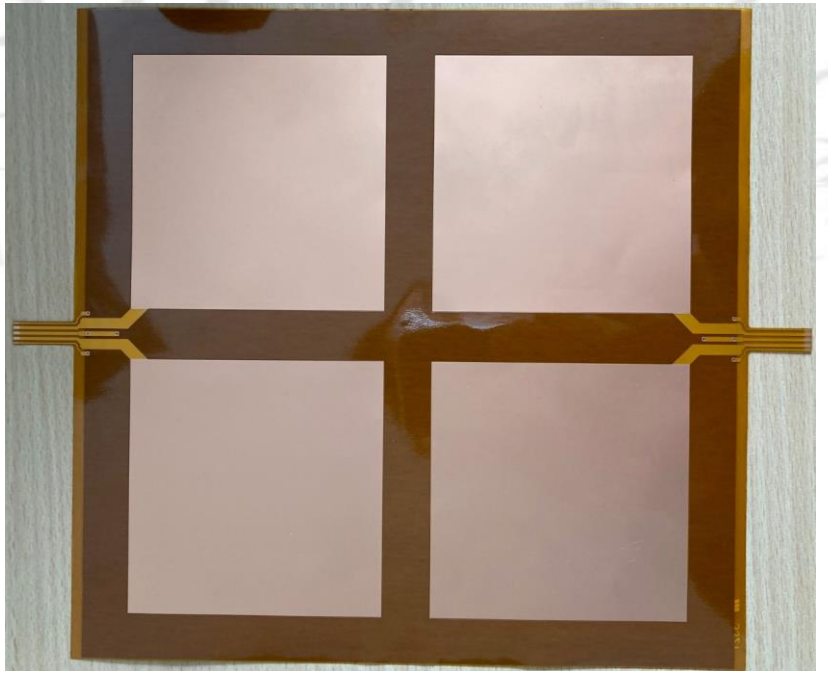
- Previous company stop BGA activities
- Found Chinese company NCAP
  - 390 chips packaged
  - First results are good
- Need few weeks of tests
  - Functional tests
  - DAC/ADC linearity
  - Scurves (trigger vs hit)
  - 10 minutes / chip



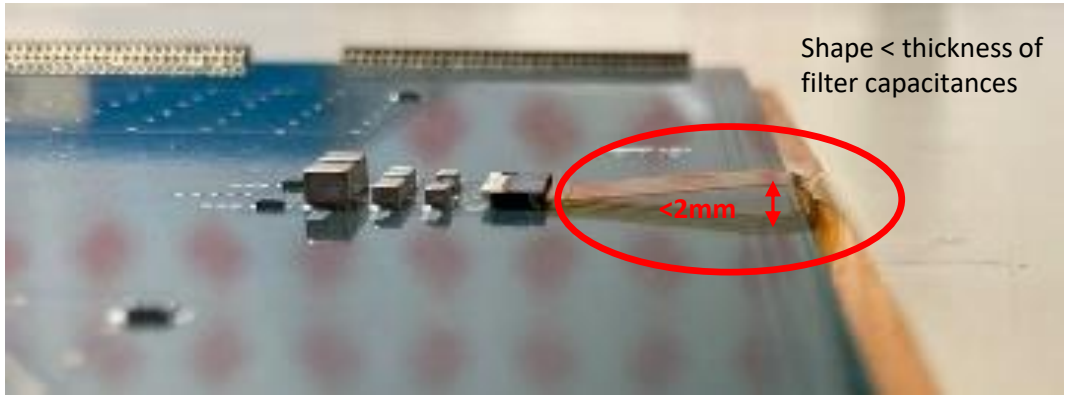
- Thanks to Stephane (Omega) for his future new Labview interface to evaluate SKIROC2A performances with Omega test board

Design new HV kapton

- Before: one kapton for 10 board
  - Difficult and expensive solution
  - Glue 40 wafers on single kapton
  - Not compatible with FEV interconnexion connector



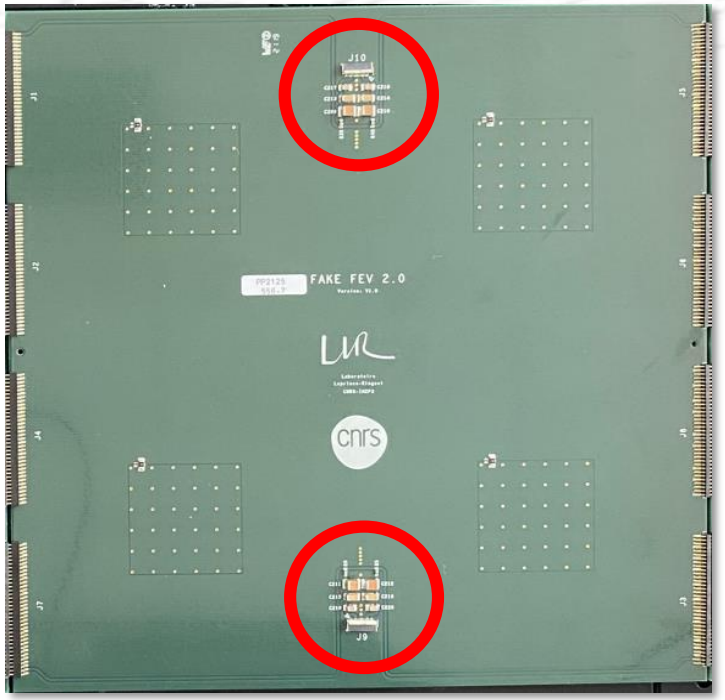
- New solution:
  - 1 kapton per front-end board
  - Easier to insert/replace in long SLAB
  - Higher wafer protection (handling)
  - HV propagate through FEV connector + filter to wafers



Design fake front-end board

- Goal: study HV distribution and mechanical assembly
  - Only HV filter, connectors and interconnexions are mounted
- Measure leakage current function of number of boards with and without wafer
  - I(V): current fct (HV)
  - I(s): current fct (time) @ 200V

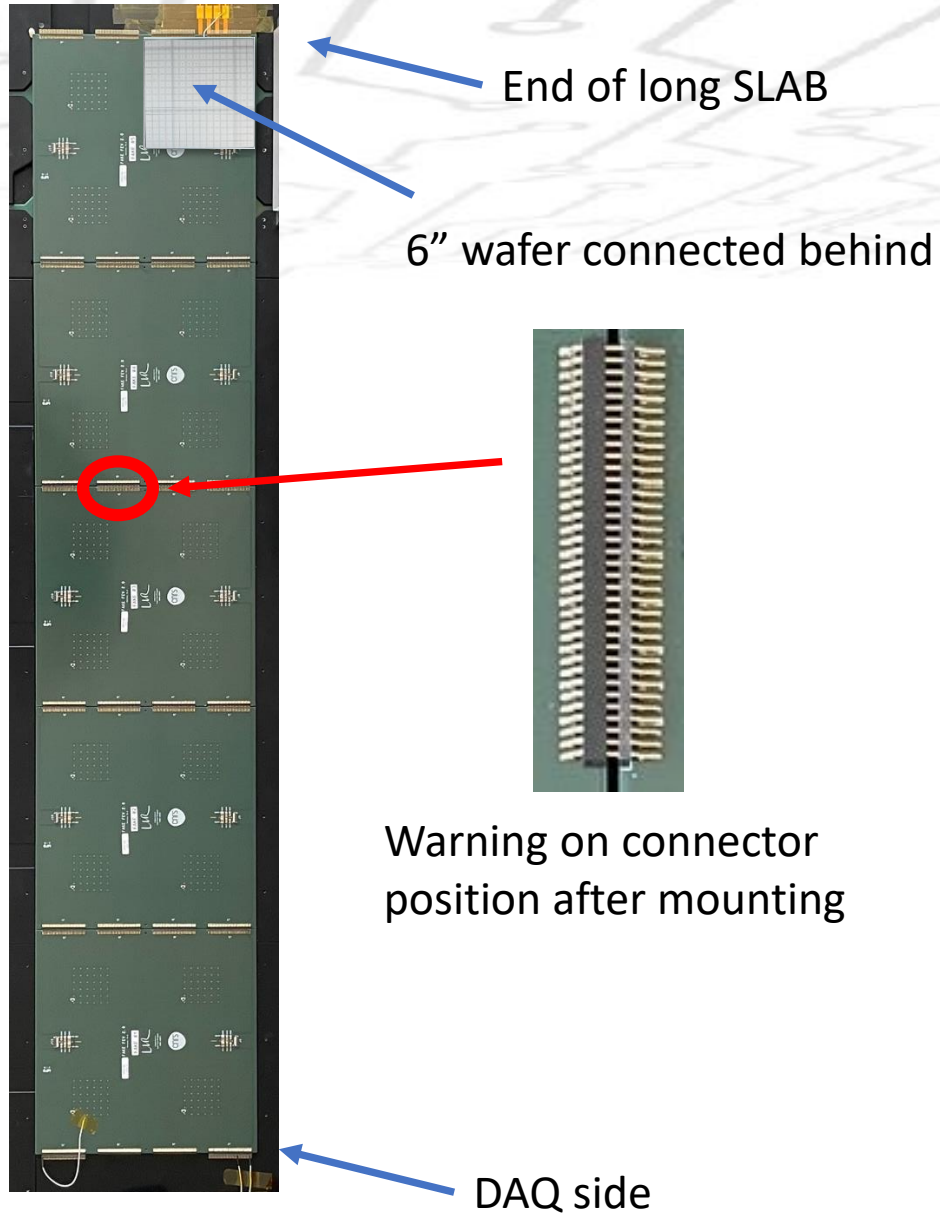
HV filter + connector



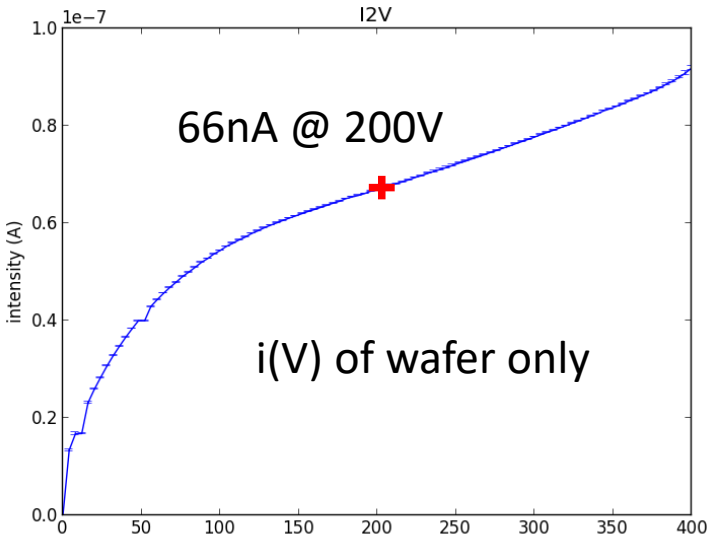
Fake FEV is composed by only 2 layers
It's very different compare to 10 layers of FEV2.0

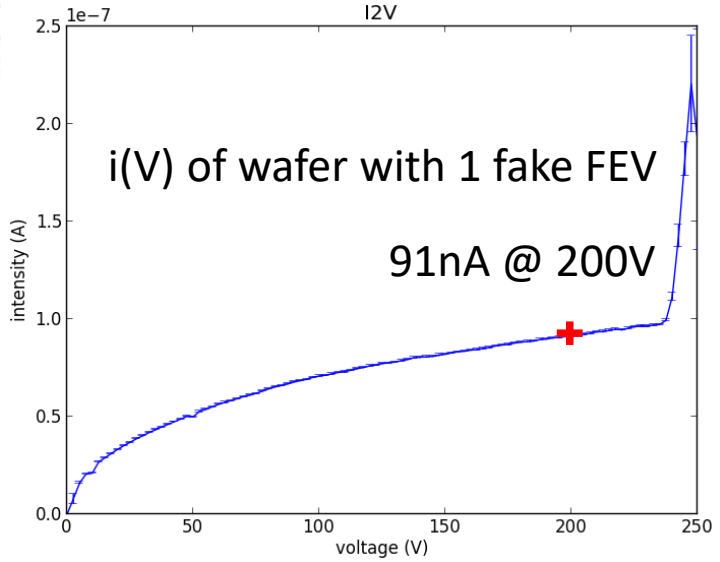
Status on fake long SLAB

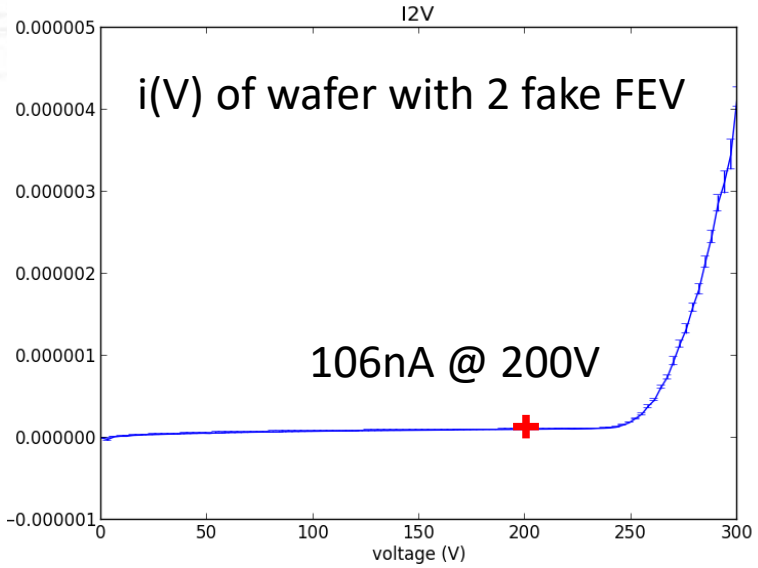
- Succeed to connect 5 fake FEV
  - Difficulties to plug 2 boards (3N / contact)
  - Need mechanic solution to plug/unplug boards
- New kapton is not used (wafer must be glued)
- Leakage current feel increase with number of front-end board connected.
- Need to study leakage current due to PCB himself.

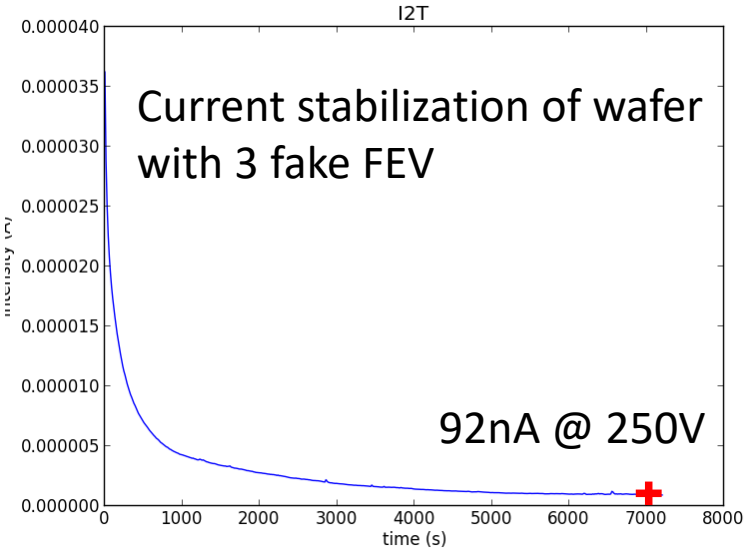


Preliminary HV results on fake long SLAB



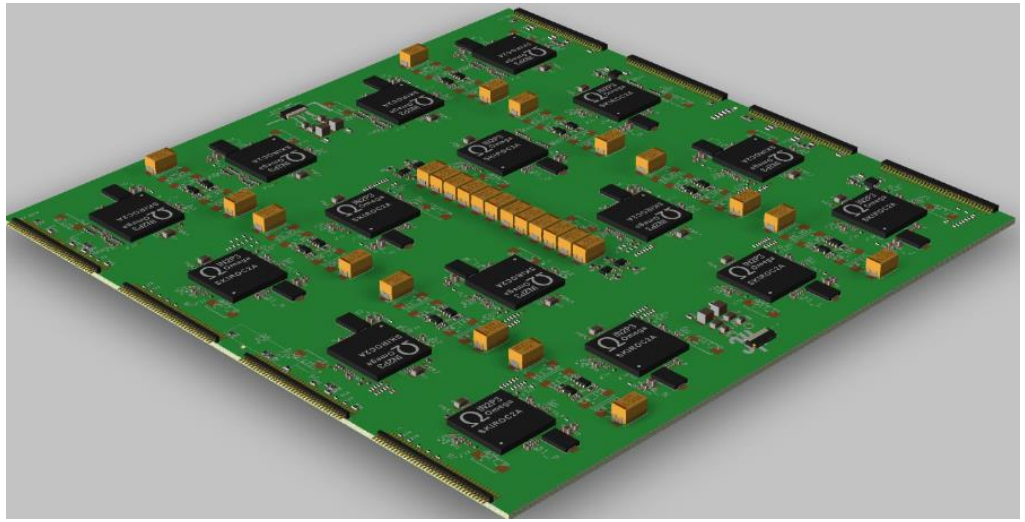






- **Many different measure from 1 to 5 chained boards but with different parameters.**
- Parameters must be uniformed to conclude something
  - Stabilisation time duration: 5h @ 200V
  - Voltage dynamic: 0-250V with 100 steps
- Need measure with FEV12 to compare leakage current and set HV level

Conclusion / perspectives



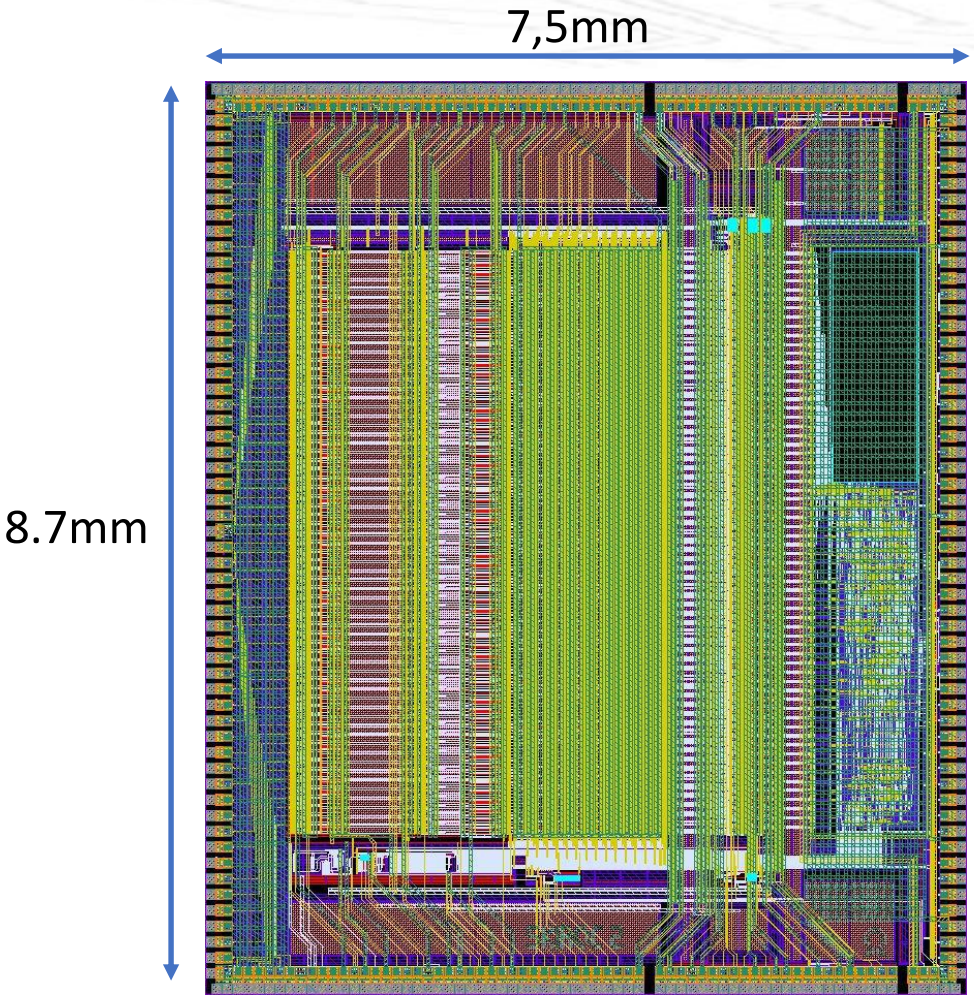
- New front-end board
  - New LV power-pulsing design
  - New LV connectors
  - New HV design
- Reception of new kapton HV and new SKIROC2A in August

- September: reception of new front-end board
  mount components (if available)
- October: start test of SKIROC2A
- November: beam test @DESY (2 weeks)
- 2022: gluing wafer
  start long slab assembly and calibration

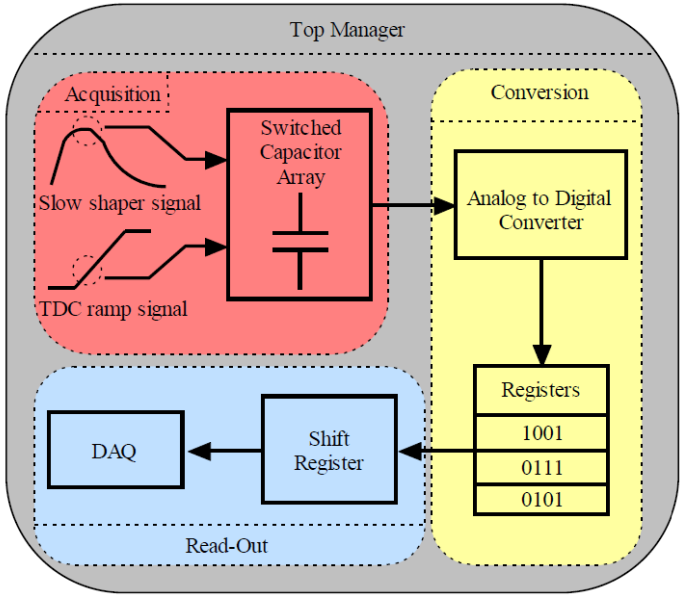
Thanks for your attention

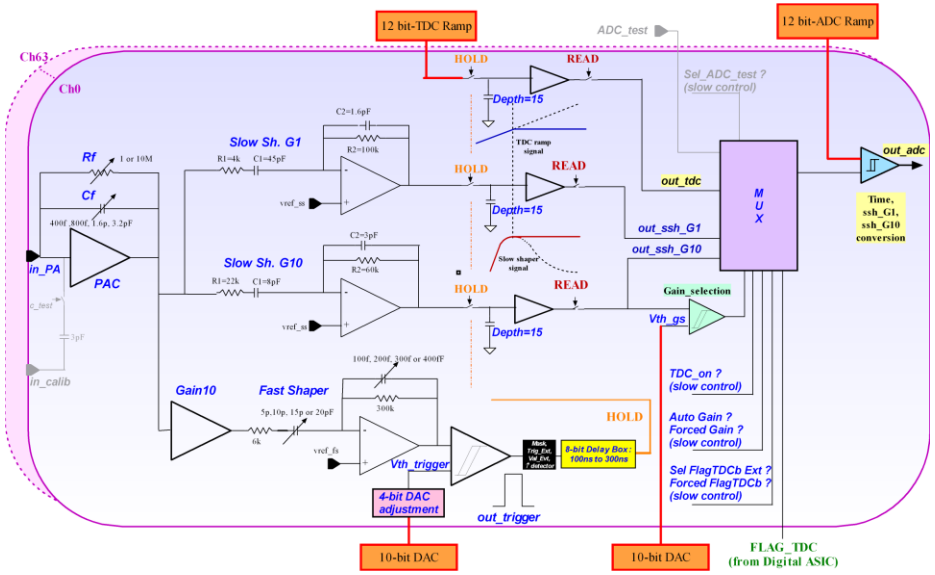
BACKUP SLIDES

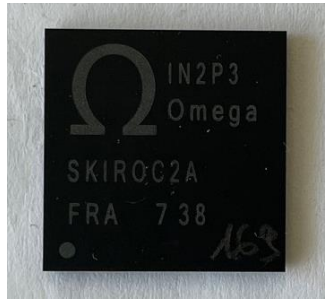
Readout chip Omega SKIROC 2A



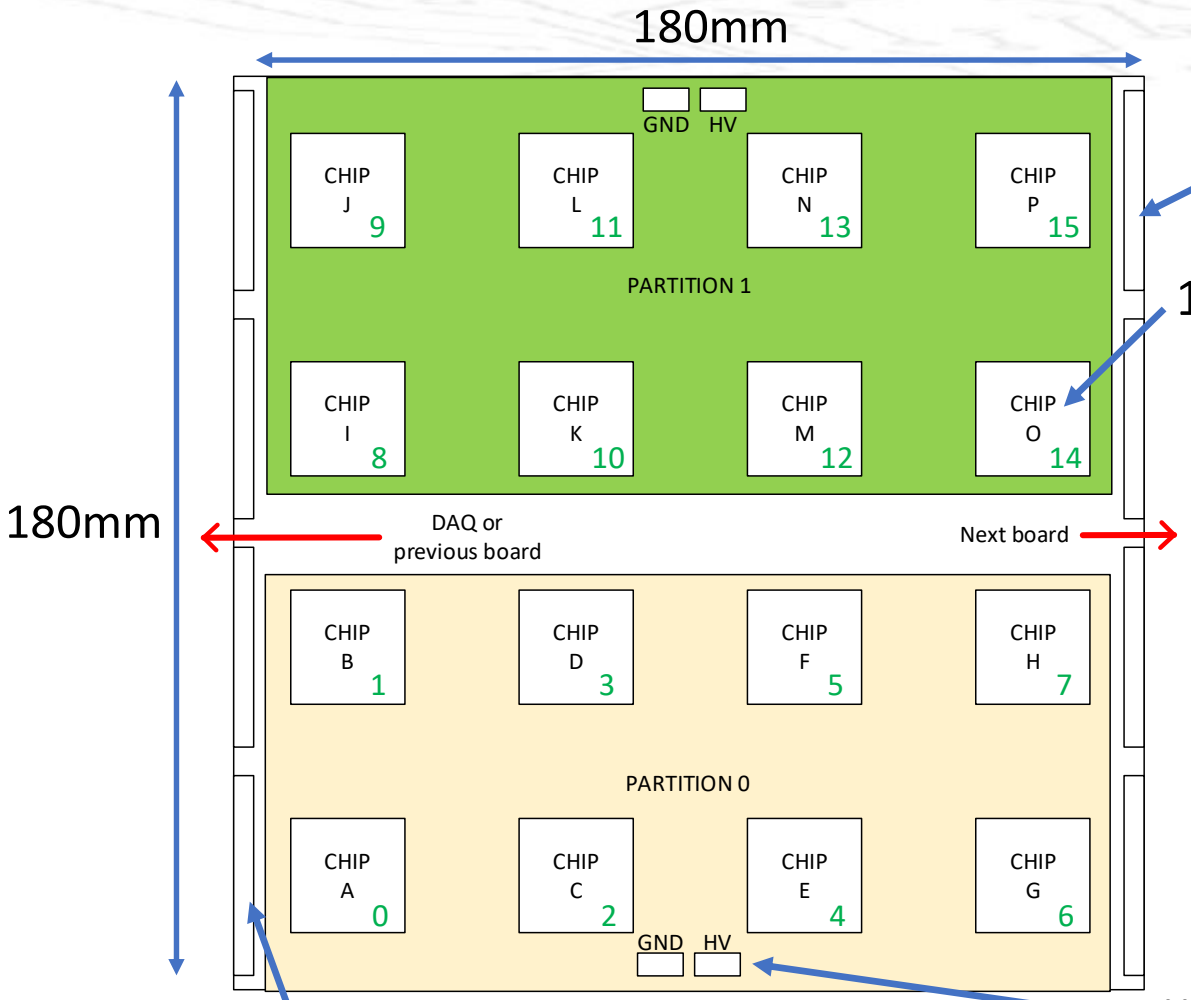
Chip 64 channels
Technology AMS 0,35µm
Large dynamic: 2fC up to 10pC
Very low noise: 0.4fC
Analog memory depth: 15
Full power pulsing







Board synoptic



4x 35 pins female connector

Gradconn BB02-WF352-K03-000000

16 chips Omega SK2A

2 partitions for slowcontrol and data flow.

→ Could be link or bypass with 0Ω resistor

→ Test mode for 1 chip only per partition

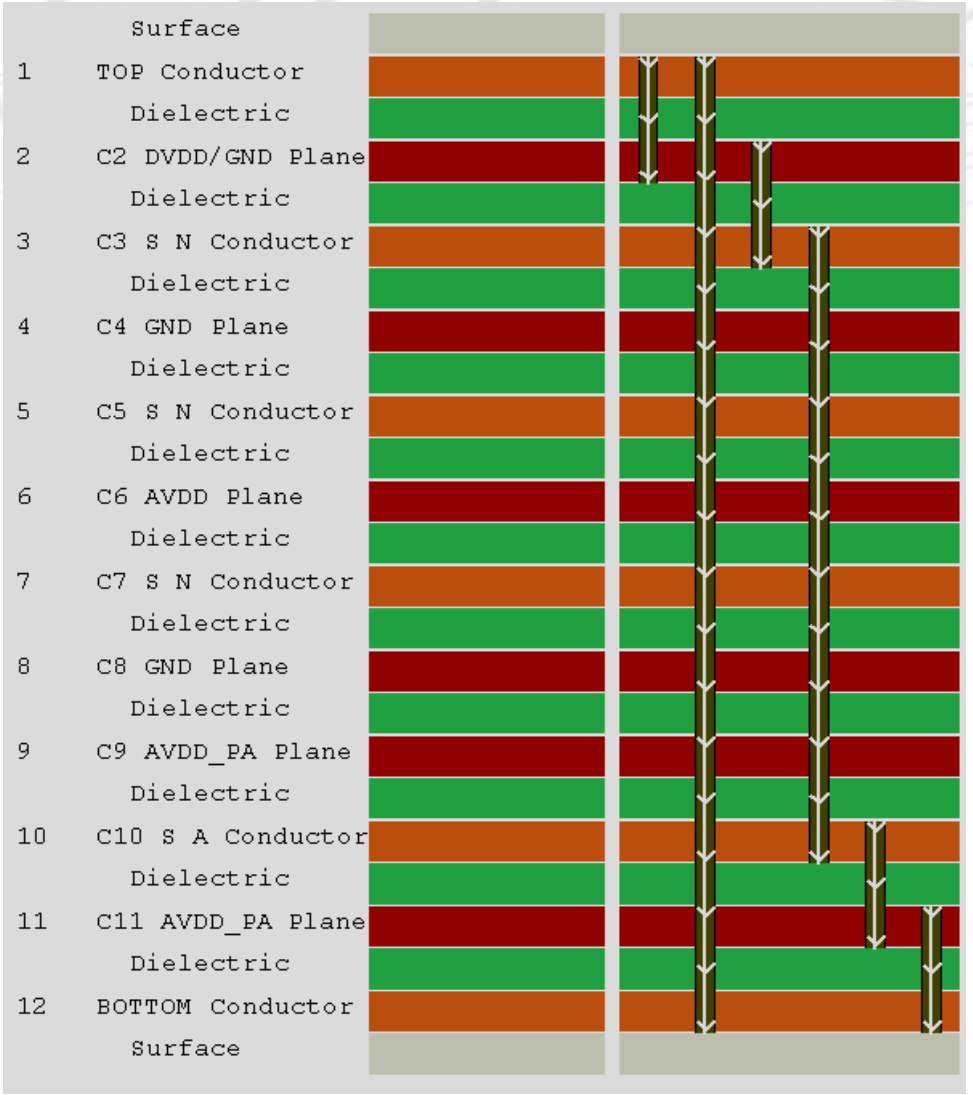
4x 35 pins male connector

Antelec AM1C100352GCMSH1BA

High voltage pad for wafer with kapton connection

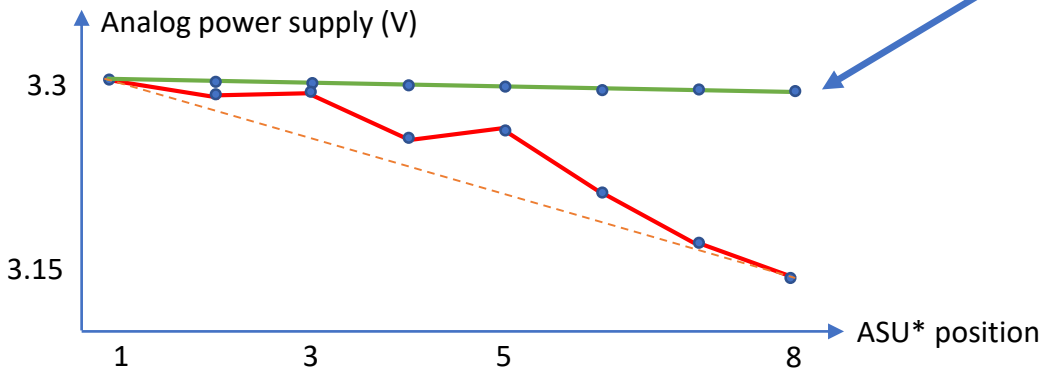
Stack-up board

- Keep layer for power
  - 2 x GND
  - 2 x AVDD_PA
  - 1 x AVDD
  - 1 x DVDD
- Minimize crosstalk
- Keep shielding mush as possible
  - AVDD_PA for preamplifier signals
  - GND for analog and digital signals
- Move away digital from preamplifier line
- Adaptation lines
  - 50Ω for single ended
  - 100Ω for ddifferential lines

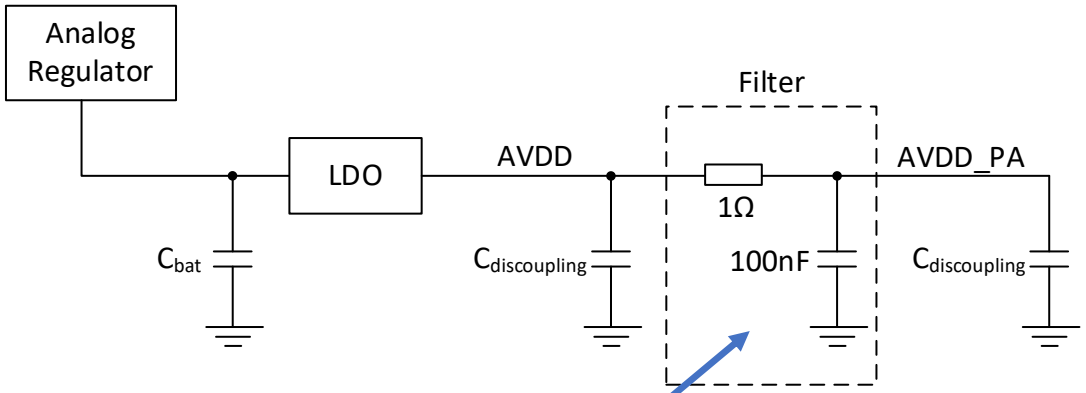


Power distribution

Expected results



ASU* (Active Sensor Unit)



Add filter to generate local preamplifier power supply

In the electrical long SLAB, 8 boards are chained. Regulator upstream produce analog 3.3V for all chips of all boards.

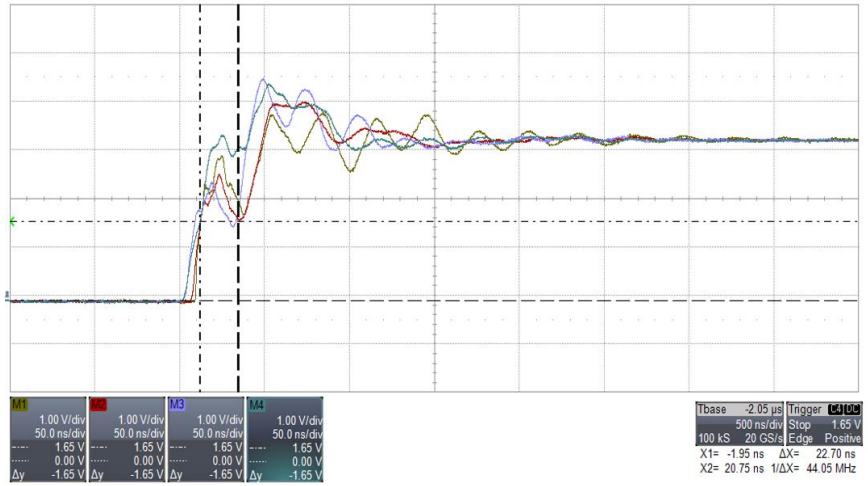
Due to resistivity of layer per board on analog 3.3V, we measure voltage drop along the long SLAB coupled with bandgap distribution.

→ We decide to generate local power supply with LDO (Low Drop Out) to cancel voltage drop.

Configuration lines (1/2)

In the electrical long SLAB, we have some difficulties to configure more than 4 boards. Configuration clock line is not design for variable number of boards chained.

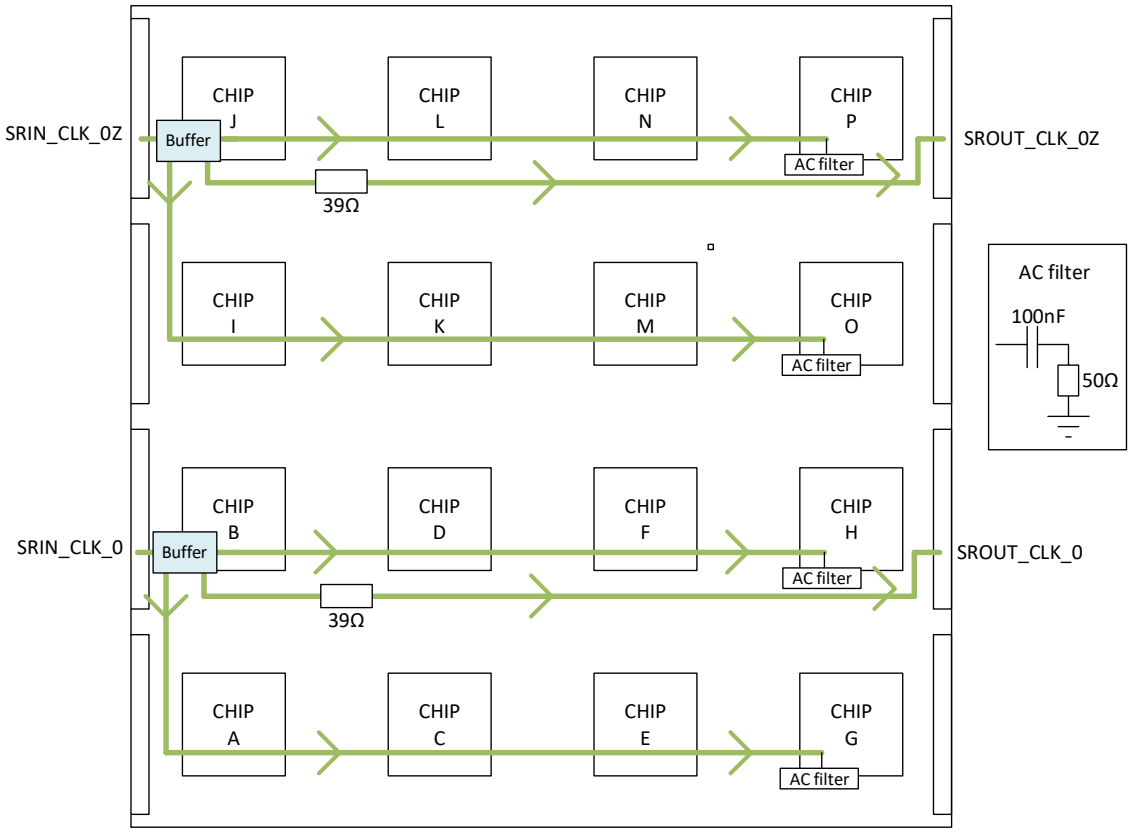
→ Only 1 buffer upstream drive all readout chips, not adapted for variable wire length.



→ Need long studies to find solution with hardware

- Make simulations with Sigrity
- Place filter to shift the reflection effect on the configuration clock

Configuration lines (2/2)



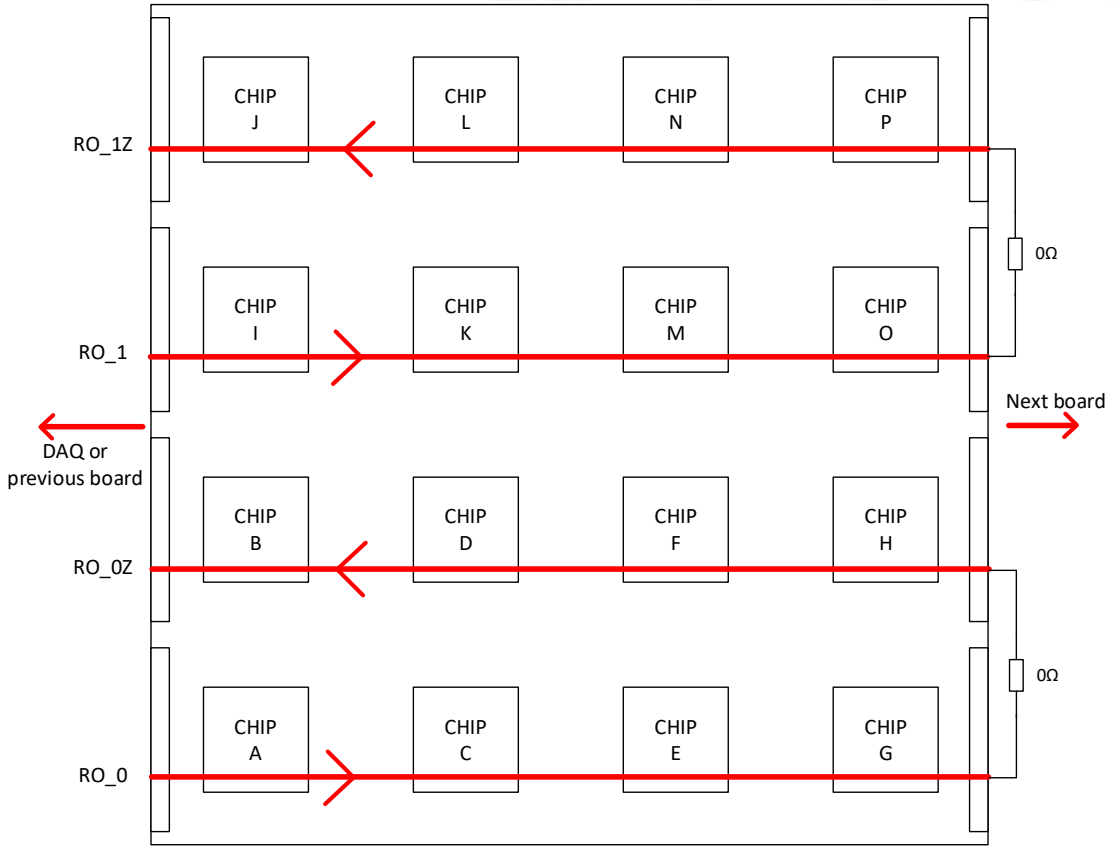
Need system to reduce length of clock line and load capacitors.

→ Add buffer or logic gates, dedicated per local partition and for next board

→ Add AC filter to reduce reflection effect on each partition.

→ Configuration clock is drawing to limit stub and reflection

Data lines



Each chip is chained in coil per partition.

Omega SK2A chips are not able to drive signal on 180 cm (10 boards).

Possibility to bypass chip if necessary with slowcontrol or shunt resistors.

→ The last chip of each partition must be the closest of DAQ.

→ Board is divided in 2 partitions to reduce readout time


The End