SiW-ECAL 15 Slabs Commissioning

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Affiliation:



In collaboration with:







Introduction

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Introduction

SiW ECAL

- Technological option for ILD ECAL.
- Optimized for Particle Flow Algorithm
- Requirements from ILD
 - High granurality
 - Compactness
- Absorber
 - Tungsten
 - X0 = 0.35 cm
 - Rm = 0.93 cm
 - λl = 9.946 cm

940

Detector SLAB

- Active material
 - Silicon





Introduction



SiW ECAL

- Each slabs are equipped with 4x4 **Skirocs** as **analog** readout units, along with a **SL board** as a **digital** readout unit.
- Si Wafers are equipped at the back of the layer.
 - \circ size: 9x9 cm², thickness: 500, 320 μ m
 - pixel size: 5x5 mm²
 - 4 of them are equipped at back of the slab.
- Number of channels
 - 16 skirocs x 64 channels x 15 layers
 - = 15,360 channels







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Introduction



- 5 layers were added to the stack \rightarrow Making it **15 in total.** (That's half of number of layers of actual ILD)
- Newly added layers contain skiroc2a, which enables us to tick channel thresholds.
- The density between the layers are realistic compared to the actual detector implementation at ILD.







Timeline for preparing the beam test



Status of Each Layers



								-		
coreKapton slot	Layer position	Slab ID	ASU type	wafer	front end (slboard ID)	Glissiere neded for the W	W in front (mm)	X0	X0 (acc)	Comments/Issues
14	0	31	FEV12	500						
13	1	30	FEV12	500						
12	2	13	FEV11	320	10	2.1mm	2.1	0.6	0.6	
11	3	14	FEV11	320	5	2.1mm	2.1	0.6	1.2	
10	4	15	FEV10	320	1	2.1mm	2.1	0.6	1.8	
9	5	19	FEV11	320	13	2.1mm	2.1	0.6	2.4	
8	6	20	FEV11	320	11	2.1mm	2.1	0.6	3	
7	7	24	FEV12	500	7	2.1mm	2.1	0.6	3.6	Stable AVDD ??
6	8	21	FEV11	320	14	2.1mm	2.1	0.6	4.2	
5	9	25	FEV12	500	3	2.1mm	2.1	0.6	4.8	problems communicating the ID of the SLboard ?? (SOLVED)
4	10	22	FEV11	320	4	4.2mm	2.1	0.6	5.4	
3	11	23	FEV10	320	6	4.2mm	4.2	1.2	6.6	
2	12	16	FEV11	320	9	2.1mm	2.1	0.6	7.2	
										problems communicating the ID of the SLboard ?? (SOLVED)
1	13	17	FEV11	320	2	4.2mm	4.2	1.2	8.4	Stable consumption ??> SOLVED shorcut in DVDD (capacitance in skiroc 14)
0	14	18	FEV11	320	0	whatever (no W will be added)	4.2	1.2	9.6	

Commissioing

Procedure





Masking



Layer 0, SLAB 31





Layer 1, SLAB 30

Layer 2, SLAB 17



mask_x_y_SLB2



Scurve



- Scurve is used to estimate the optimal global threshold for each layer.
- These thresholds can be varied depending on the size of the signal that is induced.
- Plots below shows the plateau shift with different number of MIPs. (proportional to the pulse amplitude that is being injected)



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CALICO Calorimeter for ILC

Thresholds

CHANNEL -250 CHIP

threshold_chip_chn_global_2

threshold_x_y_global_2





threshold_chip_chn_global_0



threshold_x_y_global_0

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		-80	-6	50 .	-40	-20	0	20	40	60	80	220
							10.25				×	



- Signal is needed to be read along the pulse that is generated by the slow shaper. This timing is managed by trigger delay.
 - Optimum trigger delay depends on the threshold.
- The delay-for-hold can be configured via DAQ software.
 - Inject the signal to row-by-row with signal amplitude of 1.2V
 - Hold scan was performed from the range of 20-160 in steps of 20.



Hold Scan





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Summary & Prospects

Summary & Prospects

- Commissioning for **15 layers** of slabs were performed during the summer 2021.
 - First time with **15,300 channels**.
 - Commissioning includes:
 - Masking
 - Scurve
 - Cosmic Data Taking
 - Injection Test (Hold Scan)
 - Thanks to Roman, A. Irles, R. Martinez and Engineering members at IJC Lab.

• Future Plan

- Continuation of injection test.
- Preparation towards beam test at DESY on November.

Backup Slides

Layer 3 – 5







-80 -60 -40 -20 0 20 40 60

80

X

-60



mask_chip_chn_SLB4



mask_x_y_SLB5







Entre da contra de contra

0

20 40 60 80

-80 -60 -40 -20

-80



threshold_chip_chn_global_4



Layer 3 – 5

threshold_chip_chn_global_5

220 26

X

Layer 6 – 8



mask_chip_chn_SLB6







mask_chip_chn_SLB8



mask_x_y_SLB8







threshold x y global 8





threshold_chip_chn_global_7

230

220



Layer 9 –11



mask_chip_chn_SLB9



mask_x_y_SLB9





mask_chip_chn_SLB10

mask_chip_chn_SLB11



mask_x_y_SLB11



Layer 9 – 11





threshold_chip_chn_global_10









Layer 12 – 14



mask_chip_chn_SLB12



mask_x_y_SLB12





mask_chip_chn_SLB14



mask_x_y_SLB14



Layer 9 –14





threshold_chip_chn_global_13



