SiW-ECAL 15 Slabs Commissioning

CALICE Collaboration Meeting
8-11 September 2021

Yuichi Okugawa

Affiliation:

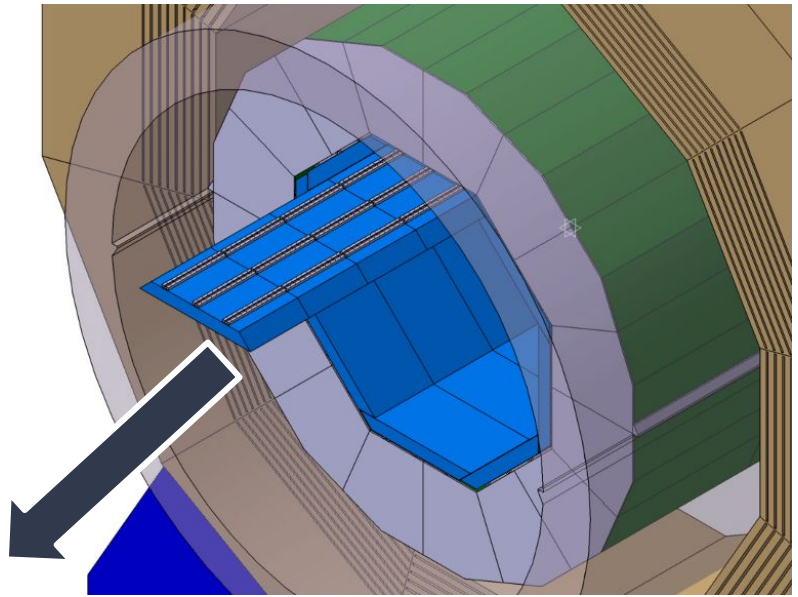
In collaboration with:

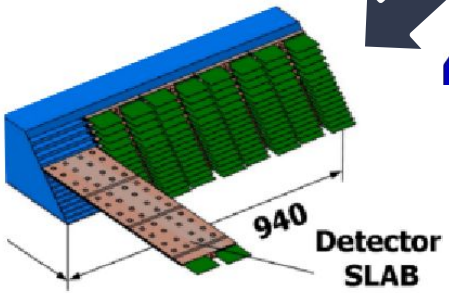
Introduction

Introduction

SiW ECAL

- Technological option for ILD ECAL.
- Optimized for Particle Flow Algorithm
- Requirements from ILD
  - **High granurality**
  - **Compactness**
- Absorber
  - Tungsten
    - X0 = 0.35 cm
    - Rm = 0.93 cm
    - λI = 9.946 cm
- Active material
  - Silicon

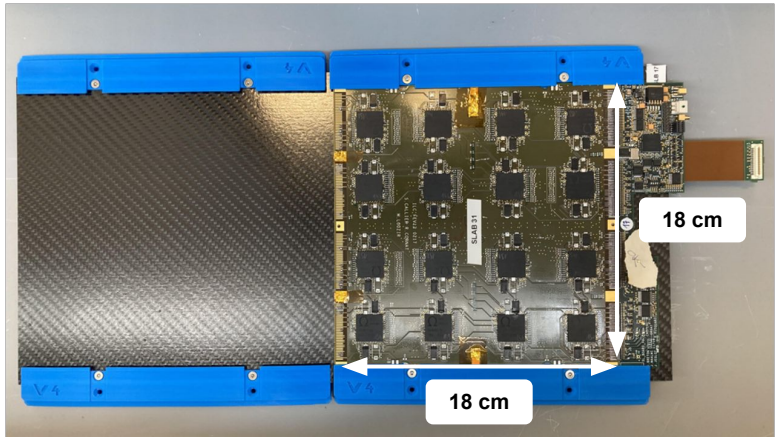


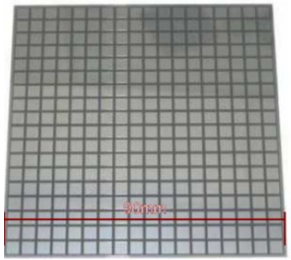


Introduction

SiW ECAL

- Each slabs are equipped with 4x4 **Skirocs** as **analog** readout units, along with a **SL board** as a **digital** readout unit.
- **Si Wafers** are equipped at the back of the layer.
  - size: 9x9 cm^2, thickness: 500, 320 μm
  - pixel size: 5x5 mm^2
  - 4 of them are equipped at back of the slab.
- Number of channels
  - 16 skirocs x 64 channels x 15 layers = **15,360 channels**





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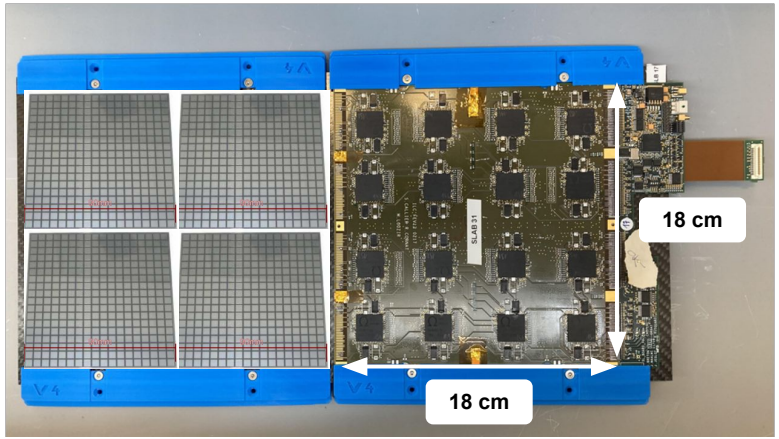
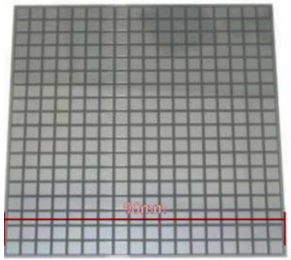
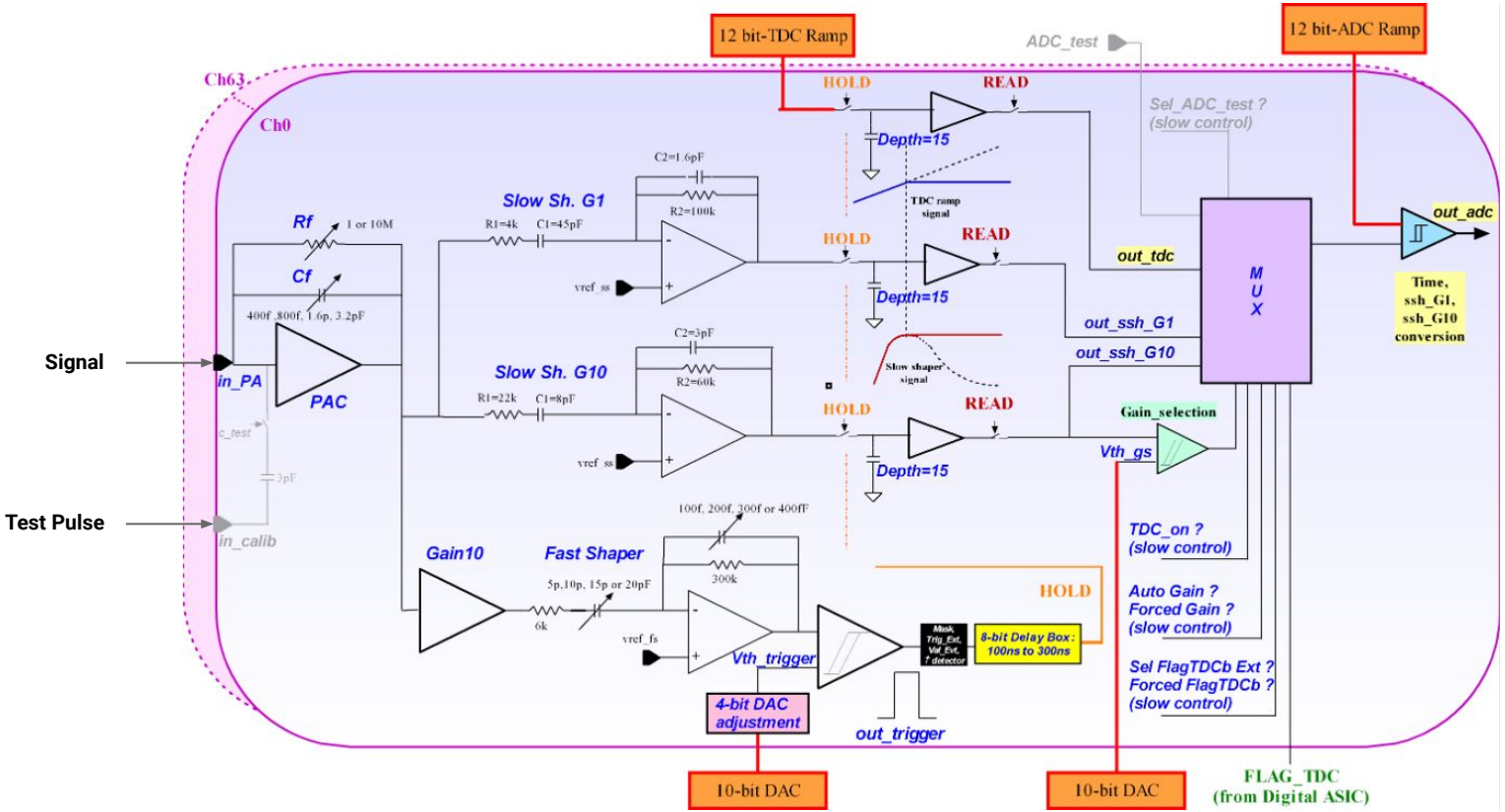
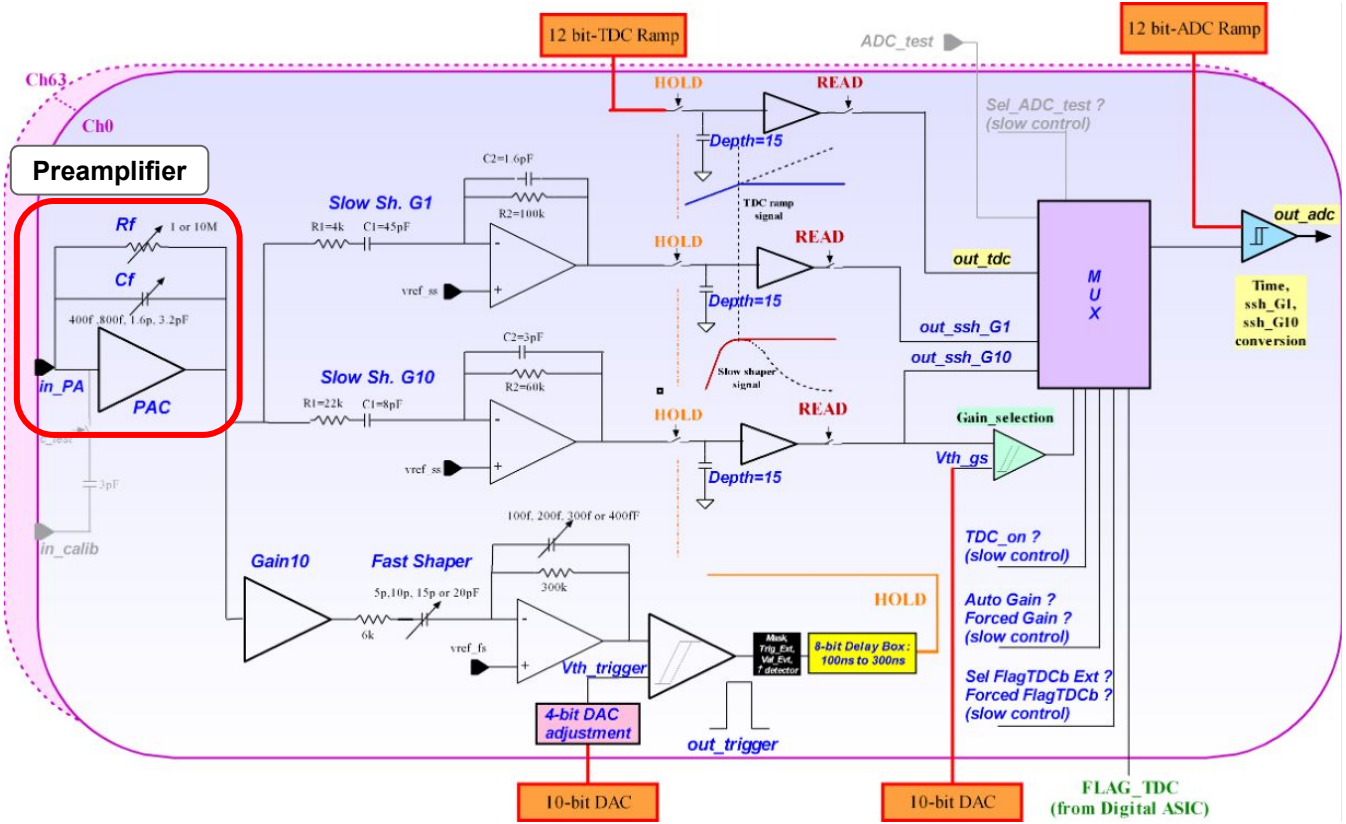




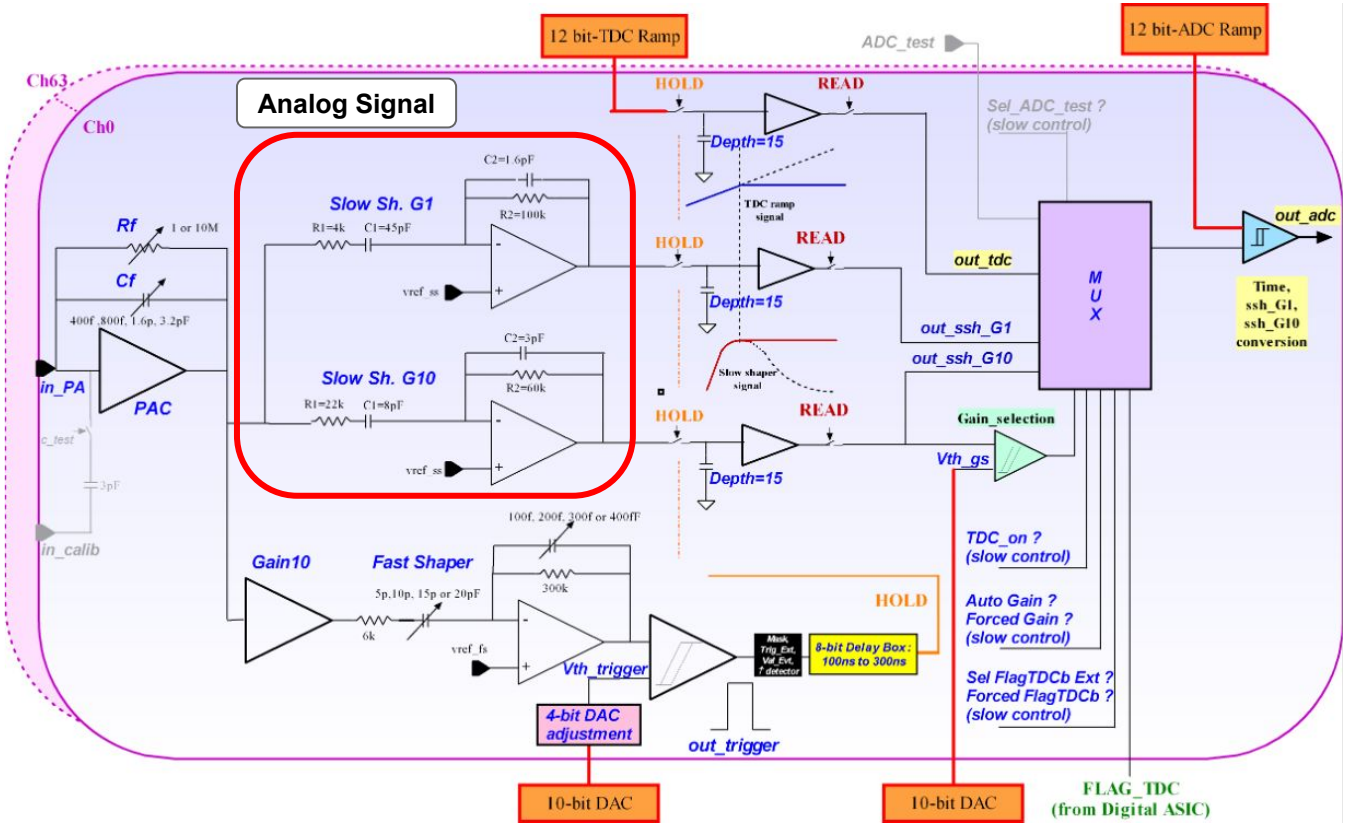
Electronics of Skiroc2



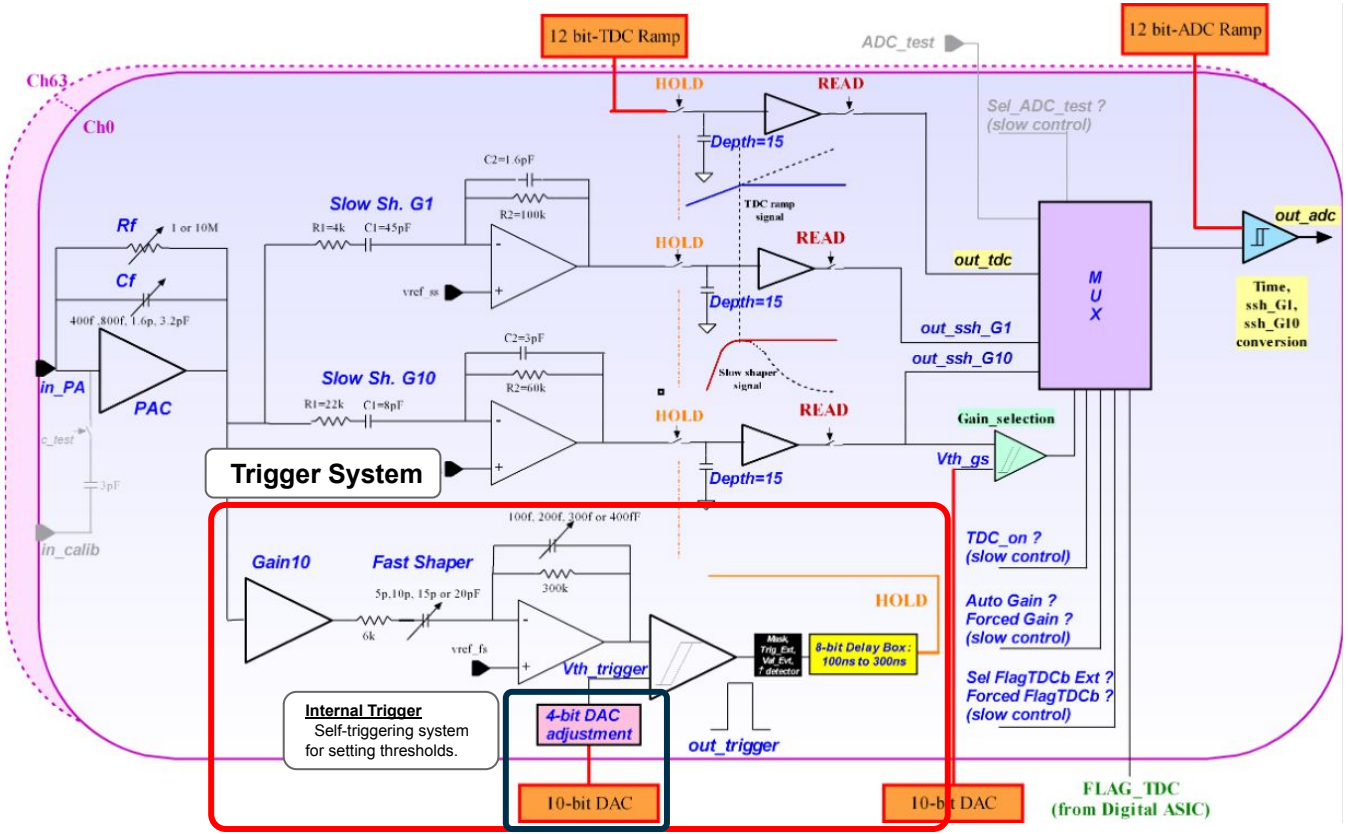
Electronics of Skiroc2



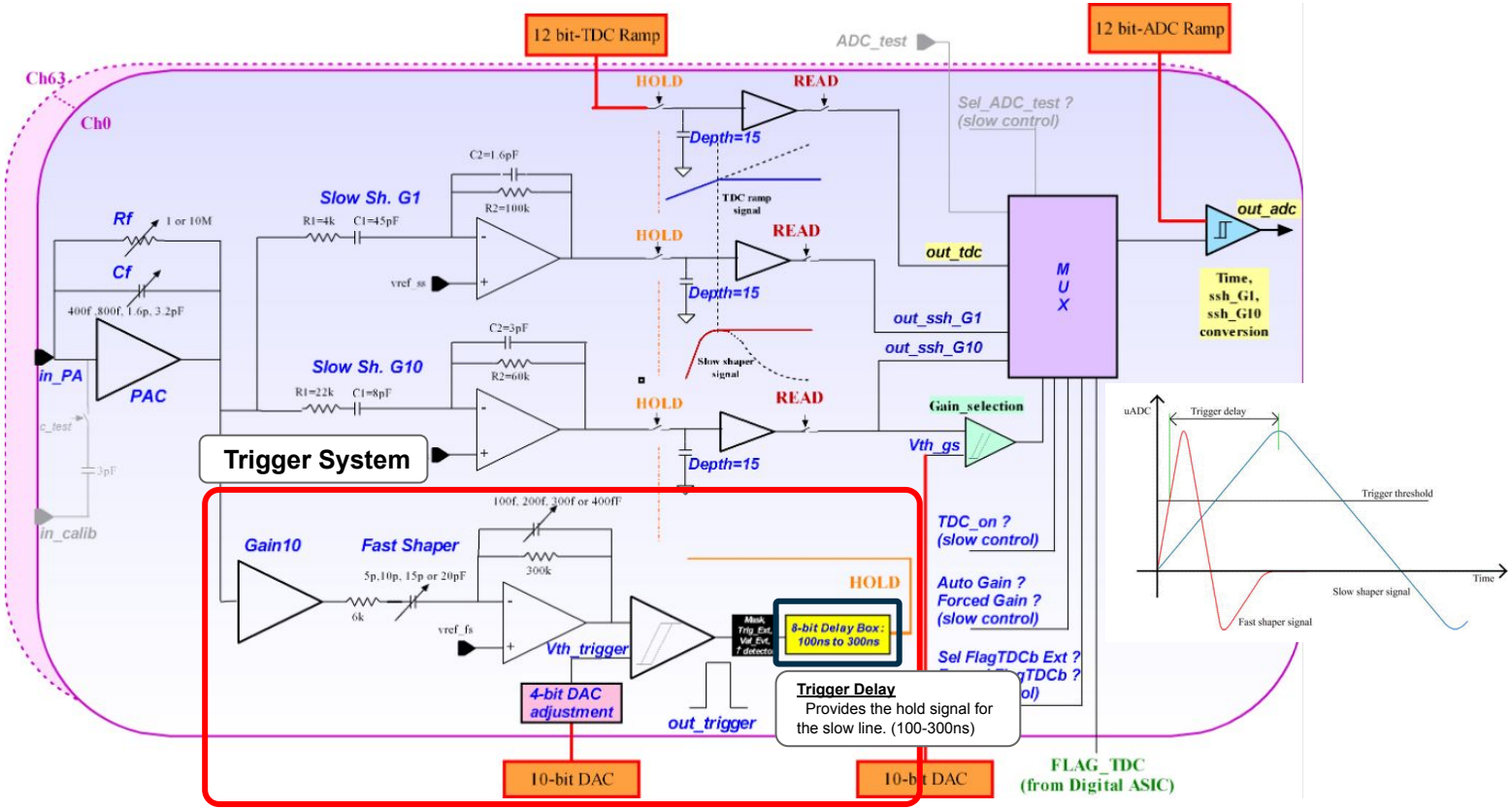
Electronics of Skiroc2



Electronics of Skiroc2

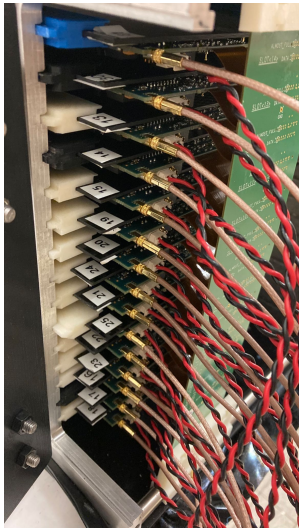


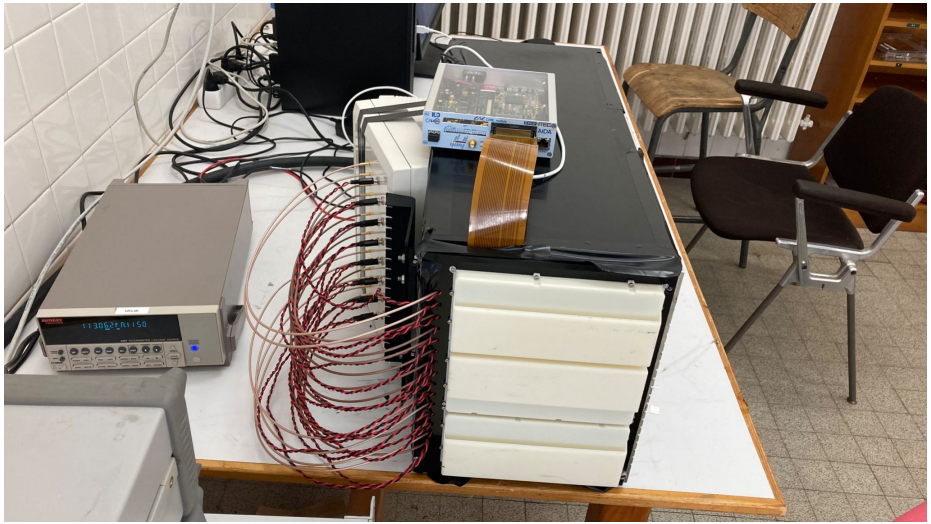
Electronics of Skiroc2



Introduction

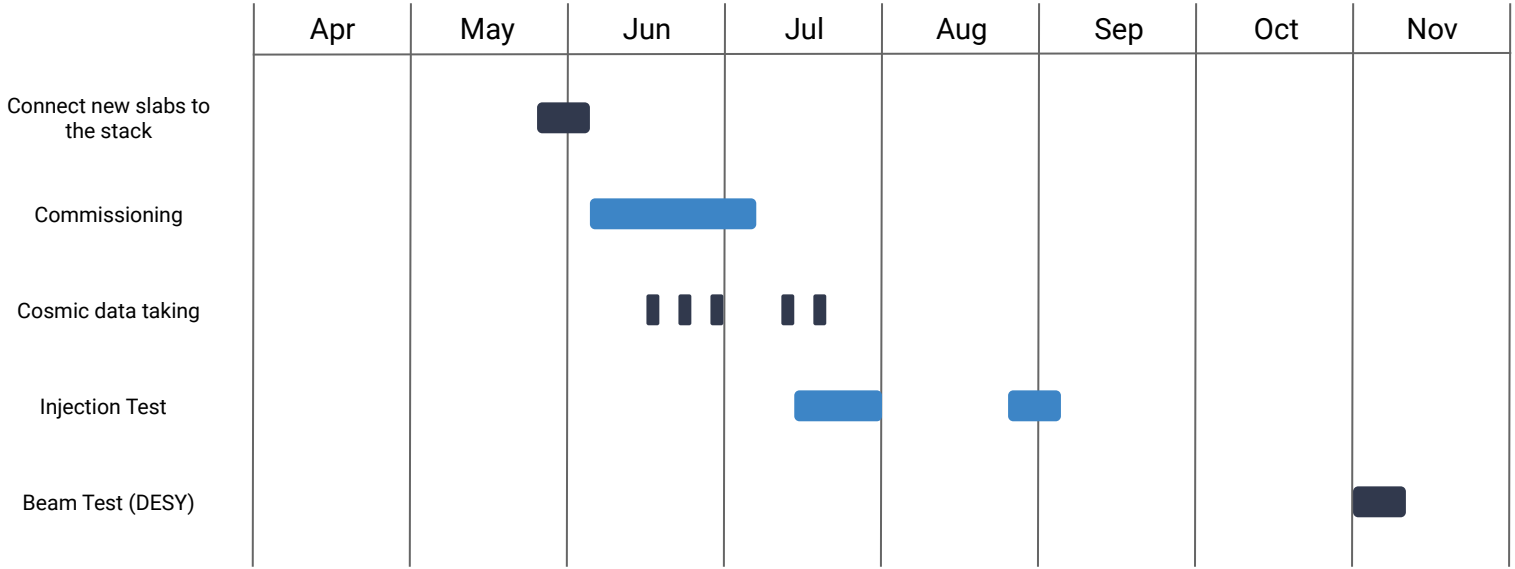
- 5 layers were added to the stack → Making it **15 in total.** (That's half of number of layers of actual ILD)
- Newly added layers contain skiroc2a, which enables us to tick channel thresholds.
- The density between the layers are realistic compared to the actual detector implementation at ILD.





Status

Timeline for preparing the beam test

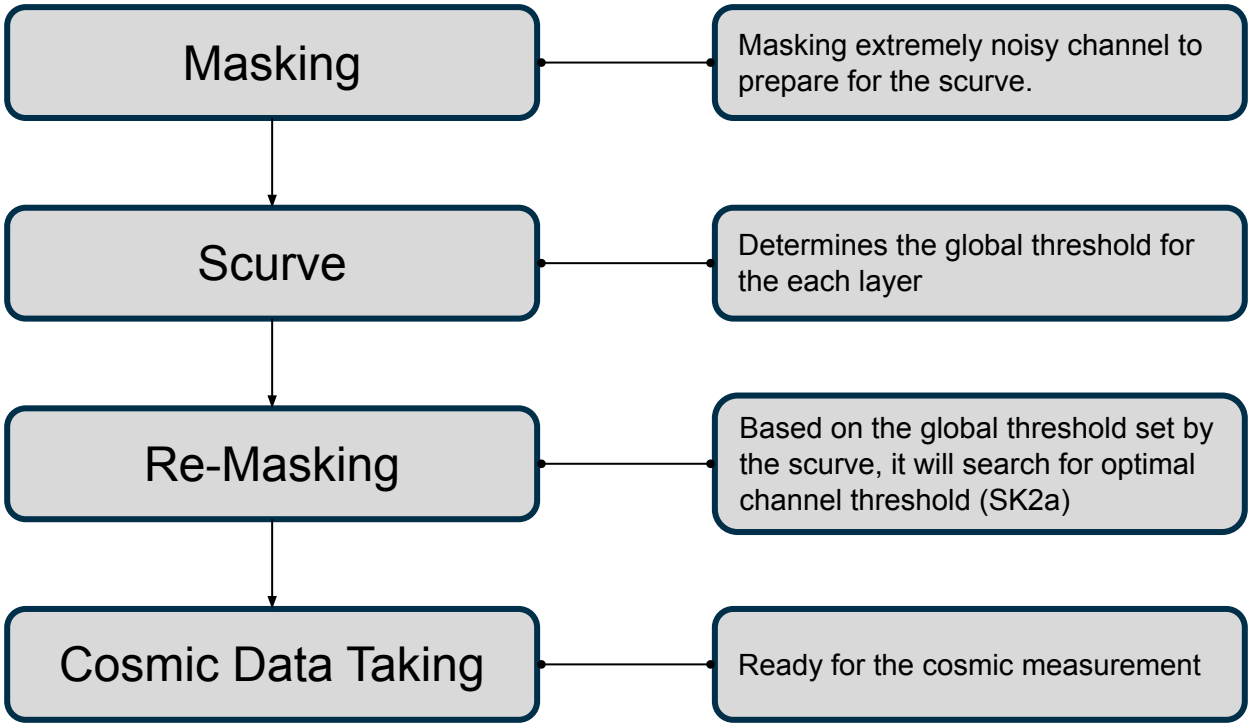


Status of Each Layers

coreKapton slot	Layer position	Slab ID	ASU type	wafer	front end (slboard ID)	Glissiere neded for the W	*W in front (mm)*	*X0*	*X0 (acc)*	Comments/Issues
14	0	31	FEV12	500						
13	1	30	FEV12	500						
12	2	13	FEV11	320	10	2.1mm	2.1	0.6	0.6	
11	3	14	FEV11	320	5	2.1mm	2.1	0.6	1.2	
10	4	15	FEV10	320	1	2.1mm	2.1	0.6	1.8	
9	5	19	FEV11	320	13	2.1mm	2.1	0.6	2.4	
8	6	20	FEV11	320	11	2.1mm	2.1	0.6	3	
7	7	24	FEV12	500	7	2.1mm	2.1	0.6	3.6	Stable AVDD ??
6	8	21	FEV11	320	14	2.1mm	2.1	0.6	4.2	
5	9	25	FEV12	500	3	2.1mm	2.1	0.6	4.8	problems communicating the ID of the SLboard ?? (SOLVED)
4	10	22	FEV11	320	4	4.2mm	2.1	0.6	5.4	
3	11	23	FEV10	320	6	4.2mm	4.2	1.2	6.6	
2	12	16	FEV11	320	9	2.1mm	2.1	0.6	7.2	
1	13	17	FEV11	320	2	4.2mm	4.2	1.2	8.4	problems communicating the ID of the SLboard ?? (SOLVED) Stable consumption ?? --> SOLVED shorcut in DVDD (capacitance in skiroc 14)
0	14	18	FEV11	320	0	whatever (no W will be added)	4.2	1.2	9.6	

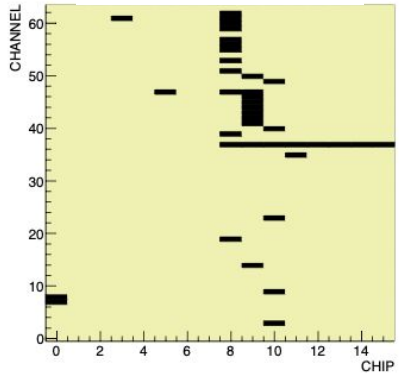
Commissioing

Procedure

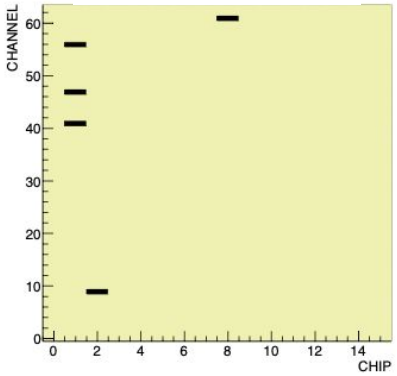

Masking
Masking extremely noisy channel to prepare for the scurve.
Scurve
Determines the global threshold for the each layer
Re-Masking
Based on the global threshold set by the scurve, it will search for optimal channel threshold (SK2a)
Cosmic Data Taking
Ready for the cosmic measurement

Masking

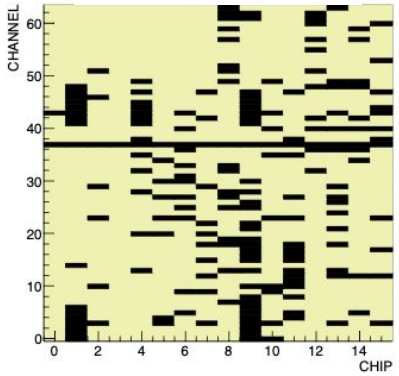
Layer 0, SLAB 31



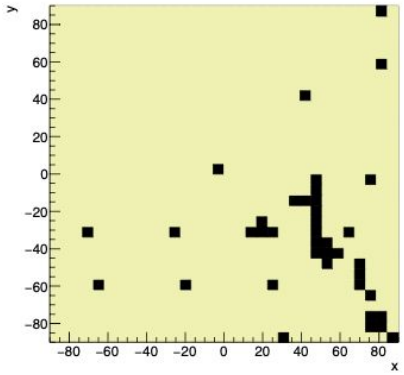
Layer 1, SLAB 30



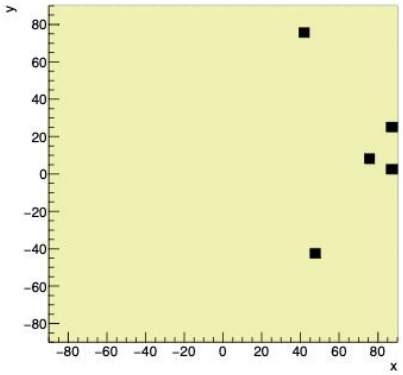
Layer 2, SLAB 17



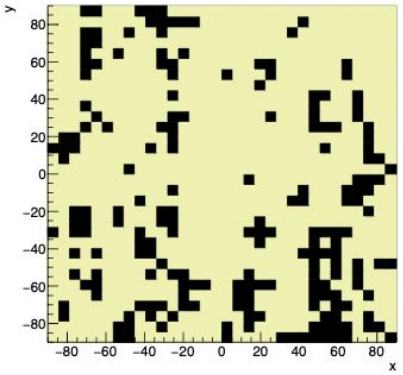
mask_x_y_SLB0



mask_x_y_SLB1

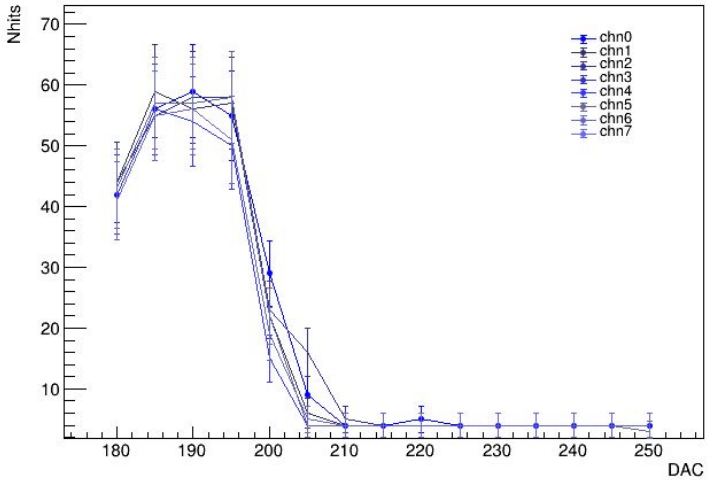


mask_x_y_SLB2



Scurve

- Scurve is used to estimate the optimal global threshold for each layer.
- These thresholds can be varied depending on the size of the signal that is induced.
- Plots below shows the plateau shift with different number of MIPs. (proportional to the pulse amplitude that is being injected)



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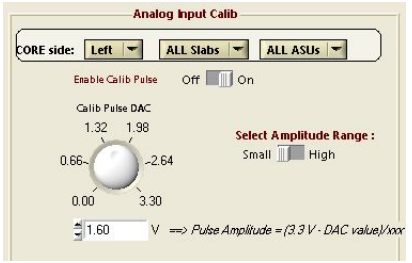
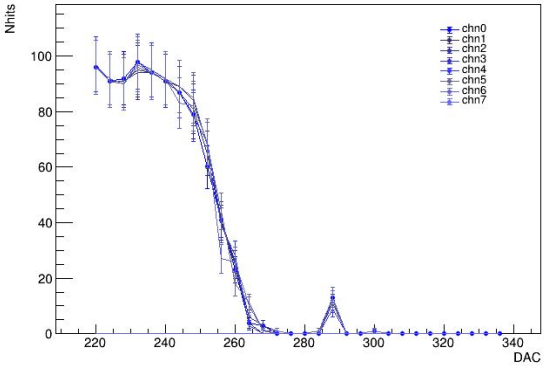
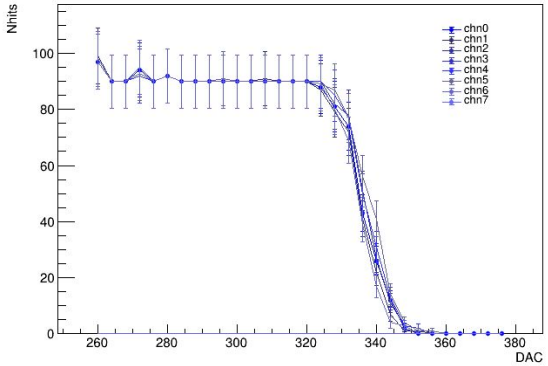


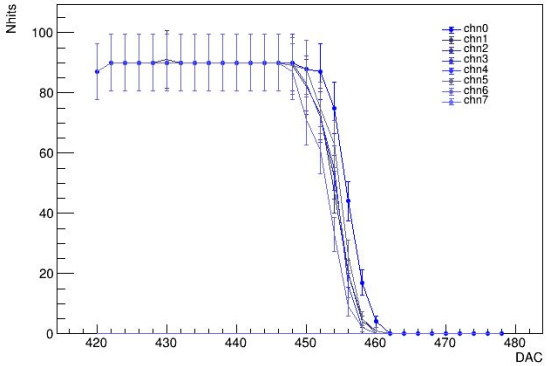
~ 0.5 MIP



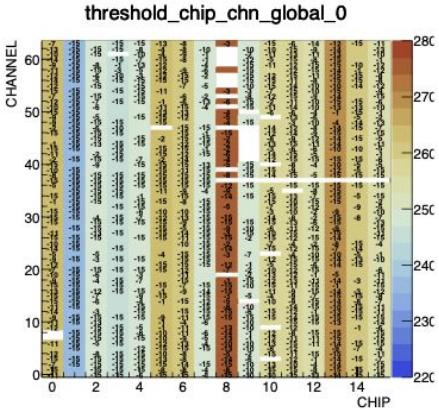
~ 1 MIP

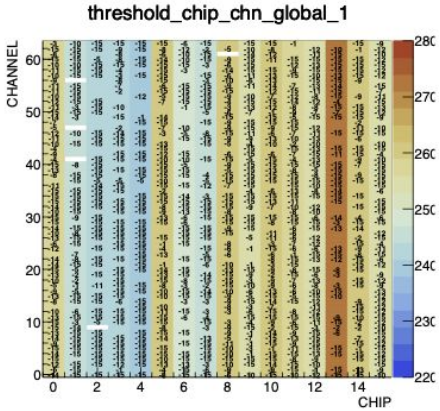


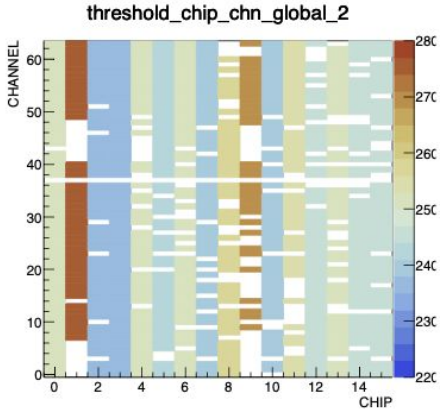
~ 2 MIPs

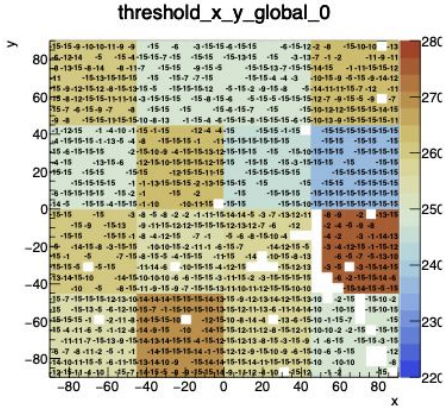


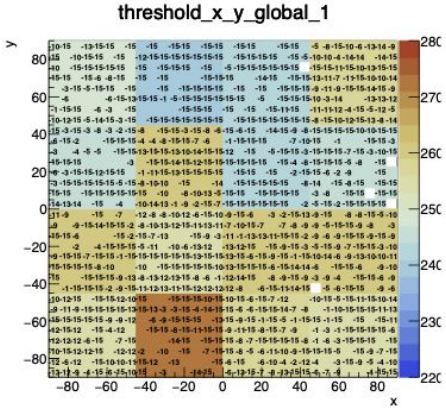
Thresholds

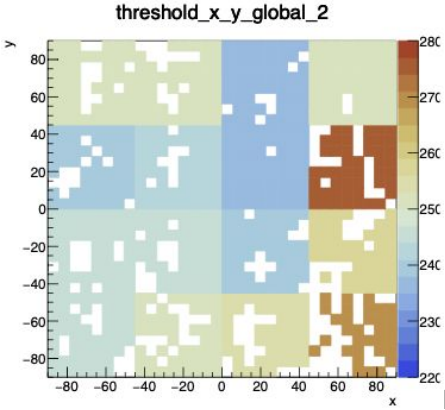

threshold_chip_chn_global_0
CHANNEL
CHIP


threshold_chip_chn_global_1
CHANNEL
CHIP


threshold_chip_chn_global_2
CHANNEL
CHIP

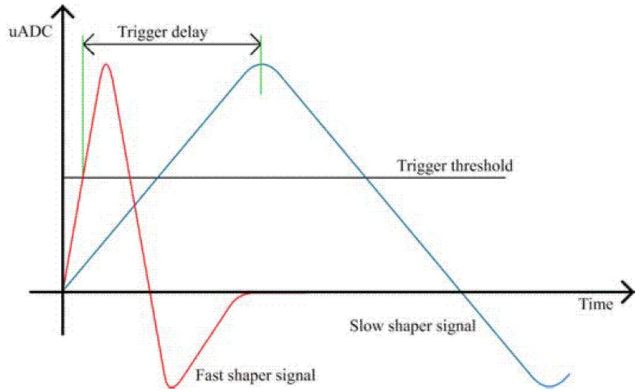

threshold_x_y_global_0
y
x


threshold_x_y_global_1
y
x

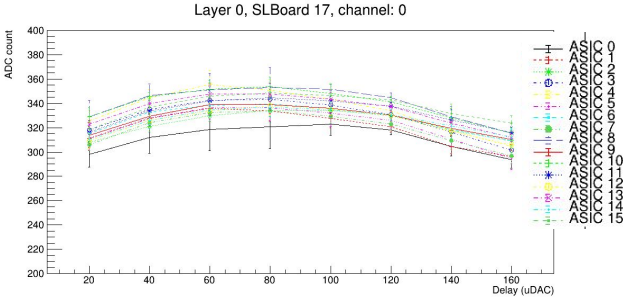

threshold_x_y_global_2
y
x

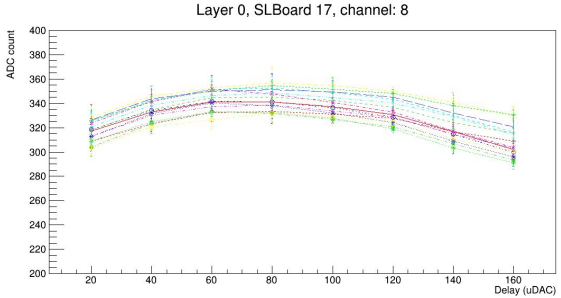
Hold Scan

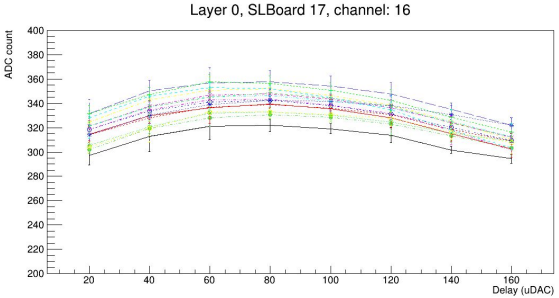
- Signal is needed to be read along the pulse that is generated by the slow shaper. This timing is managed by trigger delay.
  - Optimum trigger delay depends on the threshold.
- The delay-for-hold can be configured via DAQ software.
  - Inject the signal to row-by-row with signal amplitude of 1.2V
  - Hold scan was performed from the range of 20-160 in steps of 20.

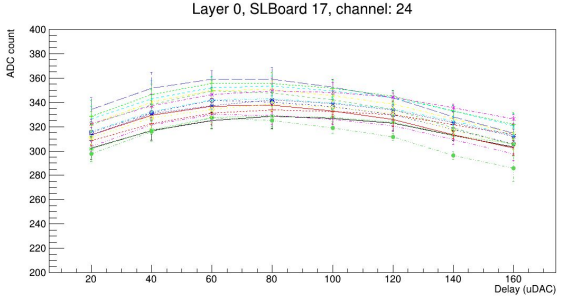


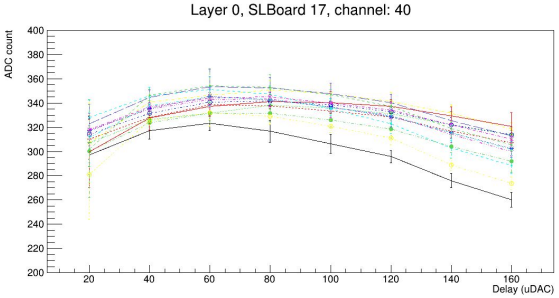
Hold Scan

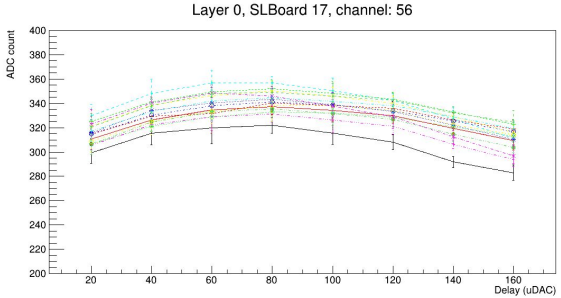

Layer 0, SLBoard 17, channel: 0
ADC count
Delay (uDAC)
ASIC 0
ASIC 1
ASIC 2
ASIC 3
ASIC 4
ASIC 5
ASIC 6
ASIC 7
ASIC 8
ASIC 9
ASIC 10
ASIC 11
ASIC 12
ASIC 13
ASIC 14
ASIC 15


Layer 0, SLBoard 17, channel: 8
ADC count
Delay (uDAC)


Layer 0, SLBoard 17, channel: 16
ADC count
Delay (uDAC)


Layer 0, SLBoard 17, channel: 24
ADC count
Delay (uDAC)


Layer 0, SLBoard 17, channel: 40
ADC count
Delay (uDAC)


Layer 0, SLBoard 17, channel: 56
ADC count
Delay (uDAC)

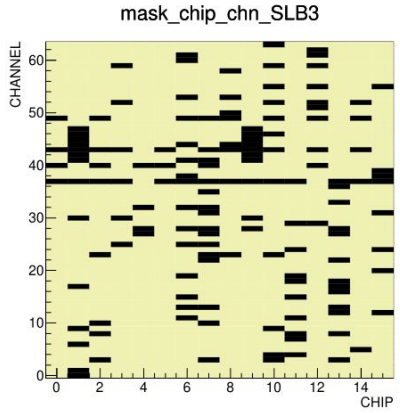
Summary & Prospects

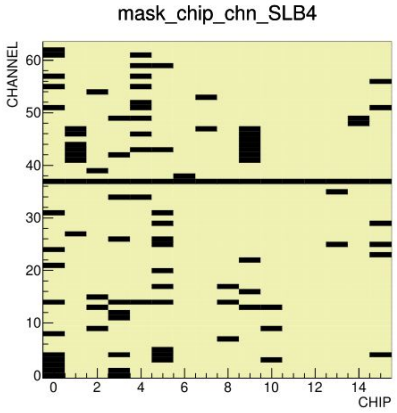
Summary & Prospects

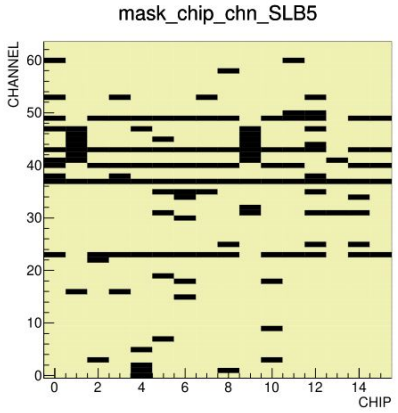
- Commissioning for **15 layers** of slabs were performed during the summer 2021.
  - First time with **15,300 channels**.
  - Commissioning includes:
    - Masking
    - Scurve
    - Cosmic Data Taking
    - Injection Test (Hold Scan)
  - Thanks to Roman, A. Irles, R. Martinez and Engineering members at IJC Lab.
- **Future Plan**
  - Continuation of injection test.
  - Preparation towards beam test at DESY on November.

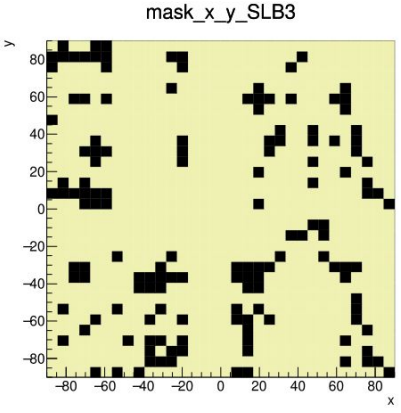
Backup Slides

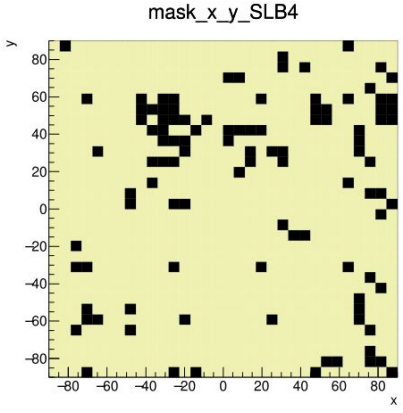
Layer 3 - 5

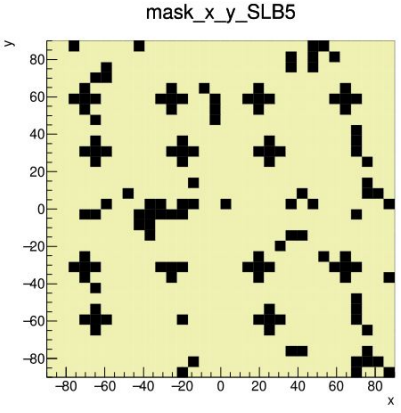

mask_chip_chn_SLB3
CHANNEL
CHIP


mask_chip_chn_SLB4
CHANNEL
CHIP

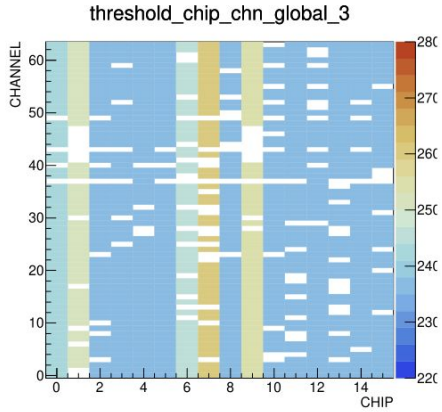

mask_chip_chn_SLB5
CHANNEL
CHIP

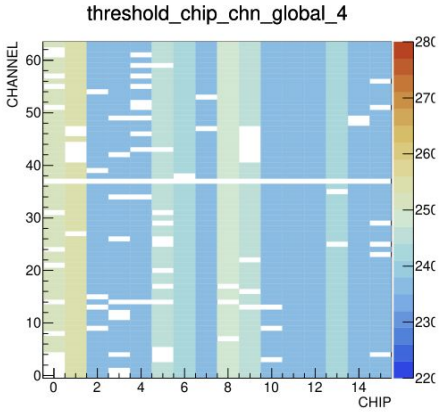

mask_x_y_SLB3
y
x

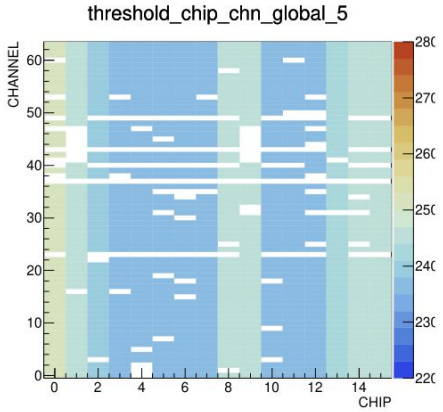

mask_x_y_SLB4
y
x

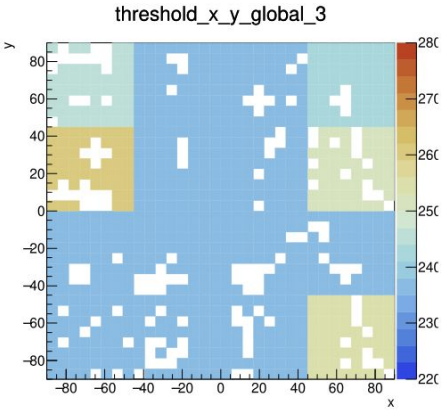

mask_x_y_SLB5
y
x

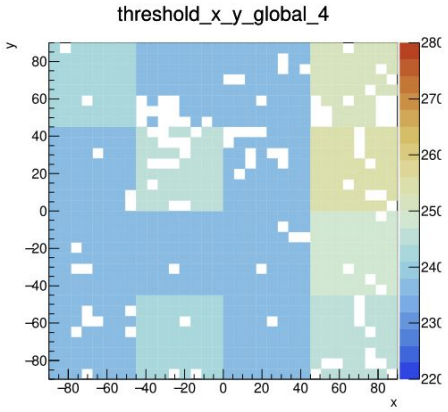
Layer 3 - 5

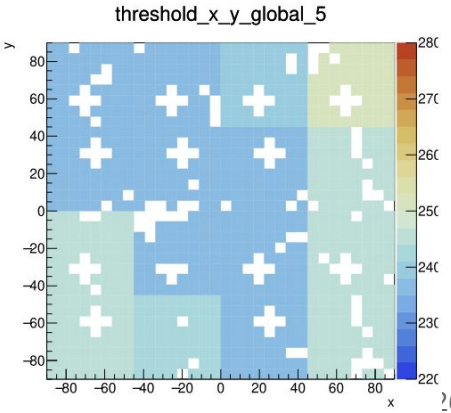

threshold_chip_chn_global_3
CHANNEL
CHIP


threshold_chip_chn_global_4
CHANNEL
CHIP

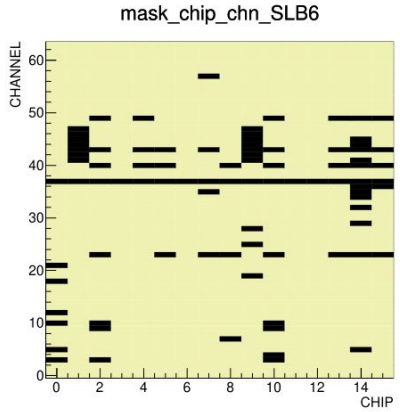

threshold_chip_chn_global_5
CHANNEL
CHIP

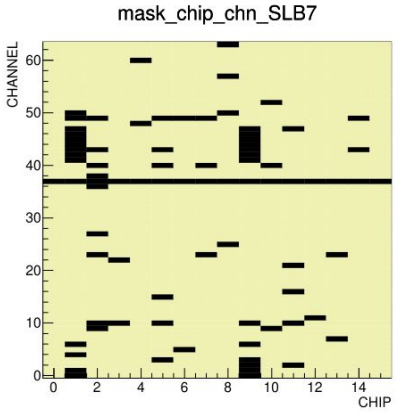

threshold_x_y_global_3
y
x

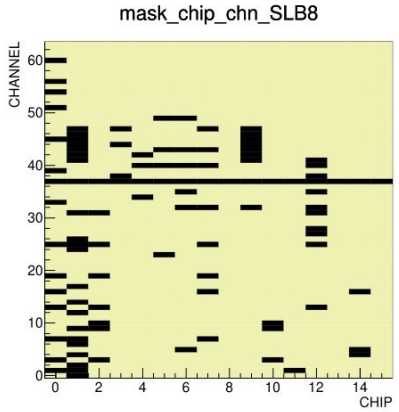

threshold_x_y_global_4
y
x

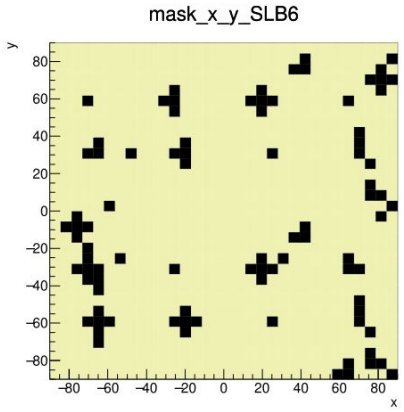

threshold_x_y_global_5
y
x

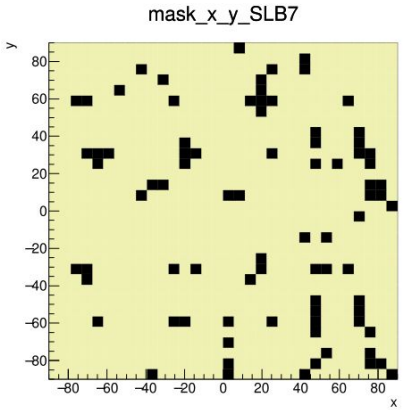
Layer 6 – 8

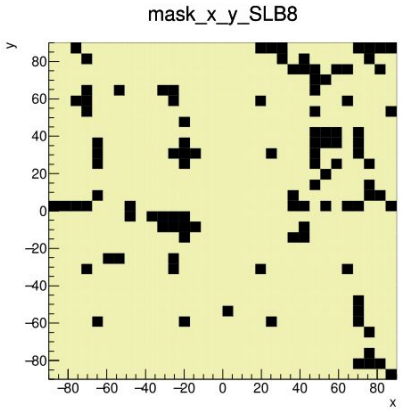

mask_chip_chn_SLB6
CHANNEL
CHIP


mask_chip_chn_SLB7
CHANNEL
CHIP

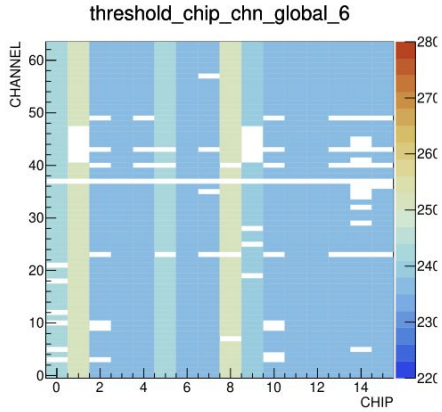

mask_chip_chn_SLB8
CHANNEL
CHIP

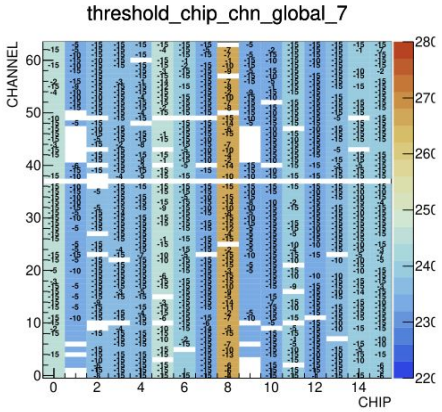

mask_x_y_SLB6
y
x

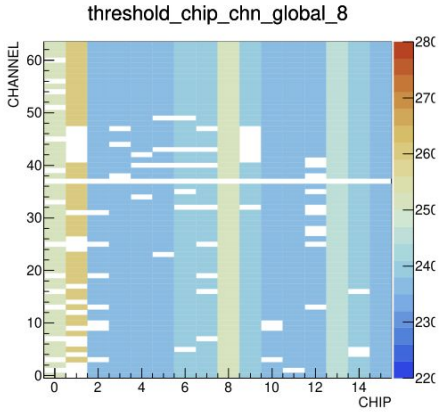

mask_x_y_SLB7
y
x

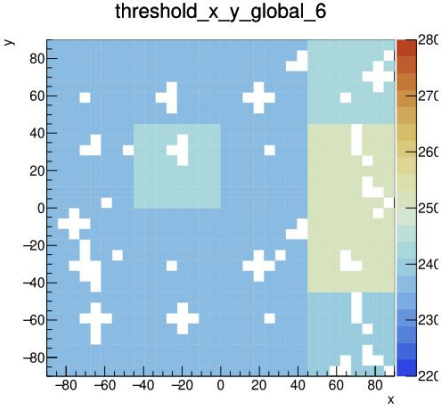

mask_x_y_SLB8
y
x

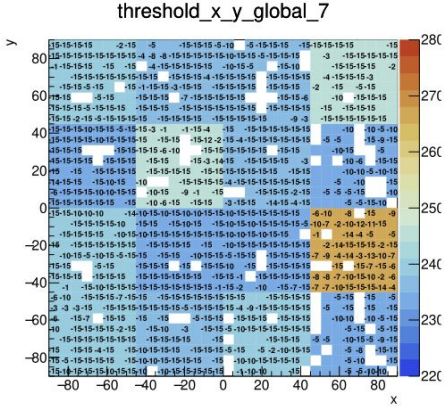
Layer 6 -8

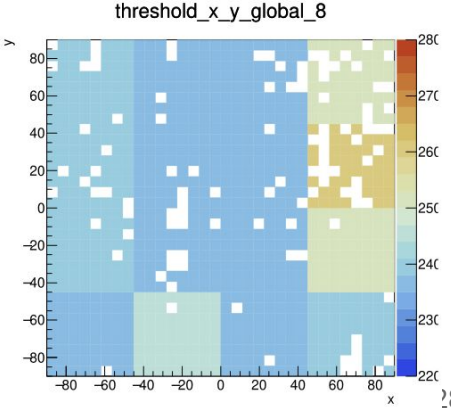

threshold_chip_chn_global_6
CHANNEL
CHIP


threshold_chip_chn_global_7
CHANNEL
CHIP

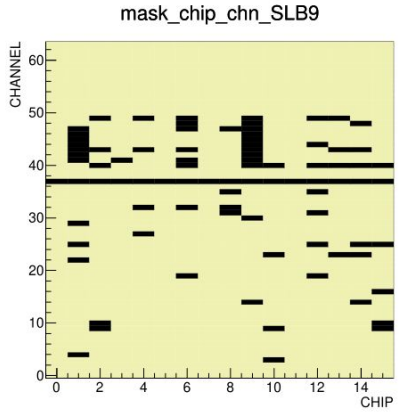

threshold_chip_chn_global_8
CHANNEL
CHIP

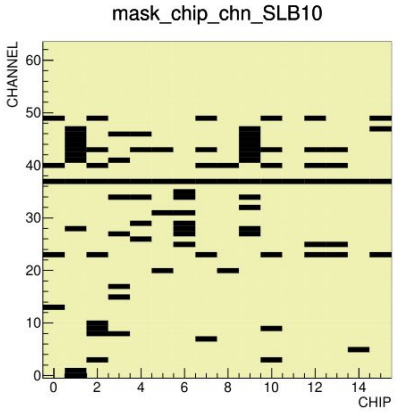

threshold_x_y_global_6
y
x

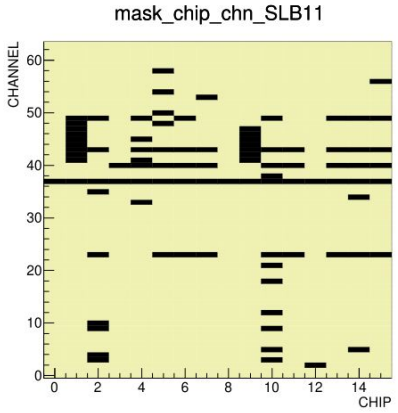

threshold_x_y_global_7
y
x

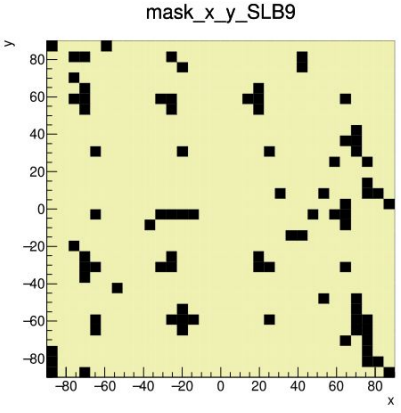

threshold_x_y_global_8
y
x

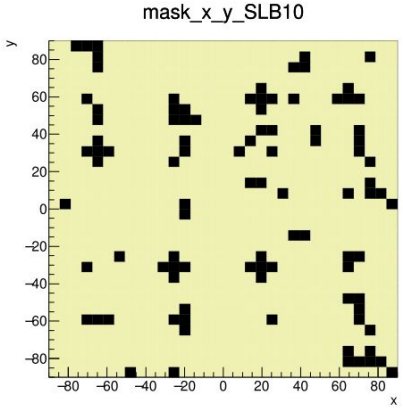
Layer 9 -11

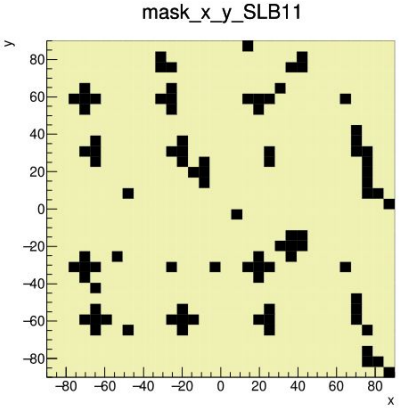

mask_chip_chn_SLB9
CHANNEL
CHIP


mask_chip_chn_SLB10
CHANNEL
CHIP

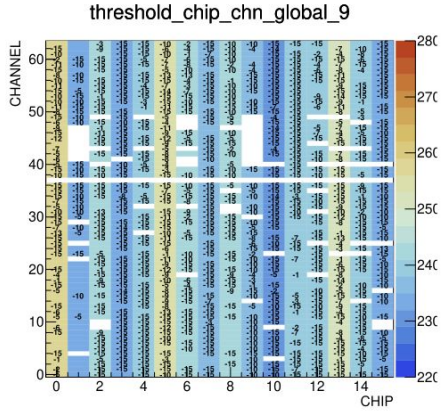

mask_chip_chn_SLB11
CHANNEL
CHIP

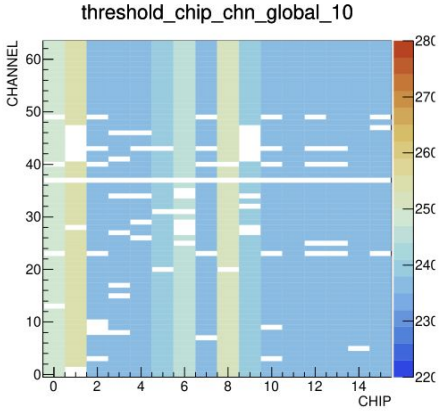

mask_x_y_SLB9
y
x

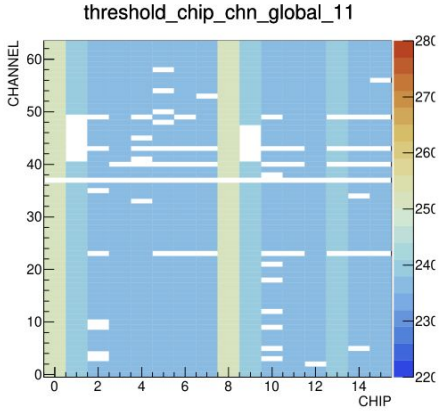

mask_x_y_SLB10
y
x

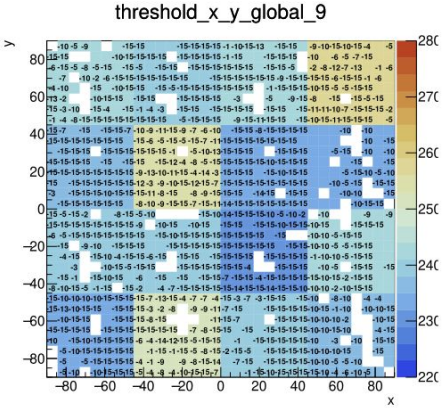

mask_x_y_SLB11
y
x

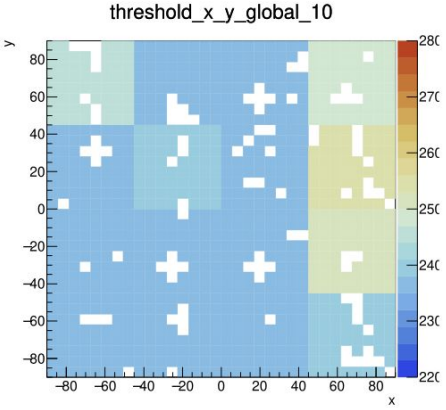
Layer 9 – 11

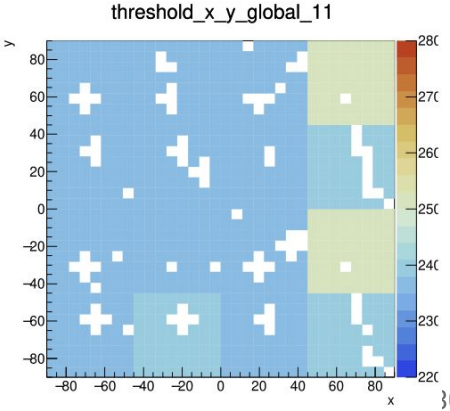

threshold_chip_chn_global_9
CHANNEL
CHIP


threshold_chip_chn_global_10
CHANNEL
CHIP

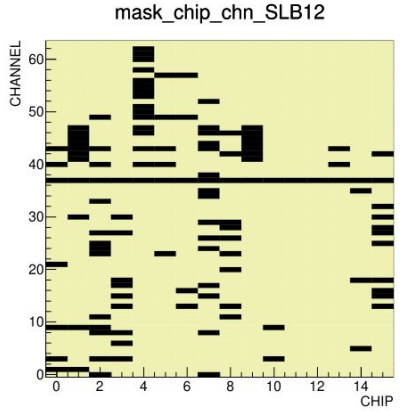

threshold_chip_chn_global_11
CHANNEL
CHIP

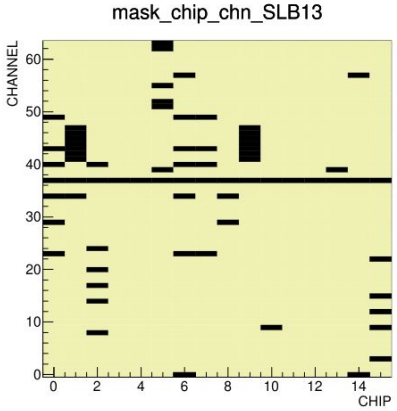

threshold_x_y_global_9
y
x

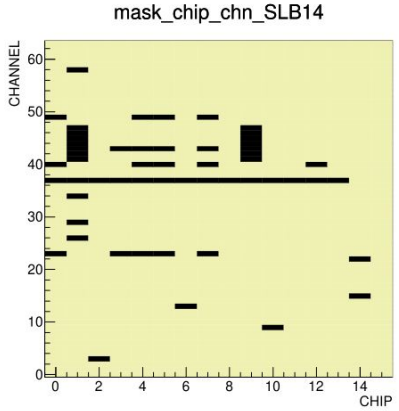

threshold_x_y_global_10
y
x

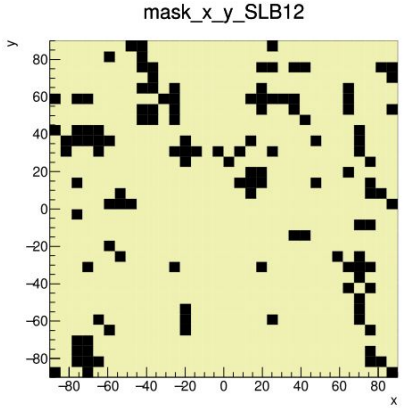

threshold_x_y_global_11
y
x

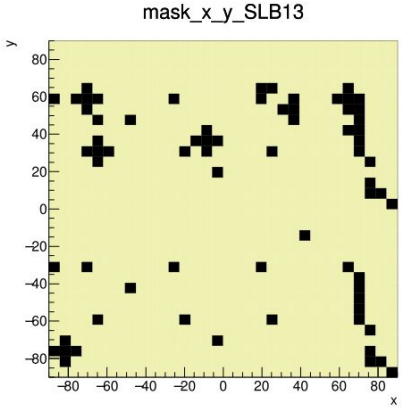
Layer 12 - 14

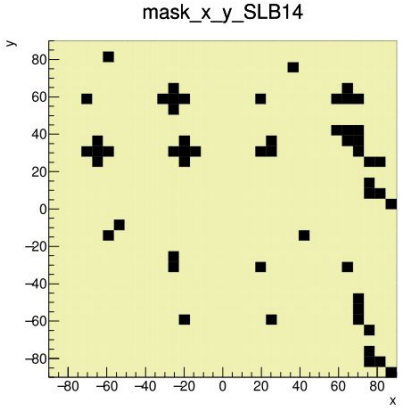

mask_chip_chn_SLB12
CHANNEL
CHIP


mask_chip_chn_SLB13
CHANNEL
CHIP

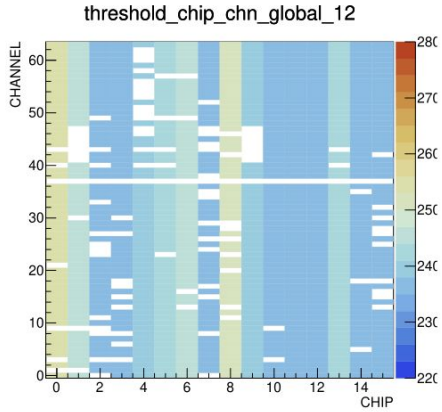

mask_chip_chn_SLB14
CHANNEL
CHIP

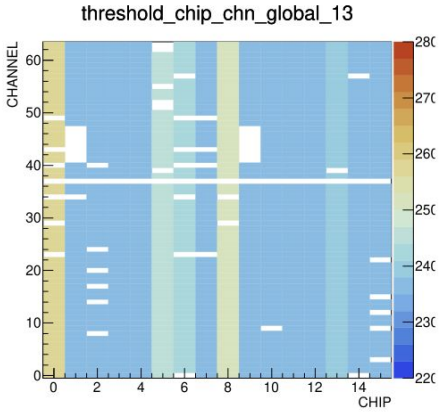

mask_x_y_SLB12
y
x

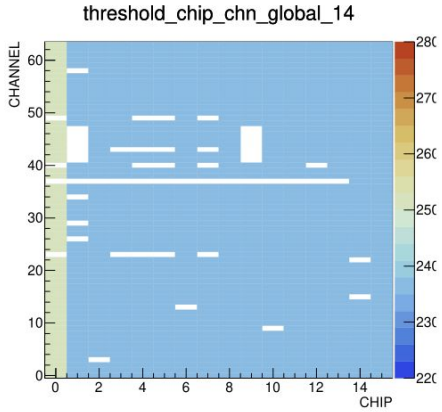

mask_x_y_SLB13
y
x

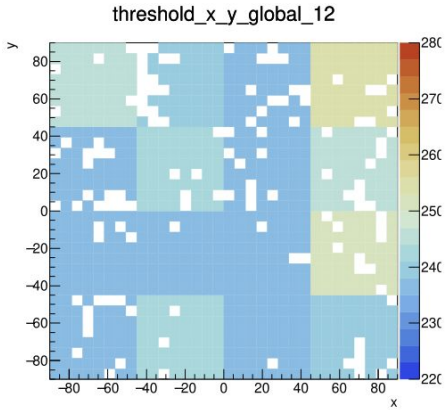

mask_x_y_SLB14
y
x

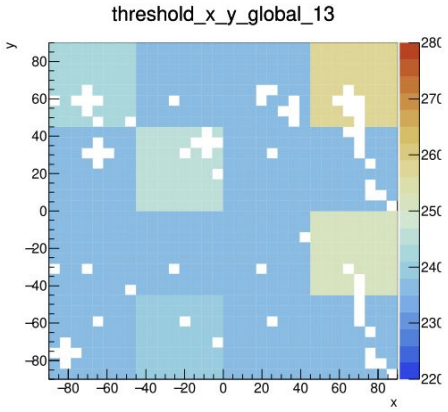
Layer 9 -14

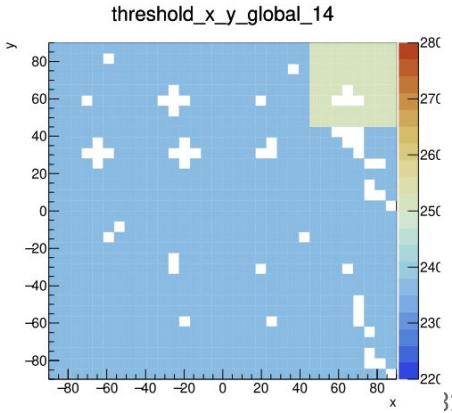

threshold_chip_chn_global_12
CHANNEL
CHIP


threshold_chip_chn_global_13
CHANNEL
CHIP


threshold_chip_chn_global_14
CHANNEL
CHIP


threshold_x_y_global_12
y
x


threshold_x_y_global_13
y
x


threshold_x_y_global_14
y
x