

CALICE SiW ECAL – Status of Prototype

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On behalf of the SiW ECAL Groups in CALICE:

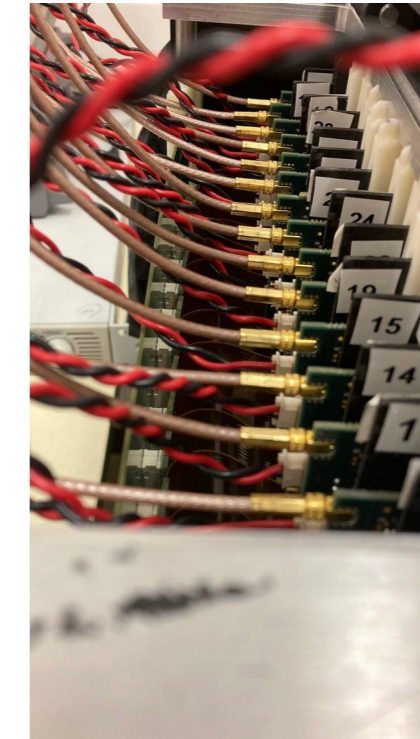
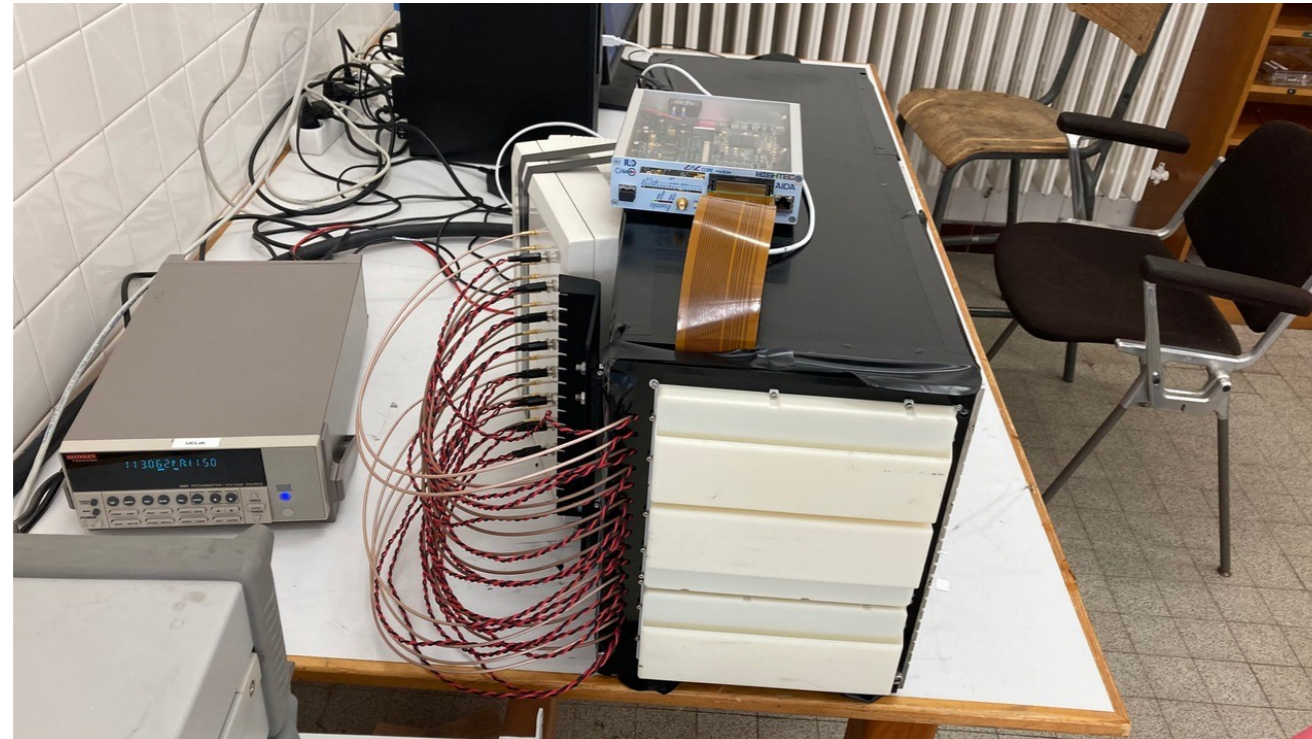


TB Meeting – July 2021

- **The stack is a priori ready**
 - However at the moment only 11 fully equipped layers
 - Two more ASUs of type FEV12 have been tested electrically and wait for being equipped with HV Kapton
 - One more is (still) under repair at LPNHE
 - COBs will complete the stack
 - Decided to produce two more over summer
 - For these two we have a metrology sheet and can thus follow the occurrence of deformations
 - Planned trip to CERN for chip bonding in June
- **Completion of the stack with the goal to run with 15 ASUs/layers**
 - Setup can be completed by FEV13 (See talk by Jihane in September meeting and next slide)
 - Would need (additional) mechanical housing
- **Continuous commissioning in coming weeks with progressive increase of number of layers**
 - Manpower situation has improved (New PhD and intern at IJCLab + Visit of Adrian to IJCLab)
- **Setup of proper interlock and slow control systems for beam test**

(Re)start of Stack

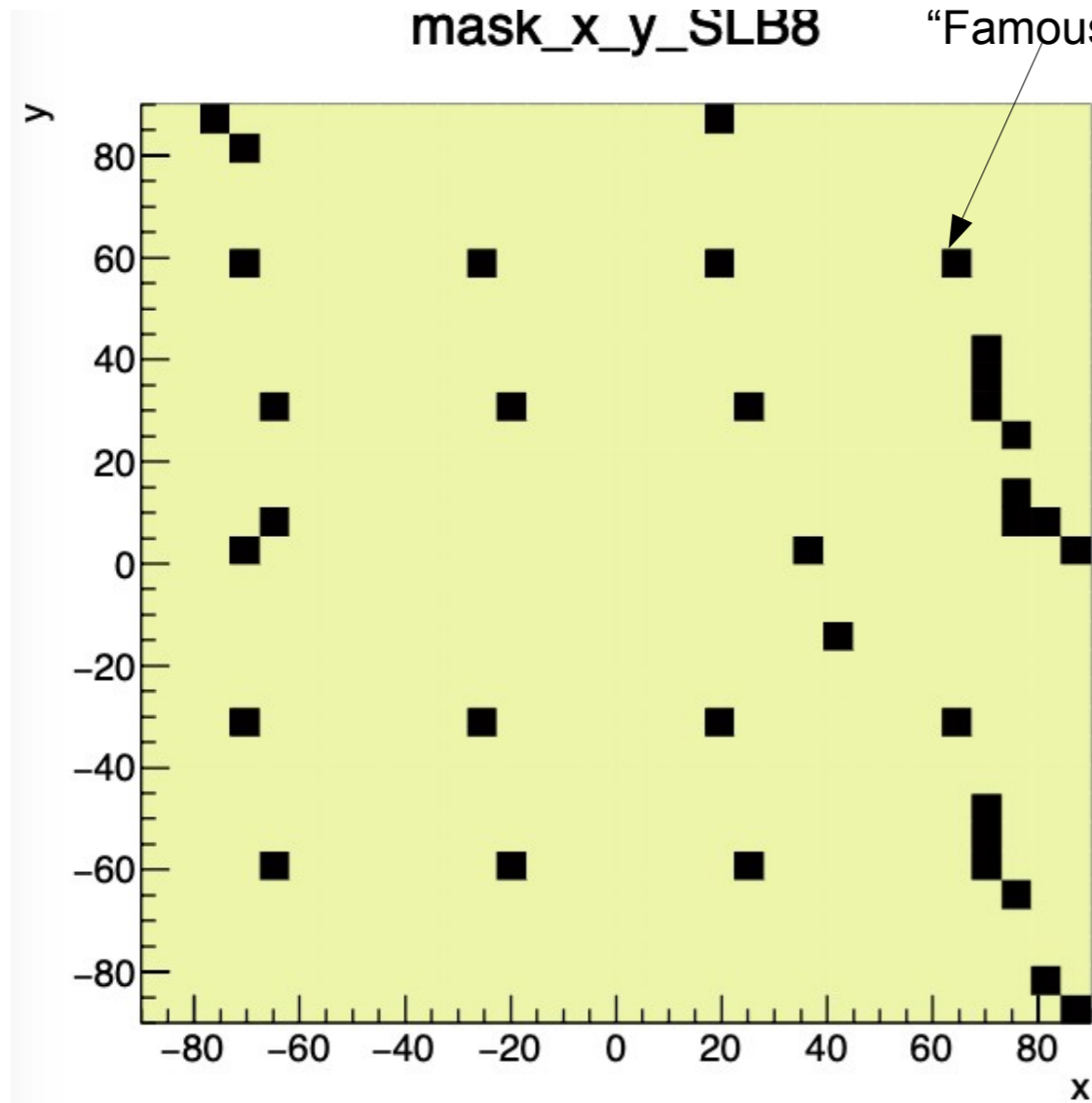
- Mounting of stack in 2nd half of may
 - ... including two slabs repaired at LPNHE over Winter/Spring 2020/21
- Start on 2nd of June with 15 layers by Yuichi (PhD), Robin (intern), IJCLab engineers and technicians and Adrian during visit to IJCLab
 - Reminder: 15 layers correspond to 15360 cells



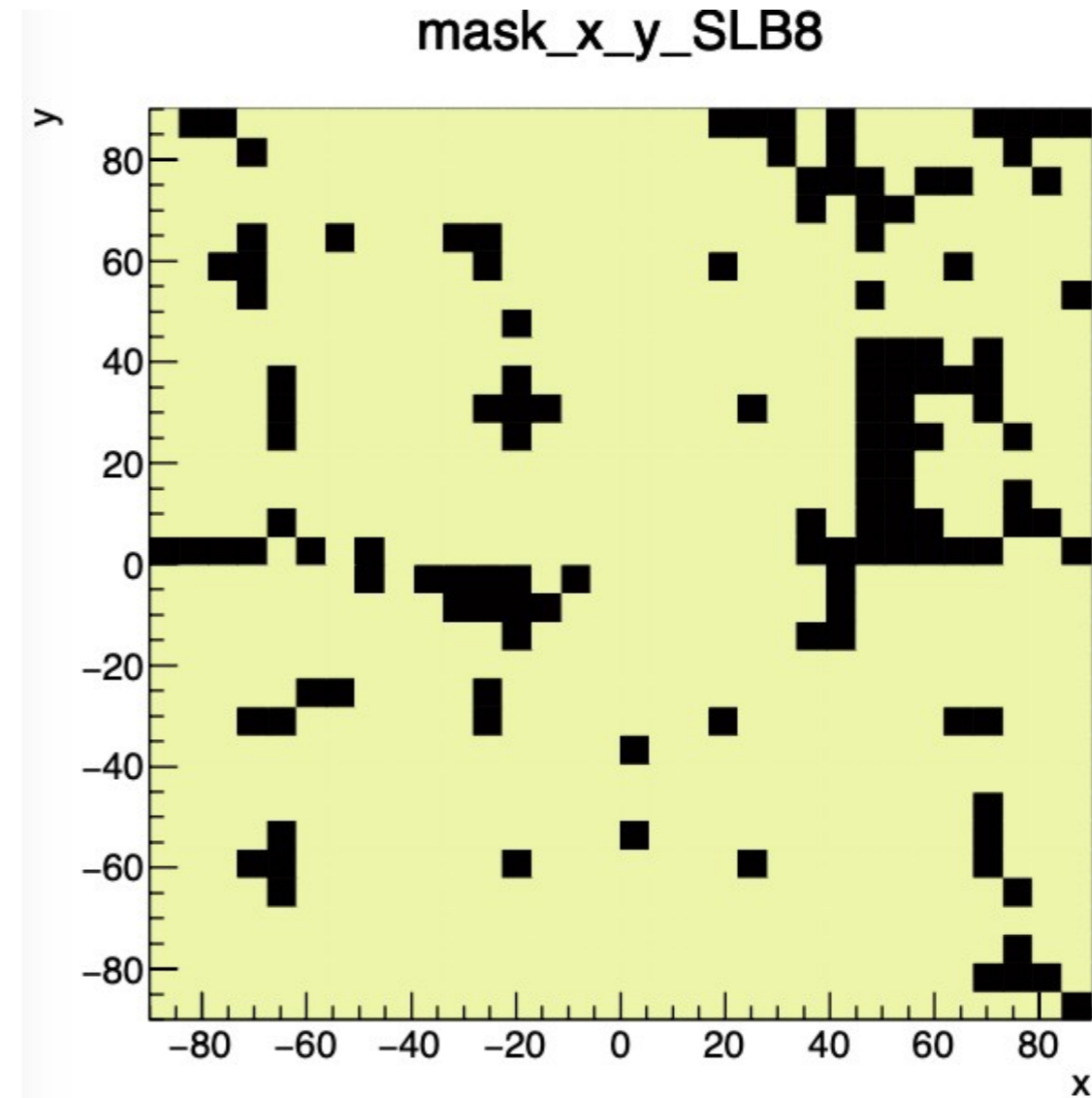
- Since 2/6/21: Commissioning
- Since 18/6/21: Data taking with cosmics

- Commissioning using scripts and s/w developed by Adrian in recent years (available on github)
- Four long cosmic runs since 18/6/21 (taken by Yuichi under guidance by Adrian)
 - 50001 - 50004
 - Consistent settings since 25/6/21
 - Report on data taking via e-mail and via elog hosted at LLR
 - Data stored in Ecal-Box at CERN and are accessible to Ecal members
 - Currently analysis is mainly carried out by Adrian and Yuichi but hope to increase circle of analysers in coming weeks/months
- Regular DQ Meetings

Typical slab: SlabID 21 (currently layer 8)



- Masked channels after lowering threshold to 275 DAC (~3/4 MIP)
- Short acquisition window 1ms
- Less vulnerable to noise and in particular to retriggering

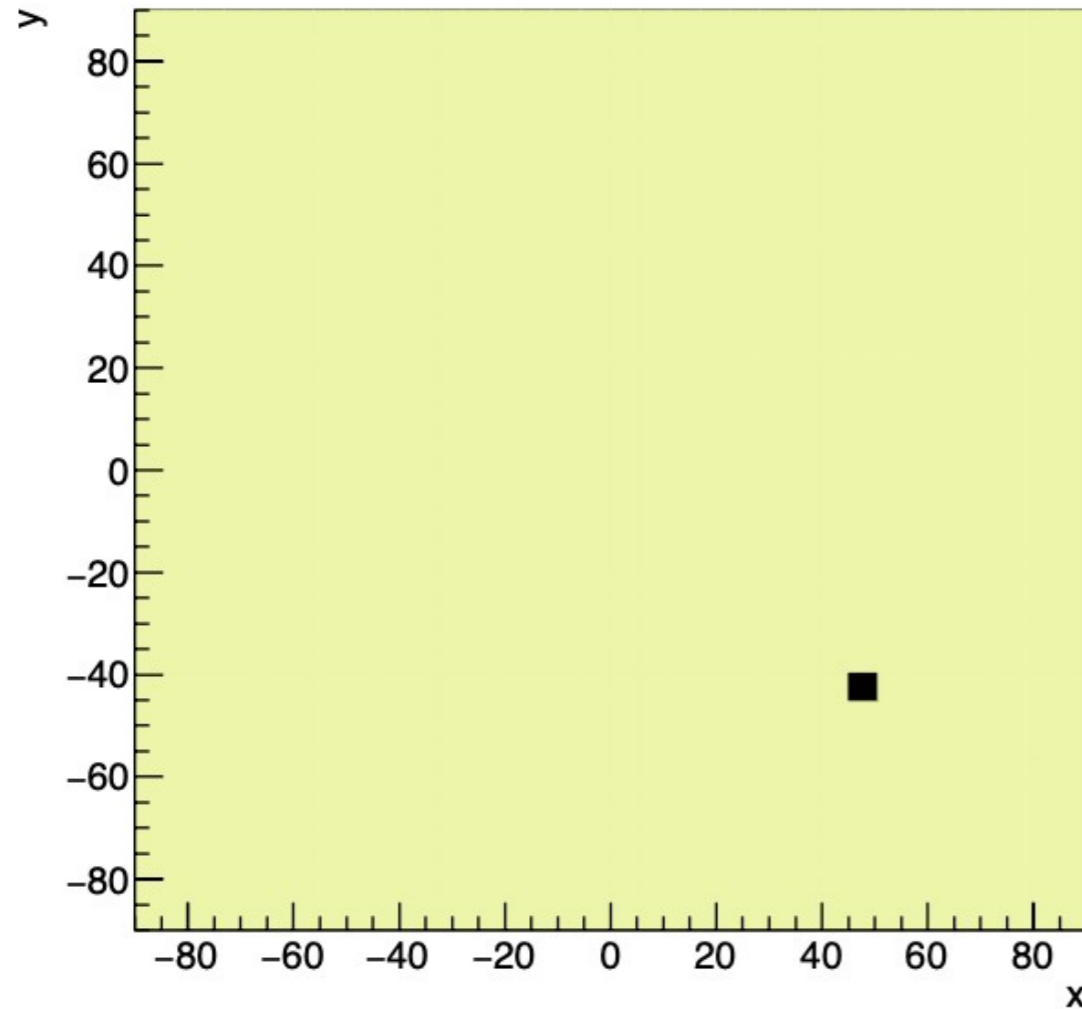


- Masked channels after optimising for cosmics
- **Long** acquisition window 100ms
- Vulnerable to noise and in particular to retriggering

Impression Commissioning II

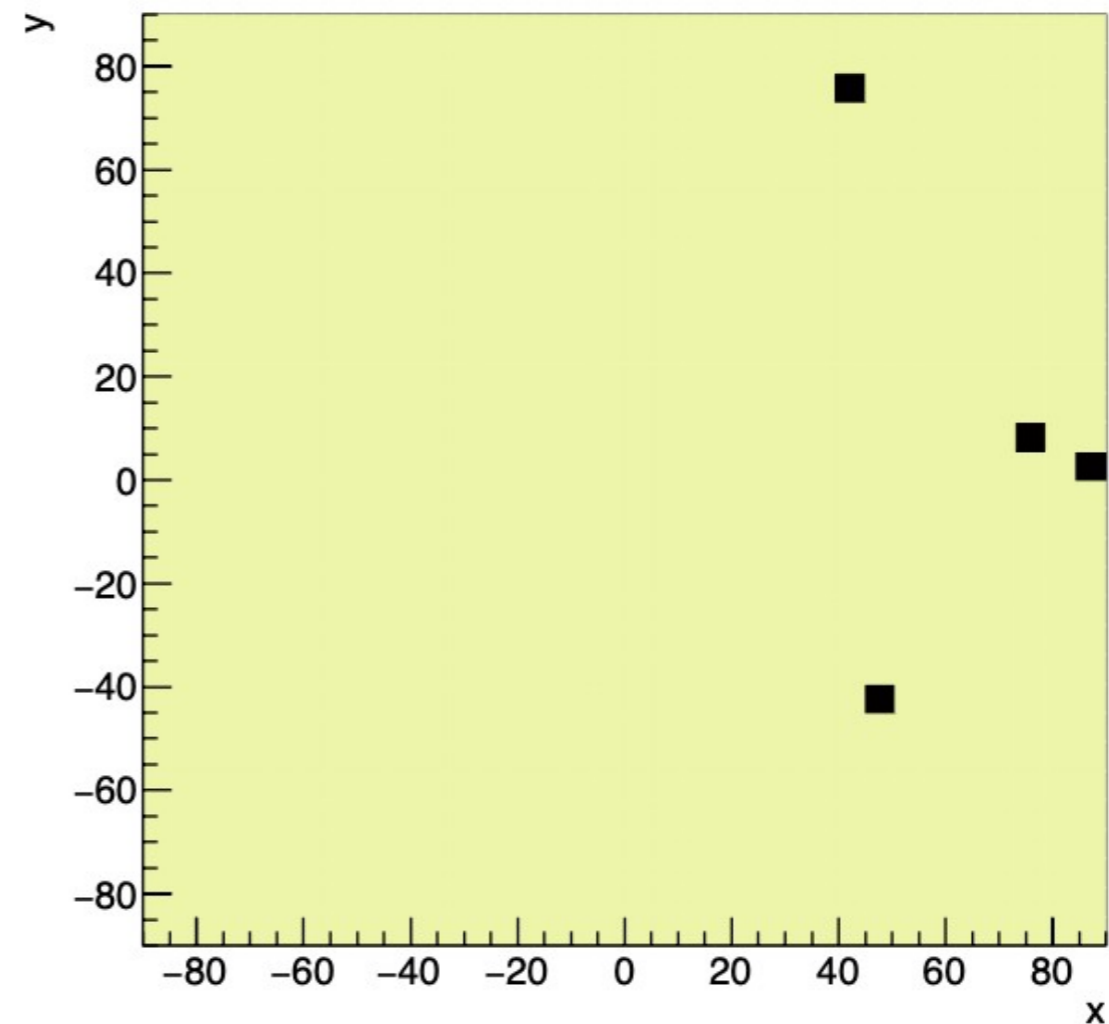
Typical slab: SlabID 30 (currently layer 1, 2021 production)

mask_x_y_SLB1



- Masked channels after lowering threshold to 275 DAC (~3/4 MIP)
- Short acquisition window 1ms
- Less vulnerable to noise and in particular to retriggering

mask_x_y_SLB1

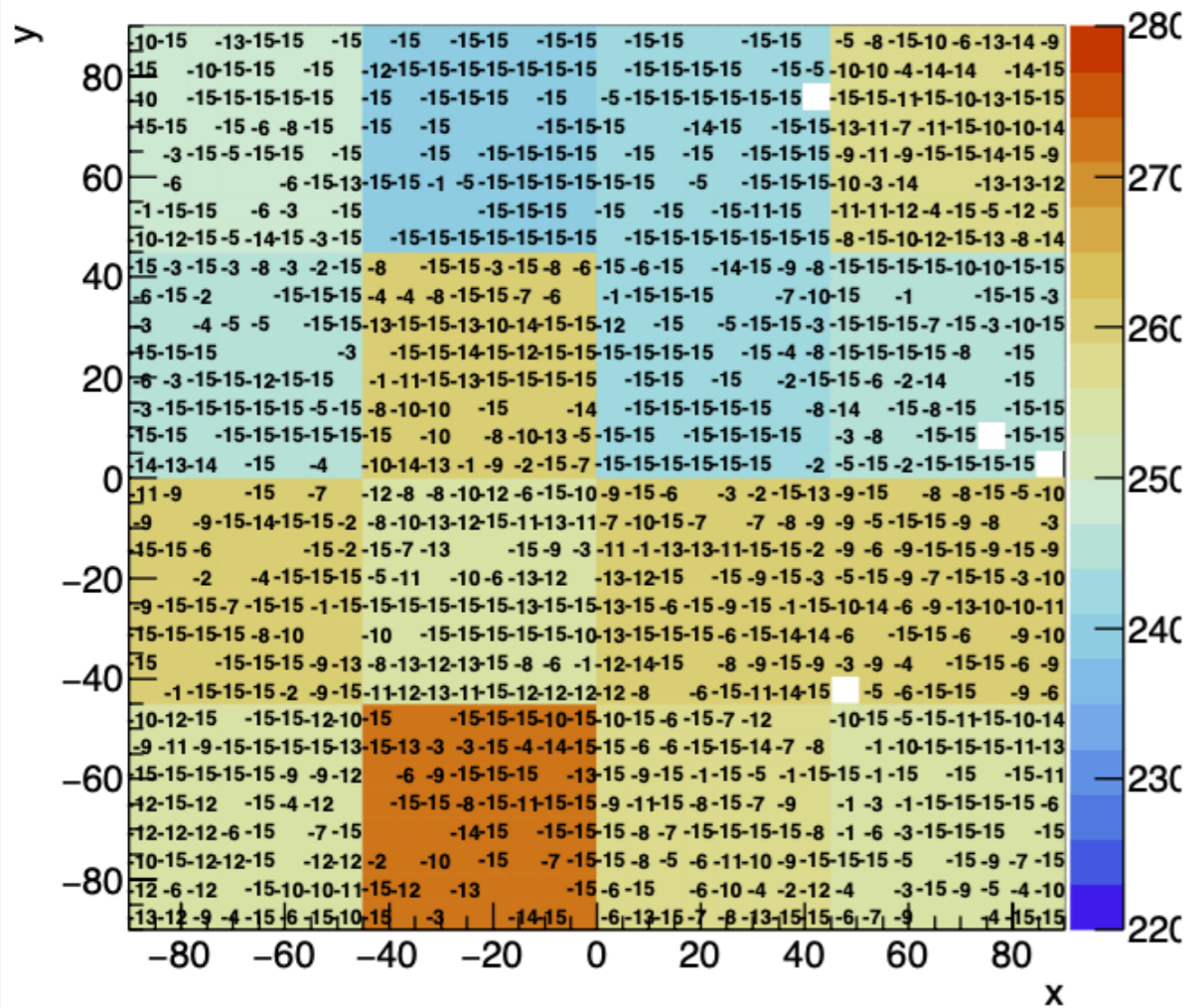


- Masked channels after lowering threshold to 275 DAC (~3/4 MIP)
- **Long** acquisition window 100ms
- Vulnerable to noise and in particular to retriggering

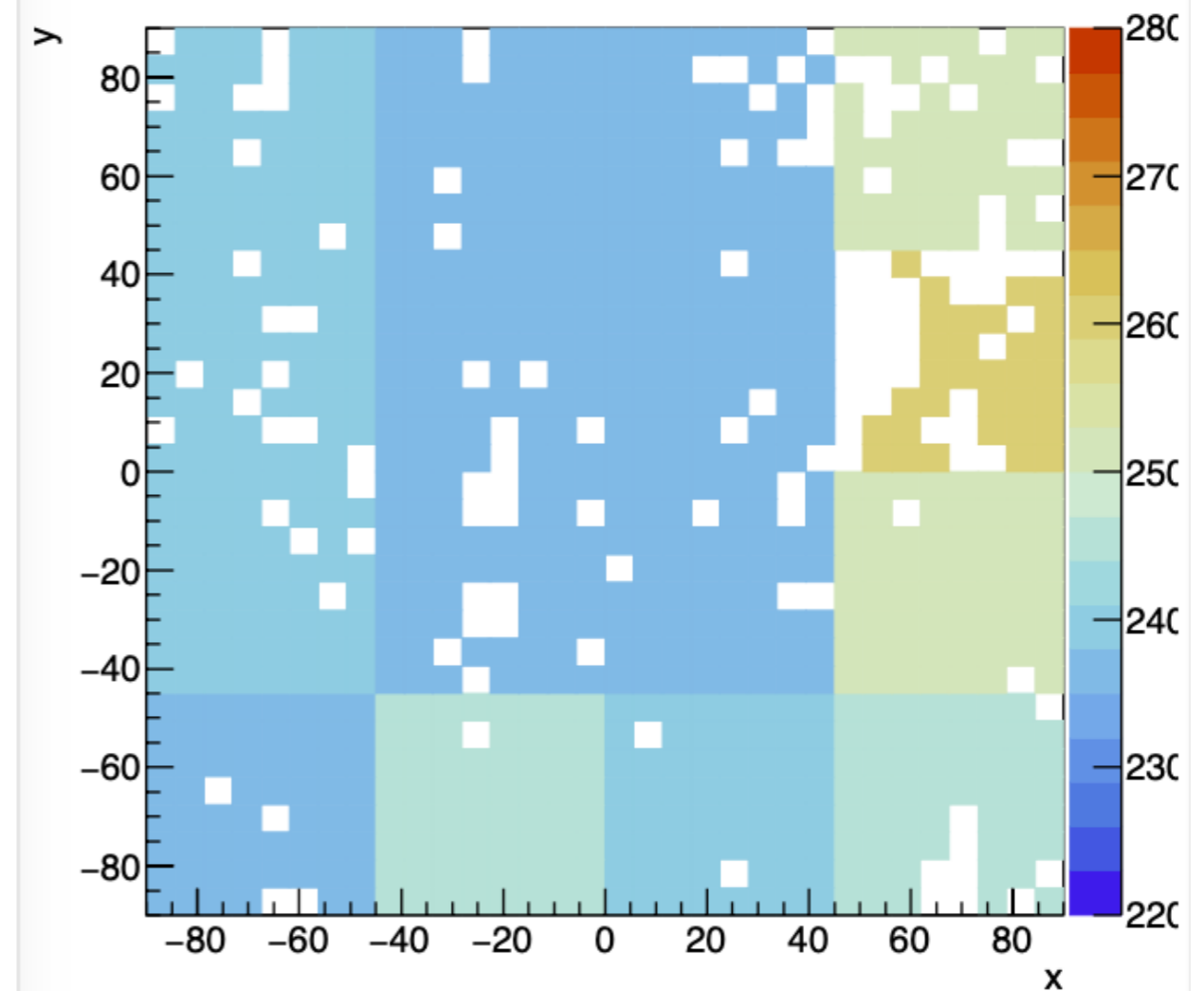
SlabID 30 equipped with SK2a => fine tuning possible

SlabID 21 equipped with SK2

threshold_x_y_global_1



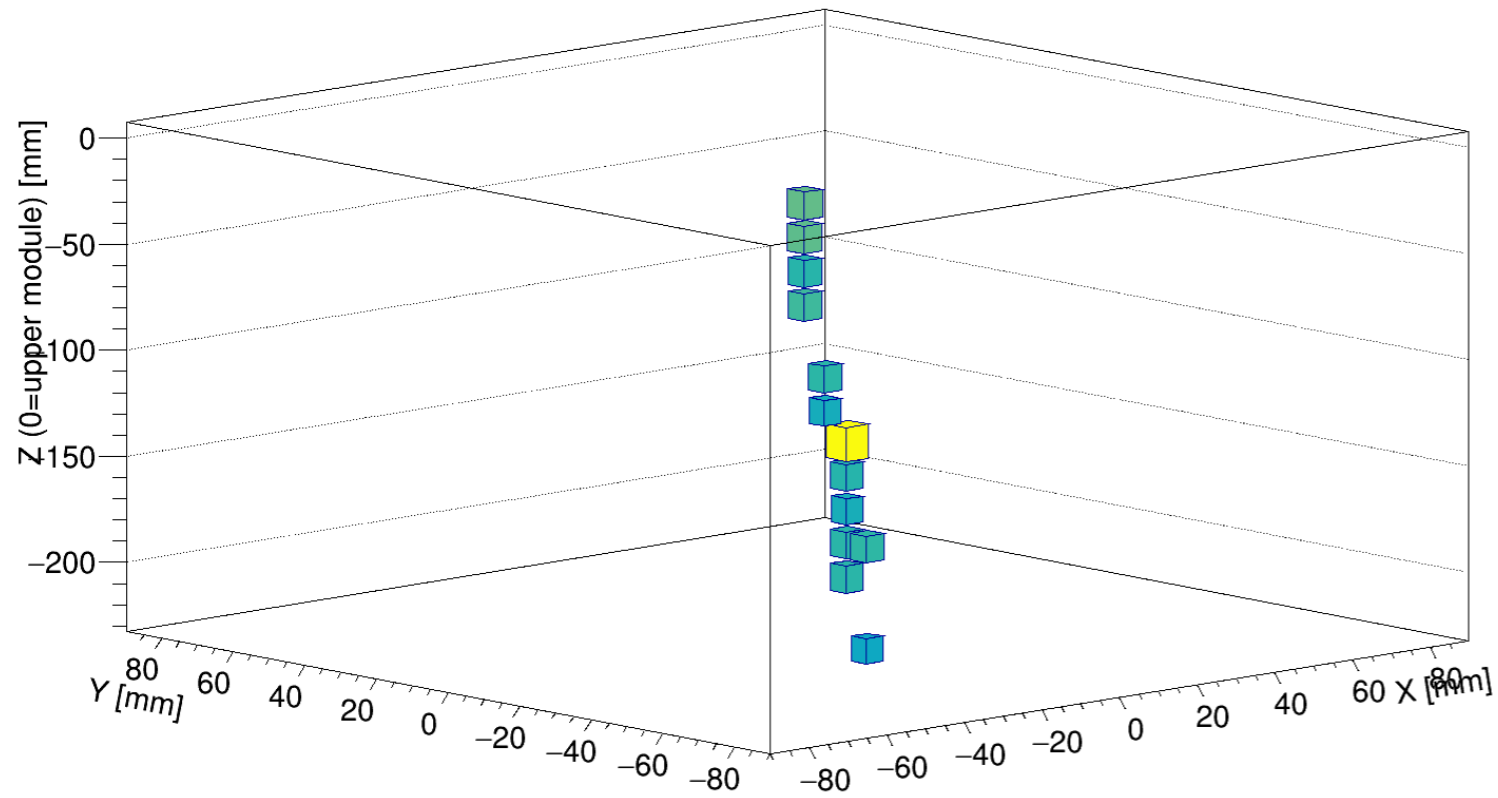
threshold_x_y_global_8



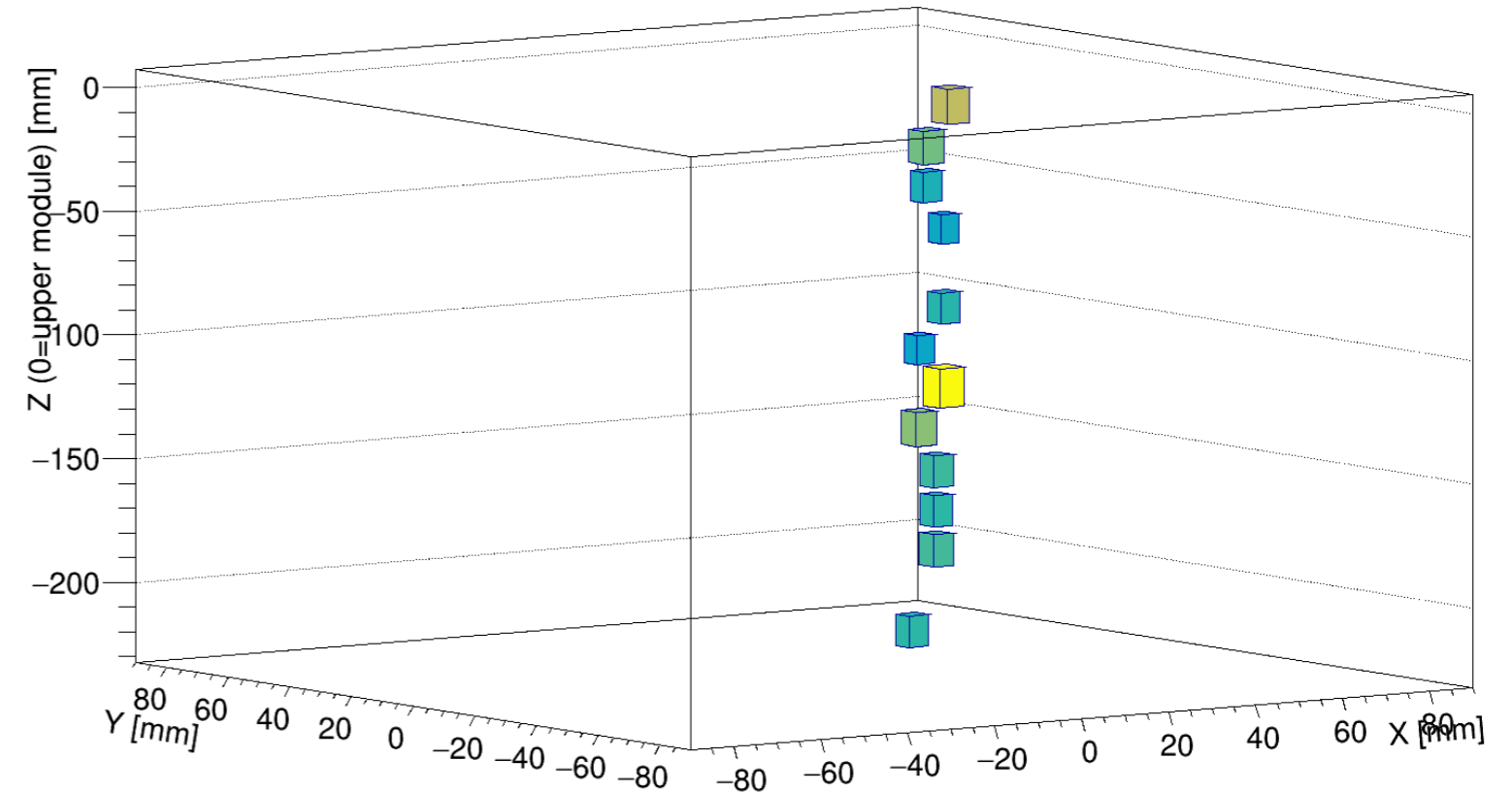
- Thresholds ~250 DAC on average
- On the high side but final interpretation after full analysis (new layer)

- Thresholds <250 DAC on average
- Roughly as expected
- Increase toward readout board (already seen earlier)

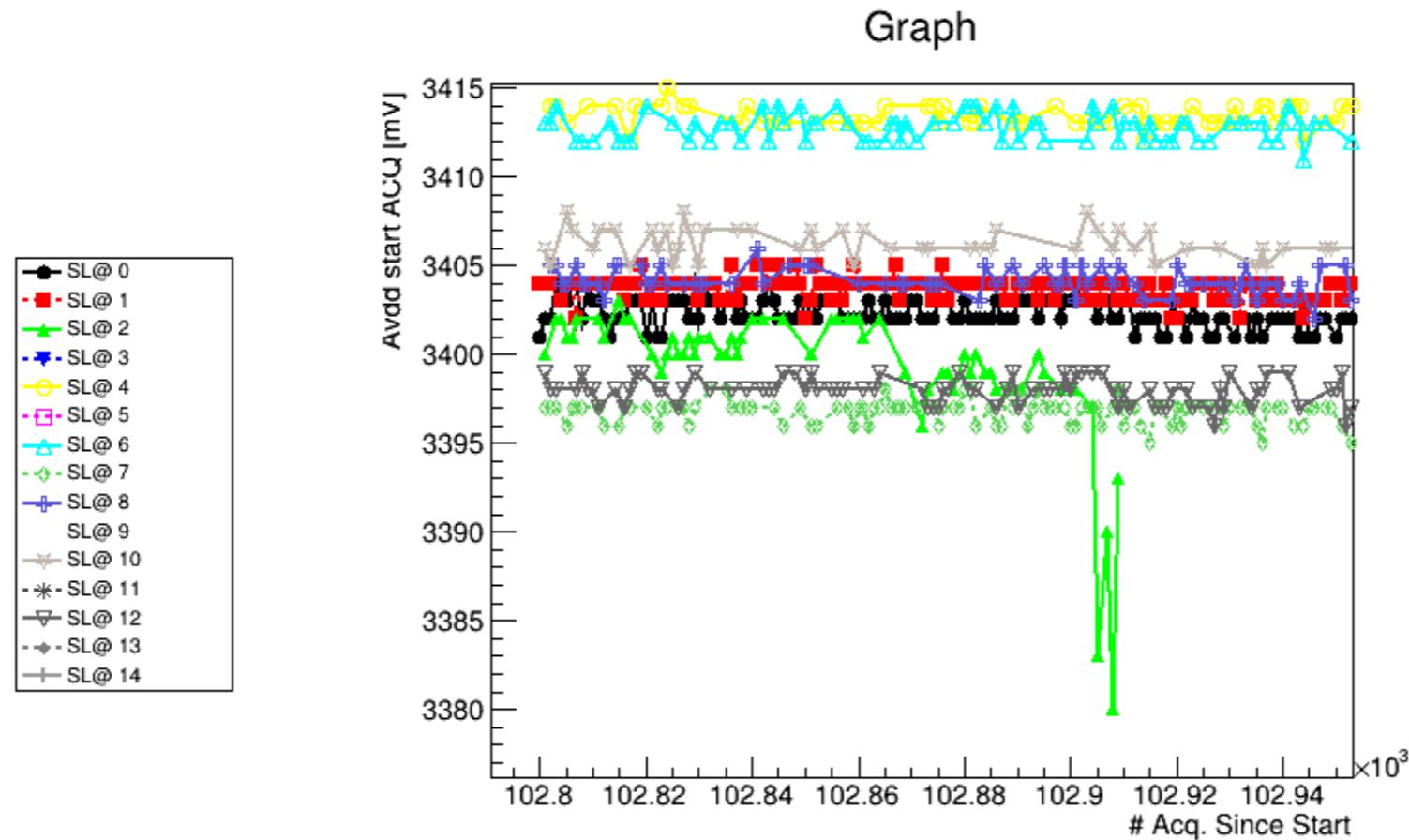
event_display_coinc_xyz_1



event_display_coinc_xyz_7



- **Cosmics seen**
- **Next steps**
 - More detailed analysis of cosmits
 - Refinement of masking procedure and threshold settings (where possible)
 - Hold scan
 - Gain intercalibration

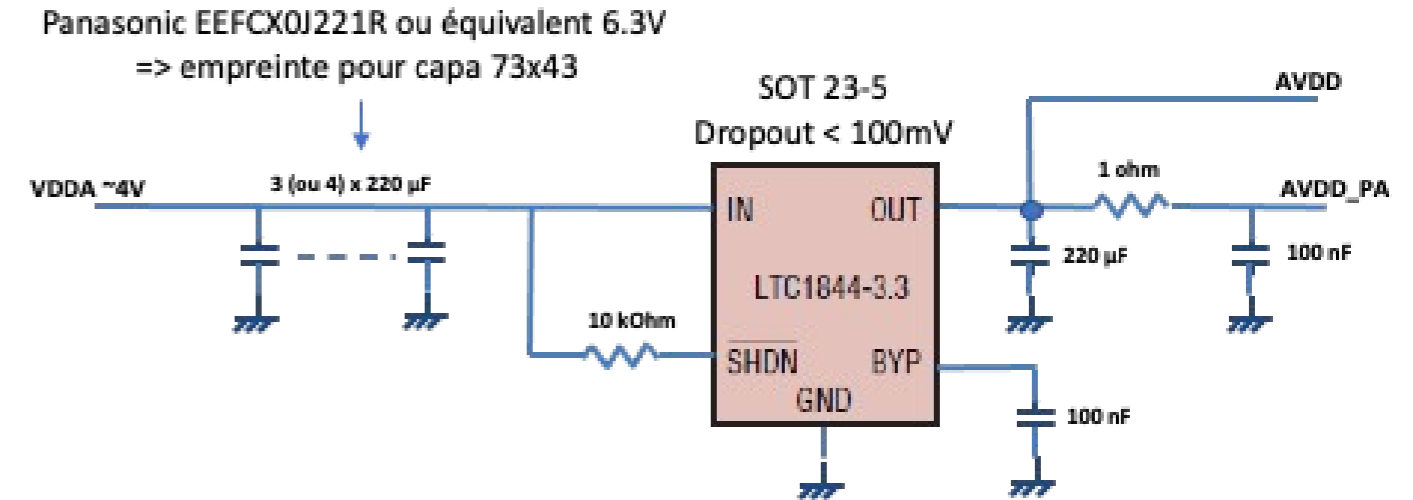
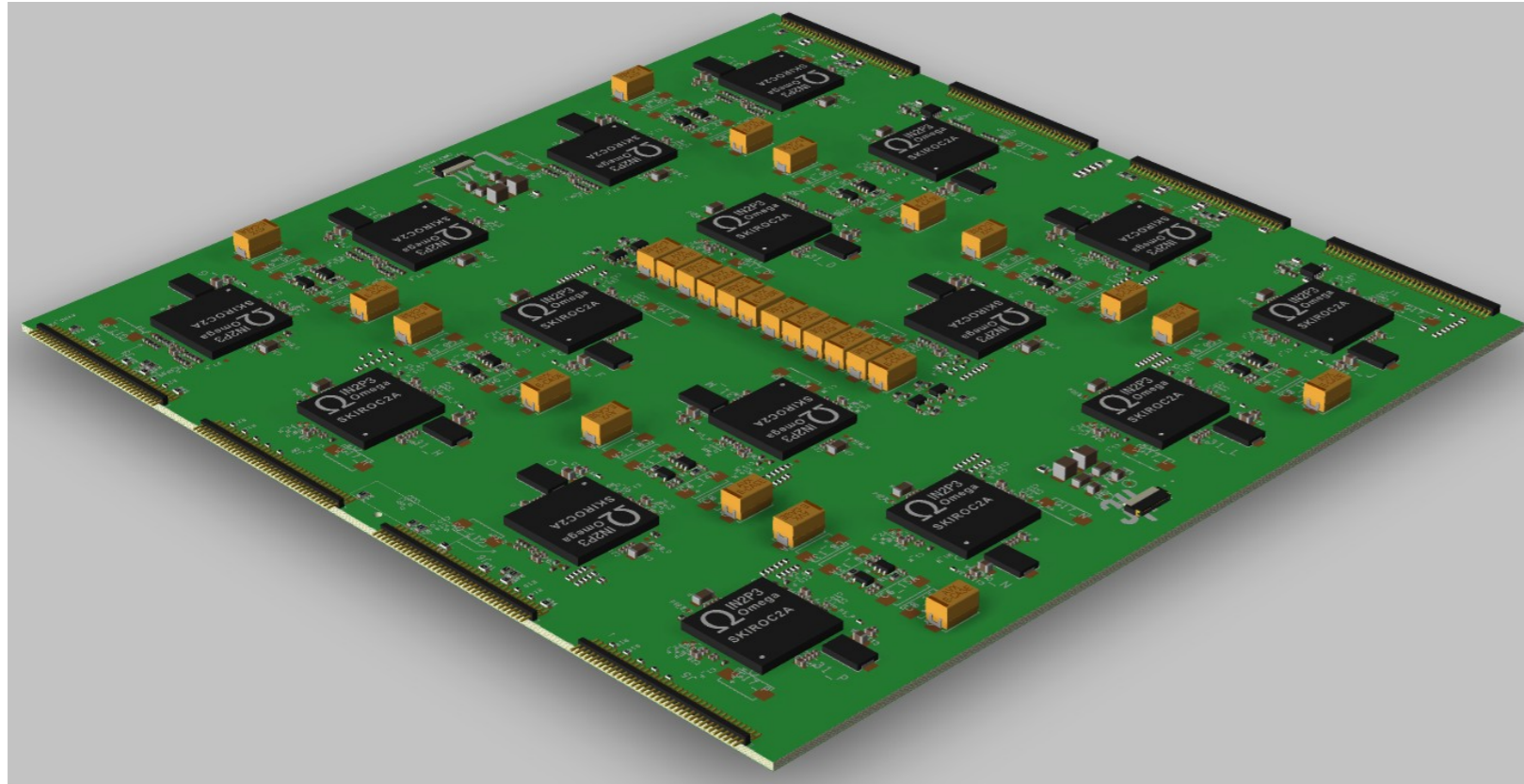


- One slab (ID13) died during cosmic run on 10/07/21 at 3am (!!!) CEST
- Slow control data show correlated voltage drop
 - Also HV power supply in weird state on Monday morning
 - 2A Fuse on SL Board got blown
 - First debugging revealed short cut between AVDD and GND on ASU
 - Reason (still) unknown

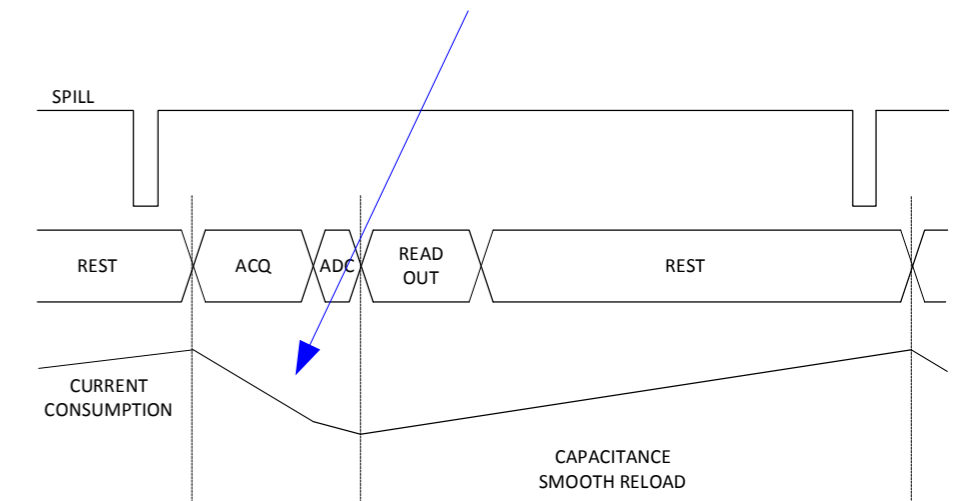
- Two FEV COBs delivered to CERN Bond lab for ASIC Boding on 1/7/21 (expect back next week)
 - For these two we have a metrology sheet and can thus follow the occurrence of deformations
 - Expect back next week
 - These are supposed to go into the stack and replace some layers (if quality is satisfactory)
 - Decision during september
- Setup can also be completed by FEV13
- Conclusion, if Slab ID 13 is really damaged we have means to complete the stack
 - However, will try to identify root cause of damage and nature of damage
 - Hopefully the accident will teach us some lesson
- at least, setup of proper interlock and slow control systems for beam test

- SiECAL slot **1/11/21 – 15/11/21** just after l'AHCAL (if Covid-19 will permit:-()
 - Rough planning is 1.5 weeks of standalone data taking
 - Exercising of common data taking in remaining 0.5 weeks
 - N.B. : First survey revealed that IJCLab engineers will not be able in the week of 25/10/21 (during AHCAL running)
- Survey for presence at beam test will be launched soon
- Will also regularly review s/w status

Status after regular discussions between engineers of LLR, IJCLab, LPNHE and OMEGA

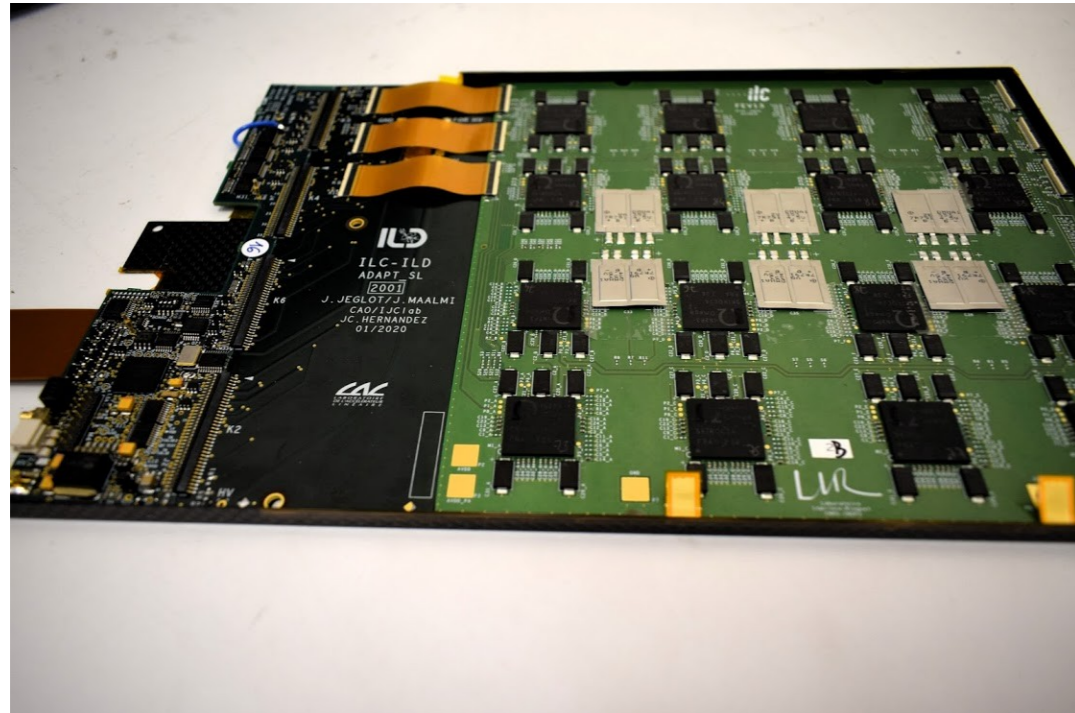


With 600 μF , we ensure 100mA during 3ms with a voltage drop of 0.5V ($\Delta V = I.t/C$).

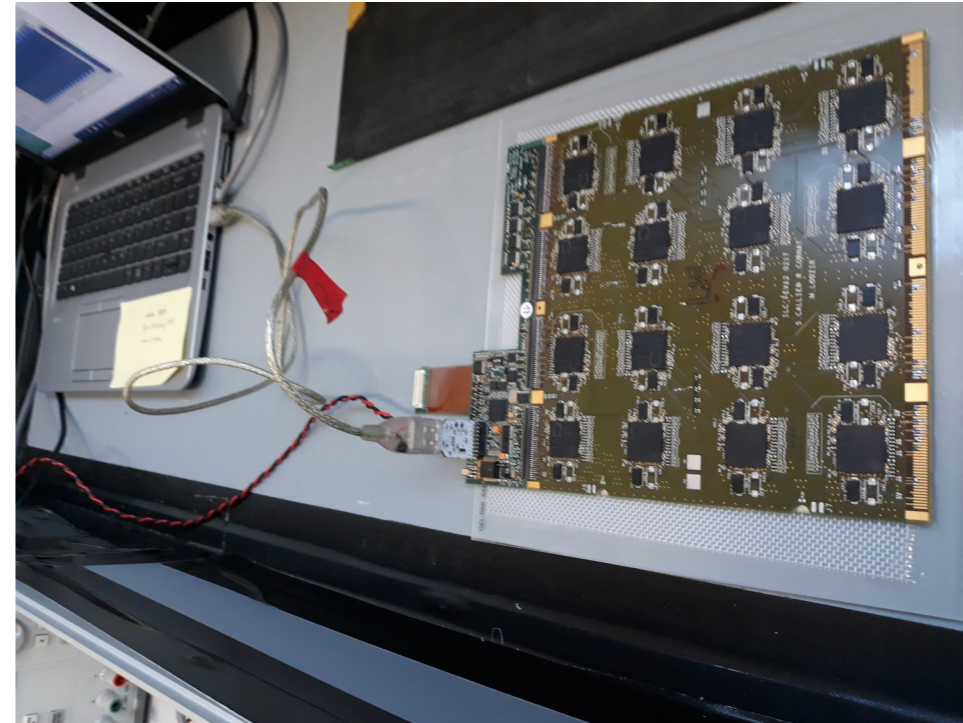


- **New board for next step of technical realisation of power pulsed Ecal layers**
 - Capacitances and LDO close to ASICs
- **Last month progress in design**
 - Stacking of PCB
 - Choice of components
- **Another important feature is that HV will be transported via connectors (i.e. On top of board)**
 - Wafer supply from bottom of board via plies (copper/kapton)
 - These plies are a delicate piece
 - Risk of shortcuts and wafer damage (the design of the kapton that goes below the board requires another design round)
- **Expect production either shortly before or shortly after the summer break (not in a hurry, carefulness comes before speed)**
- **The setup will be completed by a "Termination card" that will allow for flexible chaining of cards (i.e. No soldering of terminations)**
- **and for flexible adding of decoupling capacitances (to study noise behaviour of COBs)**

Backup



FEV13 connected via interface card to SL-Board



New FEV12 on single slab test bench

- **Interface card for allows for integration of FEV13 in stack**
 - Successful technical tests in Autumn 2020
 - In total 7 FEV13 equipped with wafers are available in F and JP
- **Started to deploy Hardware/software for digital readout (i.e. SL-Board and User Interface) to other Ecal groups**
 - First “client” LLR
 - **IFIC will follow during visit of Adrian end of May/June, as soon as travel will be possible**
 - **In preparation of deployment to Japan is planned**

SLAB	DESY 2017		CERN 2018		Comments and 2021 status
	status	calibrated cells	status	calibrated cells	
13		0%		0%	Glue spilled in the SMBv. Recovered for 2020, Short cut 10/07/21
14		0%		0%	Error in the SR return → fixed
15		0%		0%	Stopped working during the 2017 commissioning. recovered for 2021
16		92%		?	Delaminated wafer, repaired at LPNHE in 2021
17		93%		95%	Delaminated wafer, repaired at LPNHE in 2021
18		94%		?	At CERN : a pattern of lower MIP values is seen in the center of the ASU.
19		93%		93%	
20		94%		96%	
21		54%		0%	Stopped working at DESY 2018. Fully recovered for 2021
22		84%		87%	
23		0%		0%	FEV10 Never used → operational now.
24					FEV12 (Summer 2019)
25					FEV12 (Summer 2019)
26					Damaged COB with only one wafer
27					Damaged COB with only one wafer
28					COB : One Chip broken, operational and ready for gluing but bent
29					COB : Operational and ready for gluing but bent
30					FEV12 freshly produced in Autumn/Winter 2020/21
31					FEV12 freshly produced in Autumn/Winter 2020/21

Slabs < Slab24 are FEV10 or FEV11

15 Slabs setup 02/06/21

coreKapton slot	Layer position	Slab ID	ASU type	wafer	front end (slboard ID)	Glissiere neded for the W	W in front (mm)	X0	X0 (acc)	Comments/Issues
14	0	31	FEV12	500						
shot 13	1	30	FEV12	500						
12	2	13	FEV11	320	10	2.1mm	2.1	0.6	0.6	
11	3	14	FEV11	320	5	2.1mm	2.1	0.6	1.2	
10	4	15	FEV10	320	1	2.1mm	2.1	0.6	1.8	
9	5	19	FEV11	320	13	2.1mm	2.1	0.6	2.4	
8	6	20	FEV11	320	11	2.1mm	2.1	0.6	3	
7	7	24	FEV12	500	7	2.1mm	2.1	0.6	3.6	Stable AVDD ??
6	8	21	FEV11	320	14	2.1mm	2.1	0.6	4.2	
5	9	25	FEV12	500	3	2.1mm	2.1	0.6	4.8	problems communicating the ID of the SLboard ?? (SOLVED)
4	10	22	FEV11	320	4	4.2mm	2.1	0.6	5.4	
3	11	23	FEV10	320	6	4.2mm	4.2	1.2	6.6	
2	12	16	FEV11	320	9	2.1mm	2.1	0.6	7.2	
1	13	17	FEV11	320	2	4.2mm	4.2	1.2	8.4	problems communicating the ID of the SLboard ?? (SOLVED) Stable consumption ?? -> SOLVED shortcut in DVDD (capacitance in skiroc 14)
0	14	18	FEV11	320	0	whatever (no W will be added)	4.2	1.2	9.6	