AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

FLAME ASIC for luminosity calorimeter for future e+e- collider

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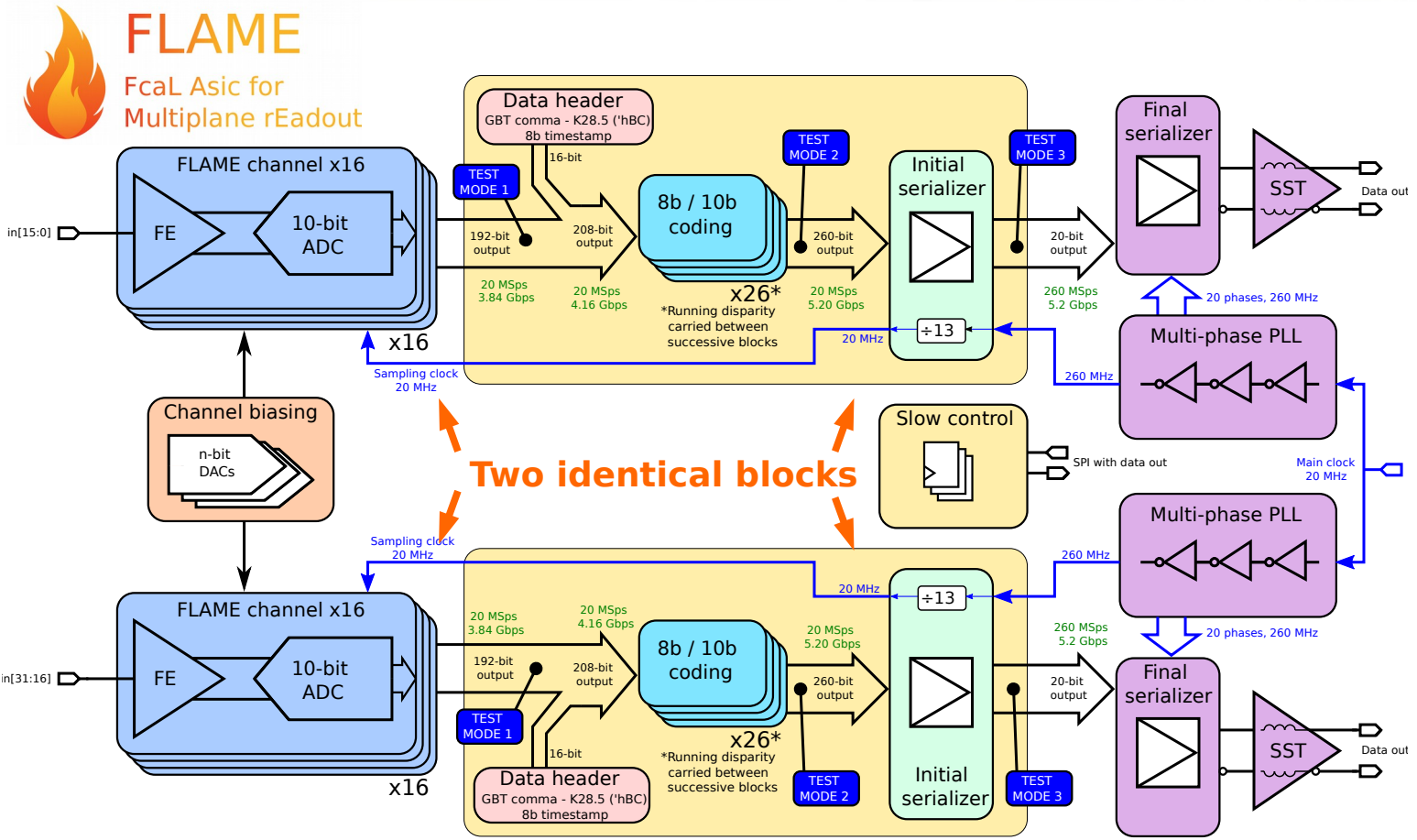
25 November 2021, Beam calorimeters and beam monitoring

Outline

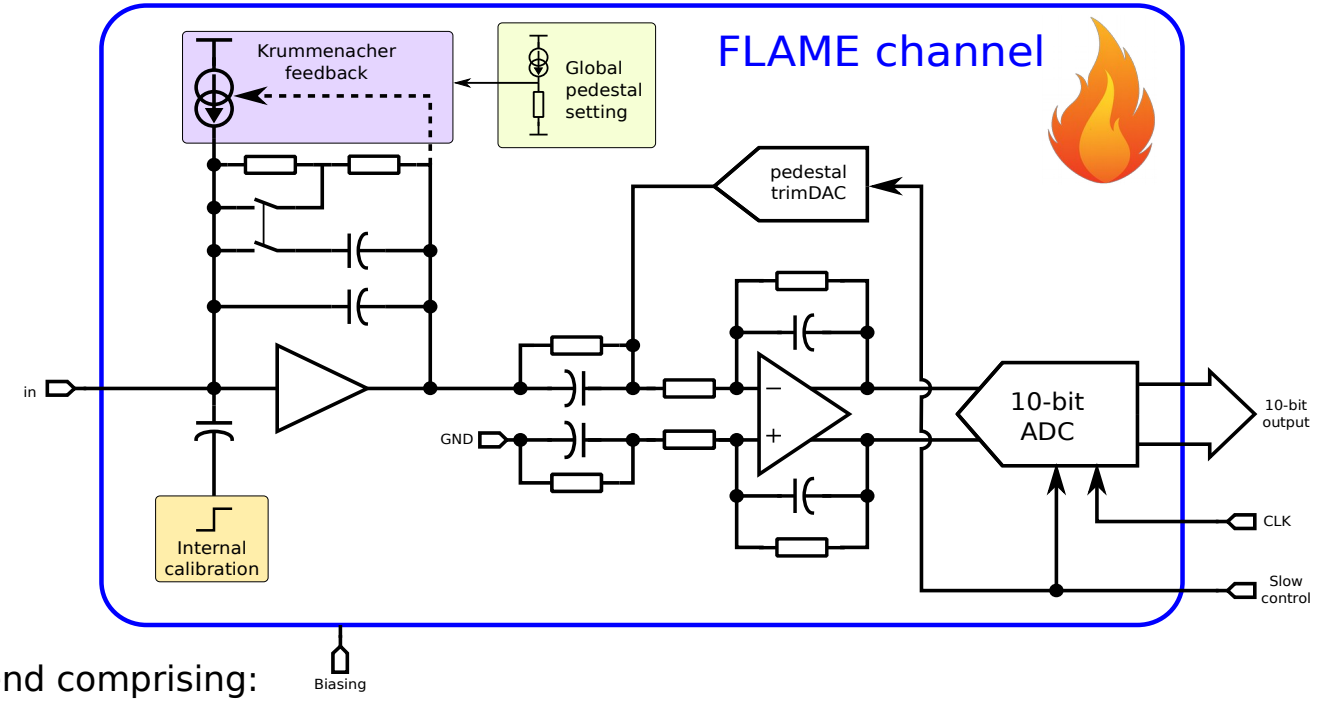
- FLAME ASIC for luminosity calorimeter in LC
- FPGA-based FLAME readout
- First Test-beam with FLAME
- Summary and Plans

FLAME Readout ASIC Architecture



FLAME is a 32-channel ASIC, designed in CMOS 130 nm, containing FE+ADC in each channel, followed by high speed serializers and data transmission.

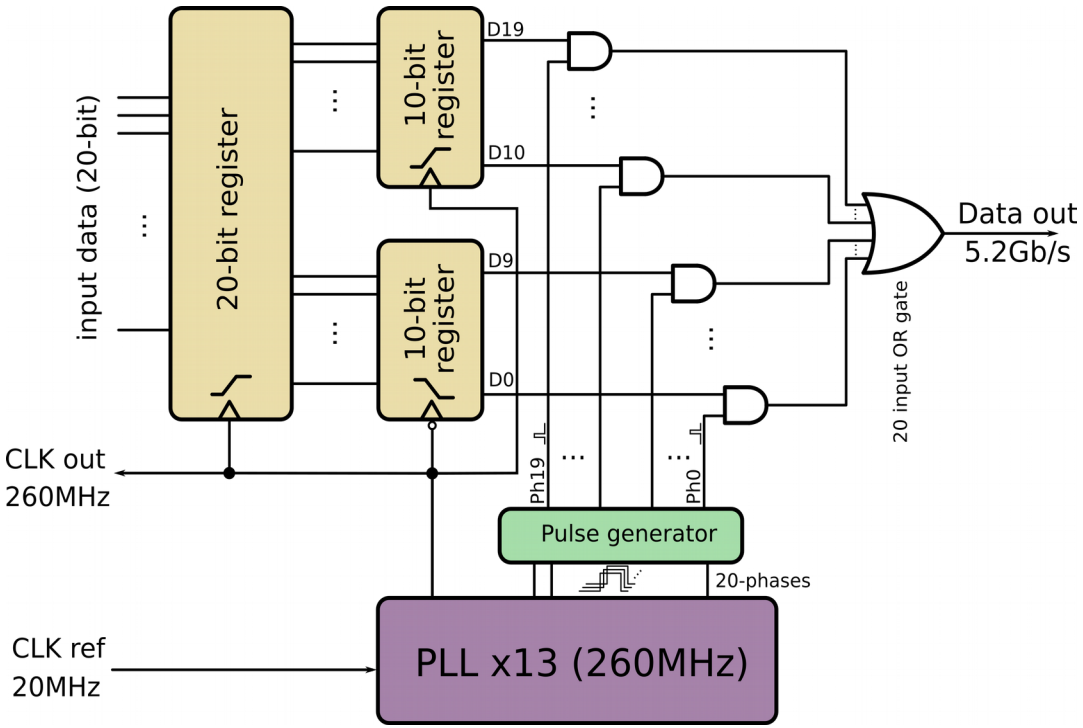
FLAME Readout ASIC
Single channel architecture



- Analogue front-end comprising:
  - Charge sensitive preamplifier with variable gain:
    - High gain – for MIP sensitivity (up to ~200fC)
    - Low gain – for shower measurement (up to ~6pC)
  - Default detector capacitance ~20-40pF
  - Differential CR-RC shaper with ~50ns peaking time – **for amplitude and time measurement using deconvolution**
  - Krummenacher feedback
  - Internal calibration and pedestal trimDAC
  - Power consumption ~1mW

- 10-bit SAR ADC in each channel
  - Default sampling rate 20MSps (max. up to 50MSps)
  - DNL, INL < 0.5 LSB
  - ENOB > 9.5
  - Ultra low power consumption (<1 mW/channel@40 MSps <0.5mW/channel@20MSps)

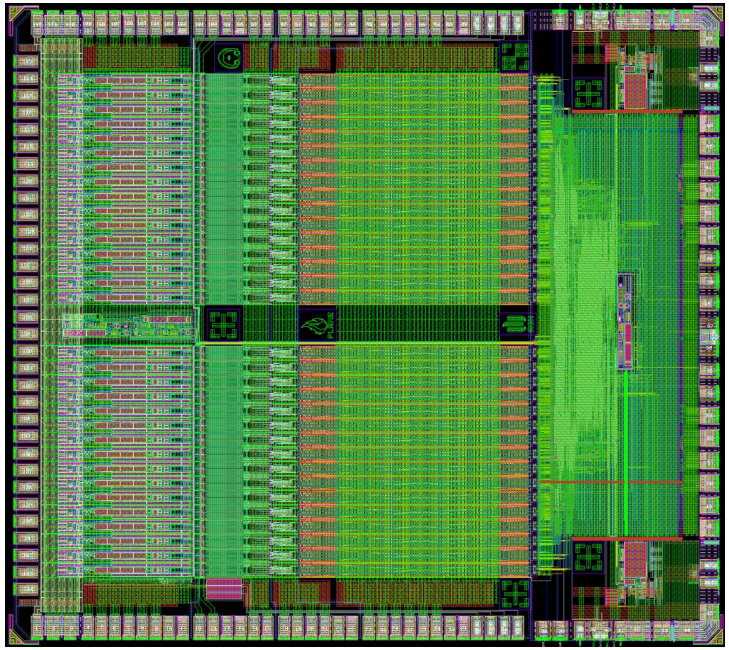
FLAME Readout ASIC
Fast serializer architecture



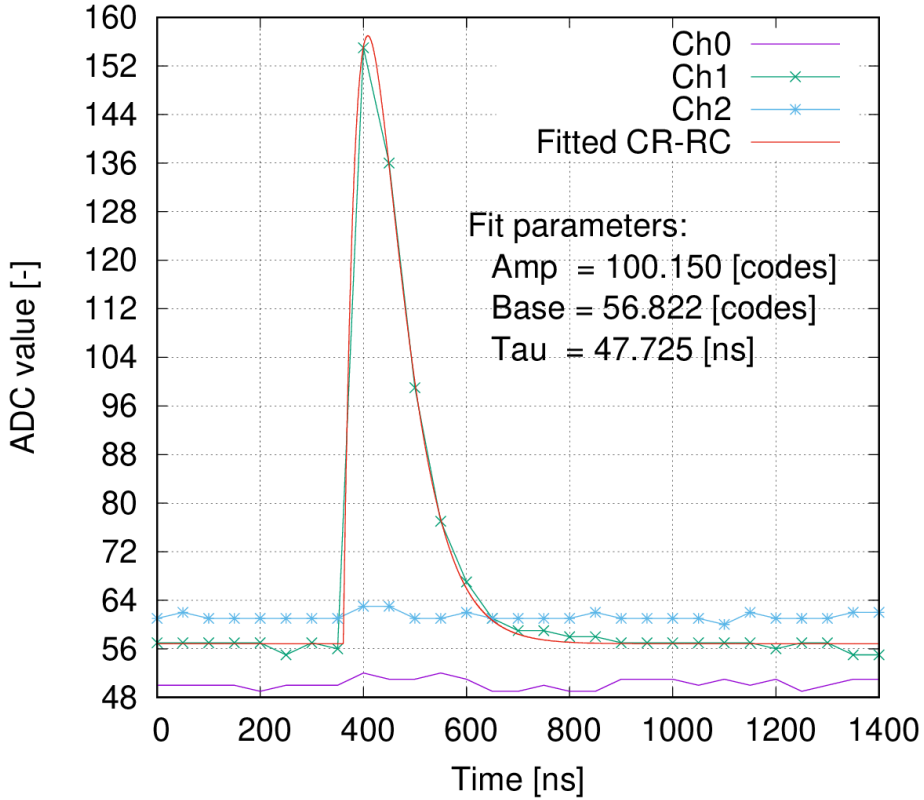
- Serialization based on 20 uniformly distributed phases of PLL clock
- PLL generates 260MHz clocks from 20MHz reference (x13)
- Data muxed by 20 narrow pulses (~200ps) passing data bits through NAND gates
- Two levels of data registers for better time margins
- Single hase 260MHz clock output for initial serializer
- 5.2 Gb/s output data rate

Two copies of serializer are implemented in FLAME, each one for 16 channels

FLAME Readout ASIC
Prototype fabrication and First Lab tests



FLAME size 3.7mm x 4.3mm



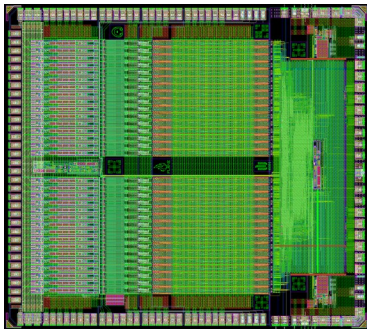
FLAME was fabricated in 2019

All basic functionalities (comprising fast data transmission) were verified

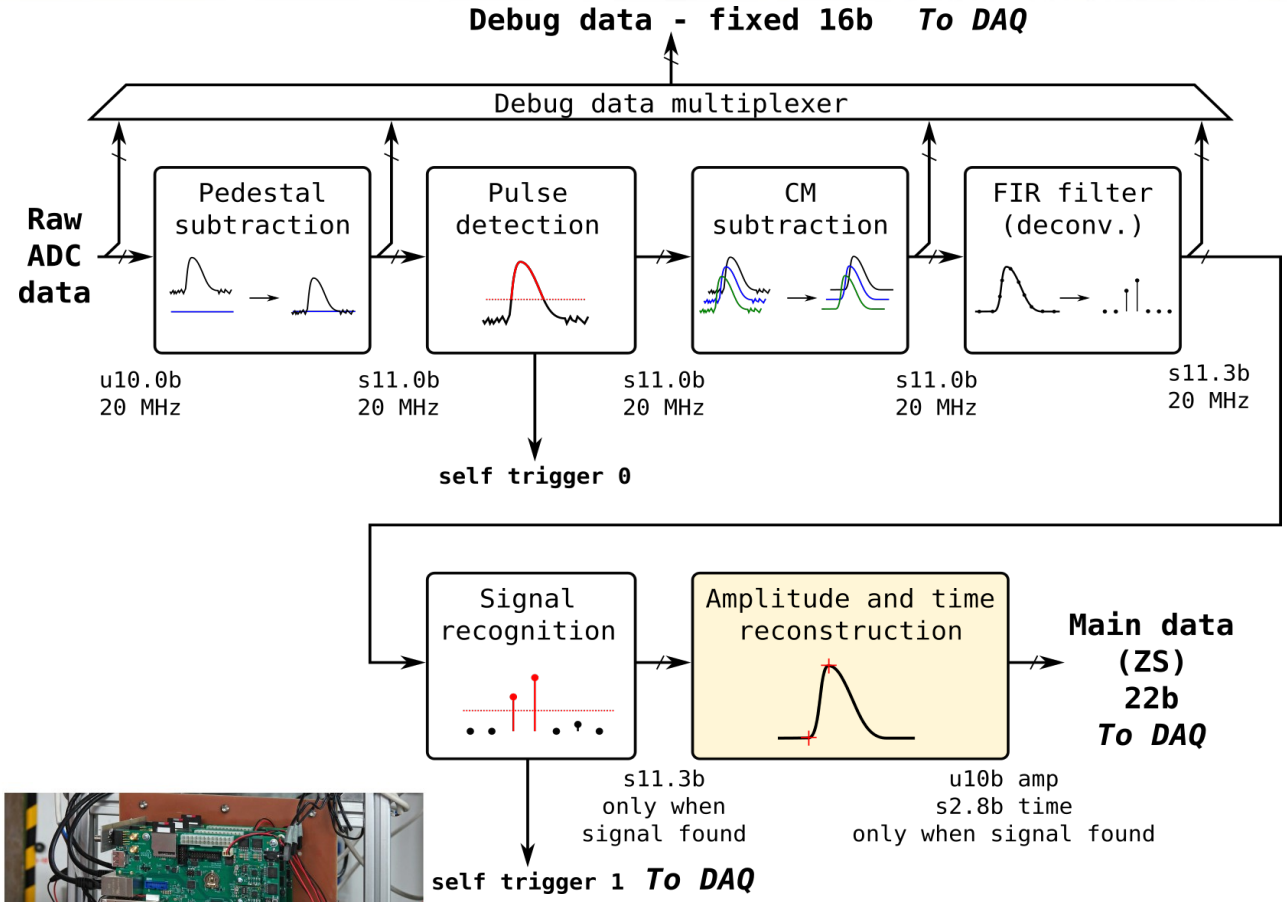
Very good pulse shape was measured, matching with CR-RC shaping

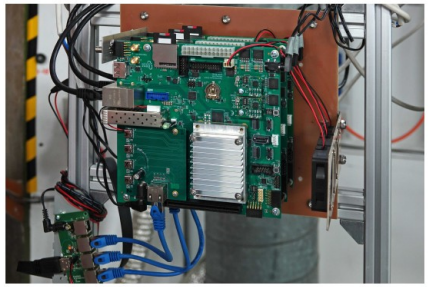
Power pulsing can be used (Digital&ADC OFF, Analog Zero biasing) – to be verified

FPGA-based FLAME Readout
Architecture of FPGA back-end



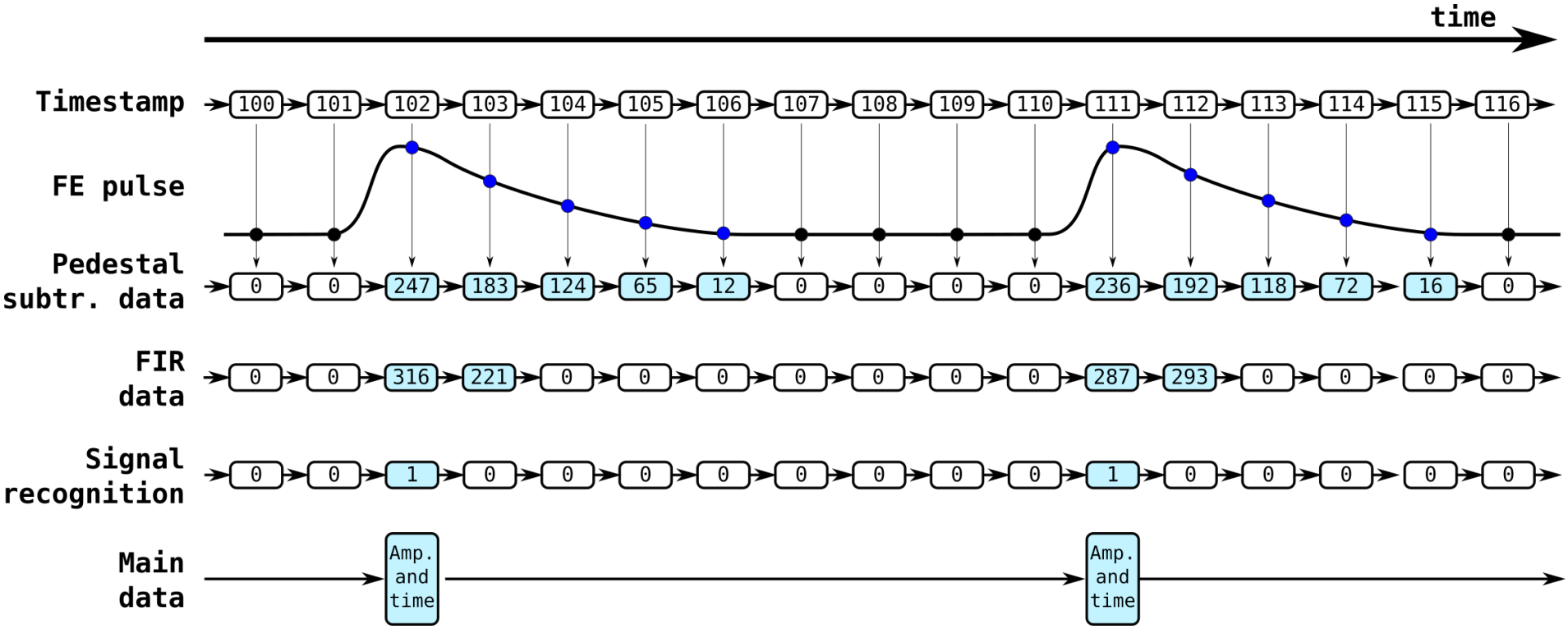
FLAME serializers send data to GTH transceivers of Zynq UltraScale FPGA for online processing





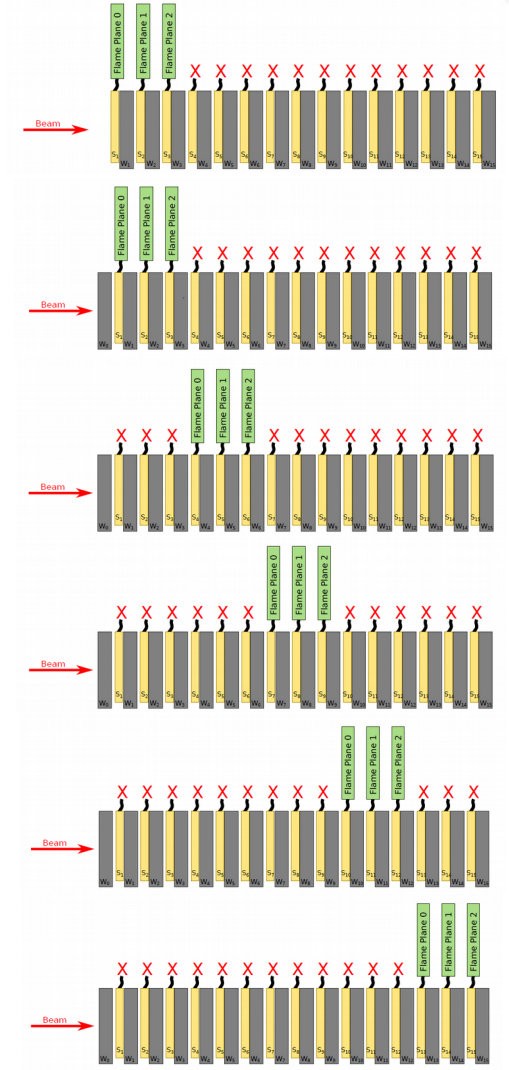
Reconstructed amplitude (10-bit) and time of arrival (~1 ns) information of detected pulses are sent to DAQ system

FPGA-based FLAME Readout
DSP online processing

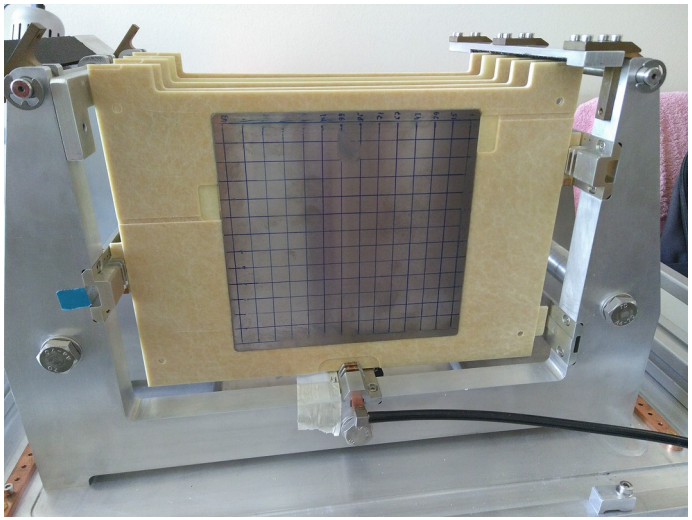


FLAME can work asynchronously to the beam, and such scheme is used in FCAL test-beams. Deconvolution decreases the S/N of the reconstructed amplitude by ~15%, while expected time of arrival should have ~1 ns precision (to be verified experimentally)

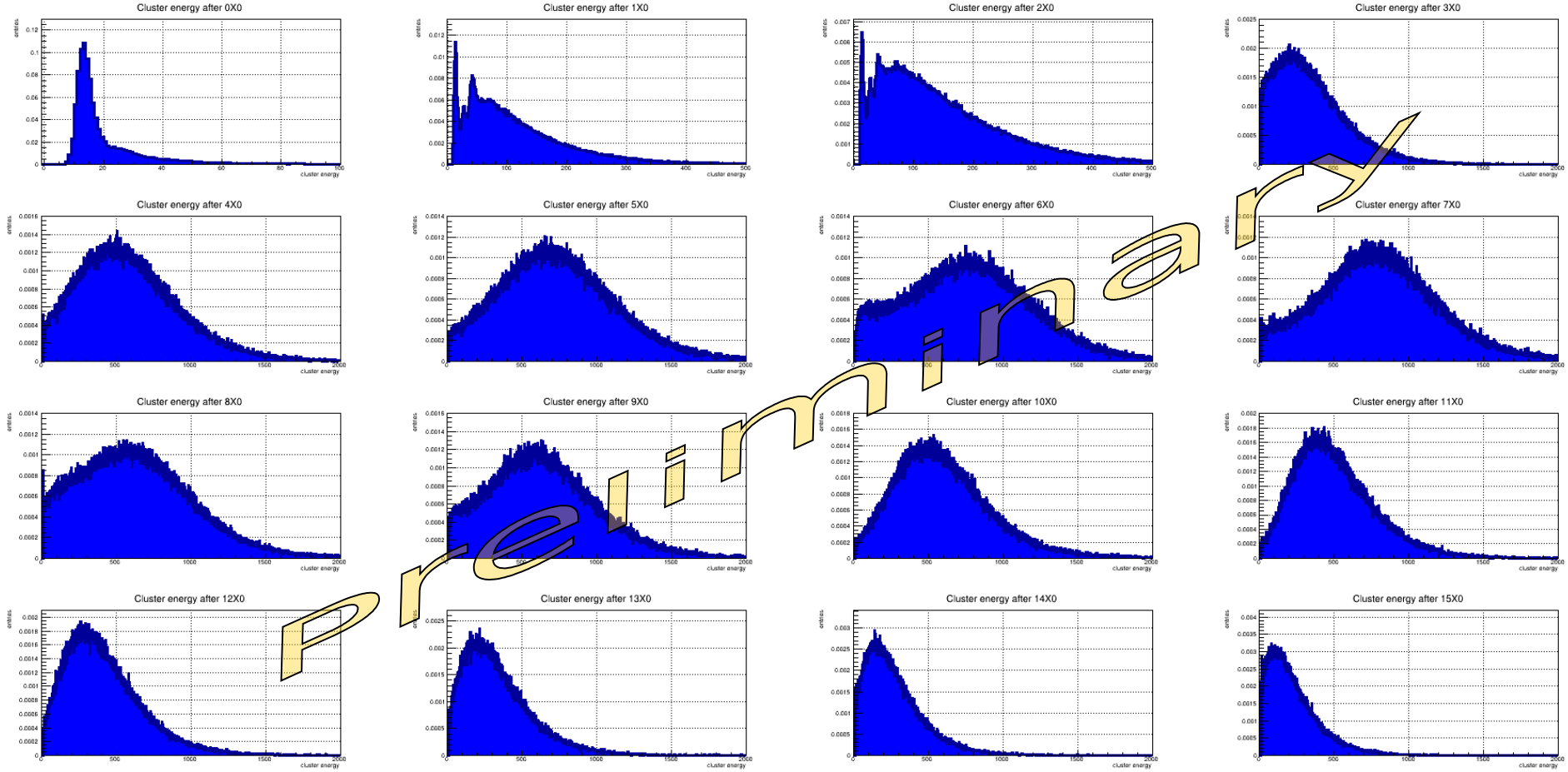
Test-beam with FLAME in 2020 at DESY
FLAME readout setup and configurations



- In march 2020 at DESY a test-beam (1-5 GeV) with 16 tungsten plates and silicon sensors was made
- 3 readout boards with FLAME chips (each board with 128 channels = 4 FLAMEs) were connected
- To study the shower development in the entire calorimeter, the 3 FLAME boards were successively connected to the next sensor layers
- Shower development reconstruction in the whole stack was done offline by merging data from different configurations



Test-beam with FLAME in 2020 at DESY
Cluster energy vs radiation length



Energies deposited up to 15 radiation lengths were measured. Some noise cuts still under tuning...

Summary and Plans

- Dedicated FLAME readout ASIC with FPGA-based back-end were developed for luminosity calorimeter
  - FLAME operation was verified in the Lab and on the Beam
  - Two weeks ago we used FLAME readout at DESY to study the performance of new GaAs sensors and compare it to CALICE silicon sensors – in both cases Landau distributions for MIPs were obtained
- Presently we are preparing a modified FLAME version for LUXE experiment
  - Digital serialization and data transmission circuitry will be significantly simplified since very low trigger rate and output data rate is needed in LUXE

Thank you for attention