ILD: Trigger & DAQ

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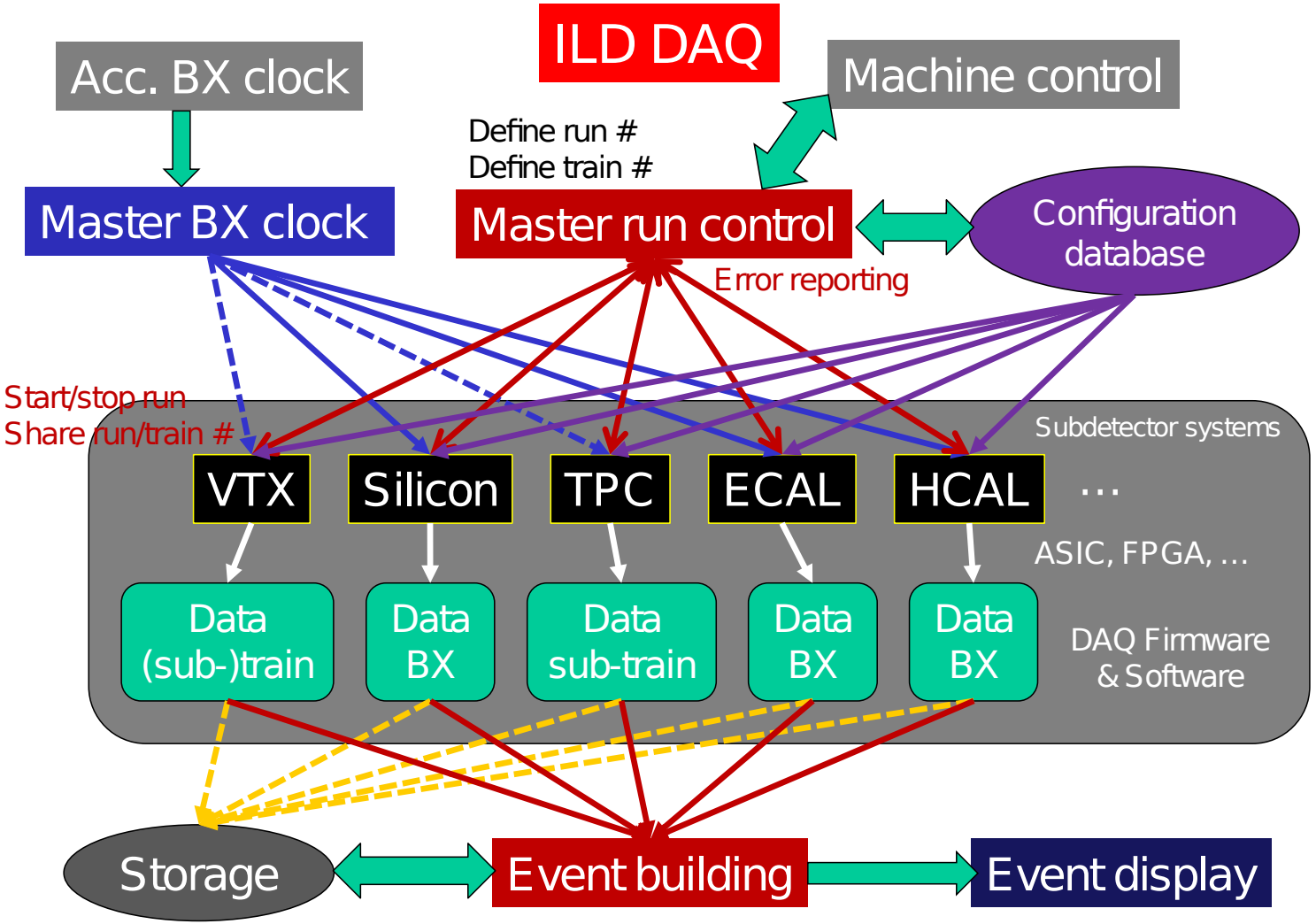
Introduction: Status

- Disclaimer: this is a limited view a limited understanding of all aspects in all subdetectors
- Last comprehensive overview: Taikan's talk at ILD meeting in Ichinoseki 2018
- Status: **Conceptual design** without big level of detail
  - Very far from the final design of the hardware and software
  - My personal problem definition: engineering (and coordination) needed more than R&D of new technology
  - ILD represents significantly smaller problem compared to LHC experiments in terms of datarates and (no) trigger
  - No driving force in the Top-down direction
- Limited efforts towards commonalities:
  - Very front-end electronics ROC: signal conditioning, self-trigger/zero suppression, time-stamping, digitization
  - (CALICE specific?) CCC (Clock and control card) demonstrator (UCL)
    - Older, concept of fast commands, HDMI cables
    - Individual (calo) detector prototypes diverged from this effort
  - Prototyping and testbeam: TLU, EUDAQ, Caribou
  - … ?


ILD DAQ
Acc. BX clock
Machine control
Define run #
Define train #
Master BX clock
Master run control
Configuration database
Error reporting
Start/stop run
Share run/train #
Subdetector systems
VTX
Silicon
TPC
ECAL
HCAL
...
ASIC, FPGA, ...
Data (sub-)train
Data BX
Data sub-train
Data BX
Data BX
DAQ Firmware & Software
Storage
Event building
Event display

What are the ILD DAQ tasks?

- **Low-jitter Clock** distribution and **BX clock** distribution (discussed later)
- **Control** of subdetectors from a master Run control
  - Both on hardware and software level
- Keep consistent and unique tagging (run nr, train nr, BX nr, …)
- **Hardware communication protocol specification**
- **Collection of data** and errors, **Transfer** to storage
- Configuration download and switch configurations. Slow control or DAQ?
- **Event building** (with reconstruction)
- Instant event display (is it software task already?)
- …?

Clock distribution

- Aim: Detector resolution <O(10 ps)
  - ToF requirement: Silicon tracker, Calo
  - Clock distribution requirement on jitter: <<O(10 ps)
- Clock strongly linked to the accelerator clock (RF cavities) ?
  - Cavity tuning during spill? what range, how fast process?
  - Concern: typical PLL / Jitter cleaner has a limited bandwidth
- Clock fan-out needs a careful design
  - delicate engineering or significant R&D ?
  - Synergies with other experiments expected, CMS example
- BX clock: regular interval?
  - If yes → can be used for the low jitter clock ?
  - If not → a complex problem of clock delivery and ROC jitter!
    - the BX time structure needs to be known in advance (How far in advance? Next train, witnin train?)

Trigger

- self trigger and zero suppression @ROC due to large number of channel
- Trigger not necessary due to (physics) hit low occupancy → **Everything is stored**
- Readout finished only before the start of new spill (~200 ms !)
- ILD Detector **feedback to the accelerator**?
  - Long latency from some detectors, needs to be identified
- Any ambition to **filter** out the noise (or beam background) **before** storage with the help of reconstruction?
- **Event building** & prompt reconstruction: Online Filter Farm
  - Processing a complete spill as a whole set on one node
  - Is it part of DAQ or computing?
  - Hardware acceleration required? (FPGA, neural network)

Data rates

- Numbers from ILC TDR (2013)
- Physics data after zero suppression: O(100 MB)/train
- O(10PB)/year storage
- Numbers need revisiting?
  - Is the beam background simulation in?
  - Concern: could specific layers systematically fill ROC local memory storage (due to more hits)
  - is the Channel→chip mapping in the simulation model accurate?
    - Help with the analysis/simulation welcome

Sub-detector	Channels $[10^6]$	Beam induced [Hits/BX]	Noise [Hits/BX]	Data volume per train [MB]
VTX (CPS)	300	1700	1.2	< 100
VTX (FPCCD)	4200	1700	1200	135
TPC	2	216	2000	12
FTD	1	260	0.3	2
SIT	1	11	0.3	6
SET	5	1		1
ETD	4			7
SiECAL	100	444	29	3
ScECAL	10	44	40	
AHCAL	8	18000	640	1
SDHCAL	70	28000	70	
MUON	0.1		8	Æ1
LumiCal	0.2			4
BeamCal	0.04			126**

Further questions on the tasks list

- **DAQ structure**: strong central DAQ or loose communication of subdetector DAQs
- **Calibration** synchronization
  - To be operated centrally or individually within subdetector?
  - Collection of muons when ILC is in downtime (for >>200 ms)
  - Light / charge injection / other – handled exclusively by subdetectors?
  - Calibration can be time consuming (and data volume)
  - Use time between spills? No (power/heating issues)
- **Thermal** management
  - Spill length affects power consumption
  - What operation changes / irregularities to be prepared for?
  - Part of slow control?
- Concern: Radiation dose during lifetime operation and the effect on the DAQ component
  - Do we have a simulation of the environment?
- **Radhard** interface/concentrator chip? (FPGA might not be sufficiently resistant)
  - CERN has experience in this field – could we adopt/reuse results of existing development

Summary

- Effort needed:
  - Clock distribution
  - Concept of DAQ architecture and run control
  - Feedback to accelerator
  - Data rates numbers
  - Identification of common concentrators and links
  - (Event building)
- Still learning...