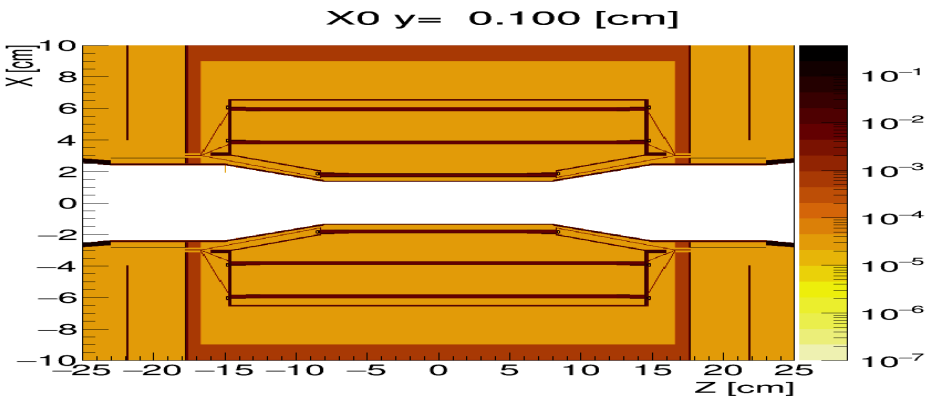
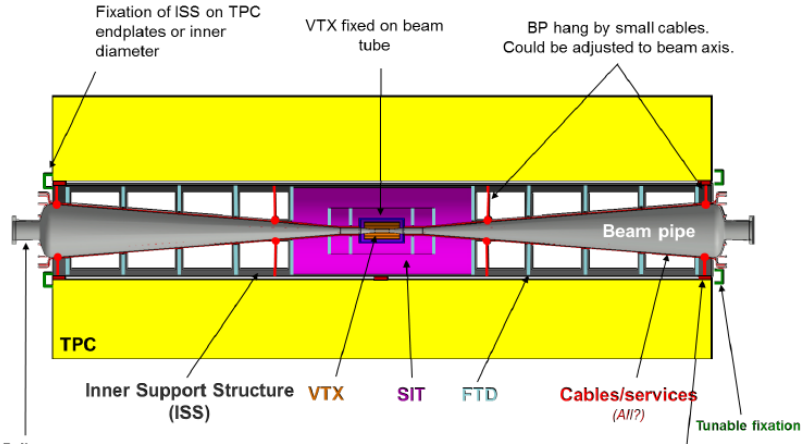
Status report on the vertex detector

Akimasa Ishikawa, Marcel Vos, Auguste Besson

Focus on the CMOS technology

(SOI, FPCCD will be covered in a future talk)



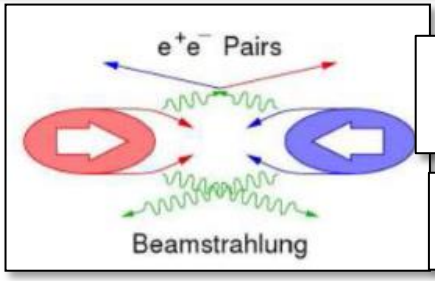


Homework from Mary-Cruz

- ✓ **Short description** of options being considered & *interplay with the rest (things that can affect full engineering but not the implementation itself)*
- ✓ **Status** of the work
- ✓ ***Software*** *related issues:*
  - *Needs of Monte-Carlo for detector optimization? Requirements of new software development or production on samples. Data Formats…*
- ✓ List of things pending to do ("urgent" & long term)
- ✓ Short/medium term plan
- ✓ **Future plan**
- ✓ Present **difficulties** (budget/manpower)
- ✓ Activities that, with the present and expected resources (assuming the present situation with the ILC) for which it will be needed to inject a significant amount of manpower or money
  - New groups could be very welcomed
- ✓ Ideas for exploiting more **synergies** with developments for other experiments and other R&D

Reminder: Impact of BS on technological choices

- Beam background dominates VXD occupancy (same for disks and SIT)
  - ✓ Governs the read-out architectures & technological choices
  - ✓ Percent level occupancy is considered as acceptable: ~few BX resolution time needed (0.5 – 4 µs)
- Constrains on technological choices
  - ✓ Presently 3 double sided layers in a CMOS tec. = baseline
  - ✓ FPCCDs presently do not cope with the hit rate (but have other advantages)
    - ~ 3 µm (CMOS) against 1 µm (FPCCD)
  - ✓ Does not exclude emerging technology (SOI, etc.)
- Trade-off needed to accommodate the hit rate, based on an interplay between pixel pitch, read-out speed and power consumption
  - ✓ achieving simultaneously the ambitioned spatial resolution & material budget is an issue
    - Targeted Mat.Budget ~0.15% X_0 / layer



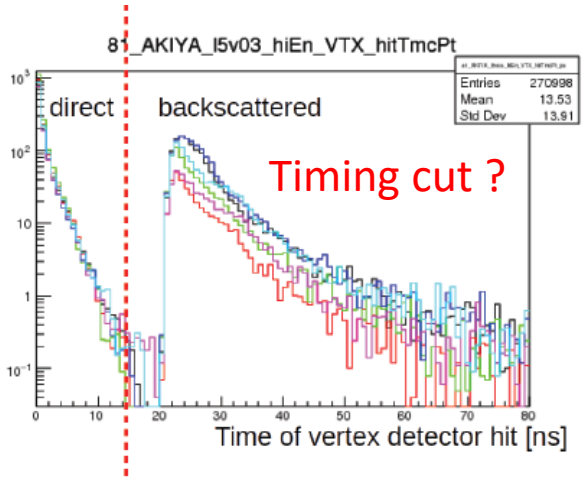
$$\sigma_b < 5 \oplus \frac{10}{p\beta \sin^{\frac{3}{2}}\theta}\ \mu m$$

Time resolution O(0.5-4 µs)

ILD @ 250 GeV

ILD_l5_v05	hits/BX			hits/BX/cm^2		
	mean	±	RMS	mean	±	RMS
VXD 1	914	±	364	6.64	±	2.65
VXD 2	545	±	207	3.96	±	1.51
VXD 3	129	±	60	0.213	±	0.100
VXD 4	107	±	53	0.177	±	0.088
VXD 5	40	±	26	0.043	±	0.029
VXD 6	34	±	24	0.037	±	0.026

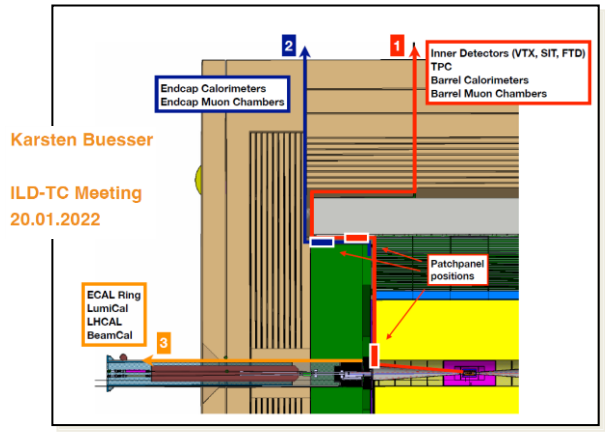
Daniel Jeans, Akiya Miyamoto

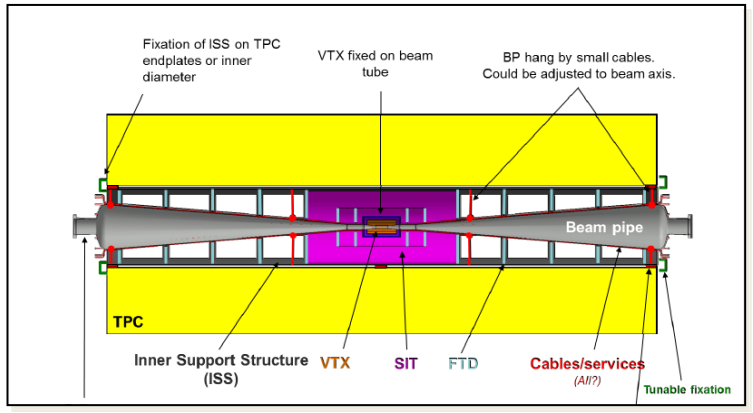


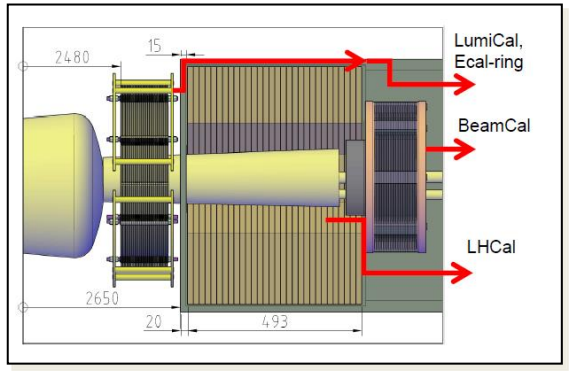
Cut at 15 ns

MDI-Phys - Beam pipe and vertex detectors

- **Meeting in December 2021**
  - ✓ https://agenda.linearcollider.org/event/9399/
  - ✓ Présentation by Henri Videaux
- Outcome
  - ✓ Strong interplay between
    - Beam pipe
    - Support
    - Services/cables
    - VXD/disks/SIT/lumical/beamcal
  - ✓ Updates needed on the forward region optimization ?
- Global strategy for everything:
  - ✓ Monitoring, cooling, cable routing, mechanics, data flow, etc.

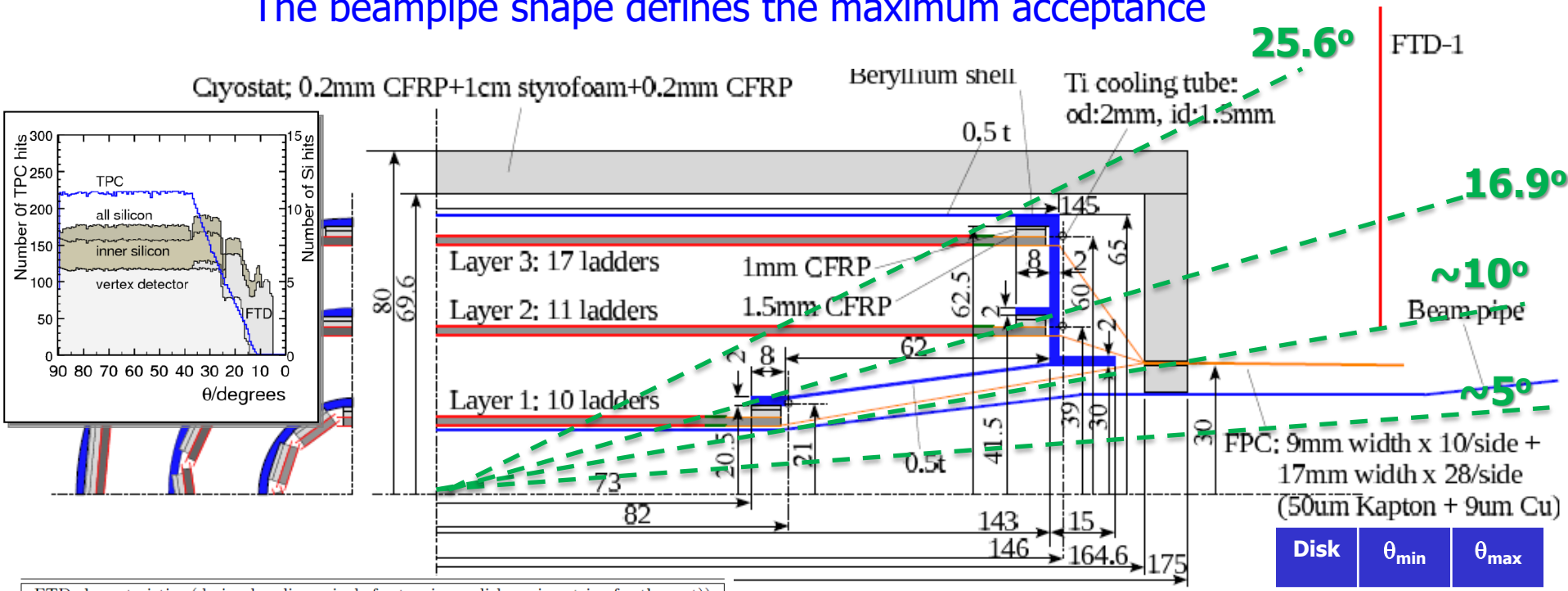




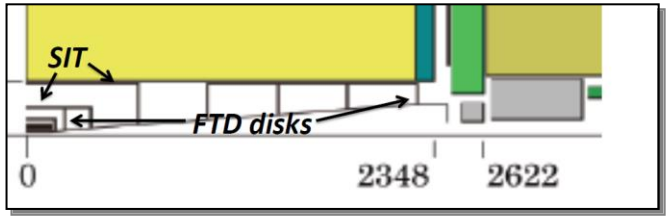


Geometry in the forward region (ILD)

The beampipe shape defines the maximum acceptance



FTD characteristics (design baseline: pixels for two inner disks, microstrips for the rest))				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
39-164	220	0.985-0.802		0.25-0.5
49.6-164	371.3	0.991-0.914	σ=3-6	0.25-0.5
70.1-308	644.9	0.994-0.902		0.65
100.3-309	1046.1	0.994-0.959		0.65
130.4-309	1447.3	0.995-0.998	σ=7.0	0.65
160.5-309	1848.5	0.996-0.986		0.65
190.5-309	2250	0.996-0.990		0.65



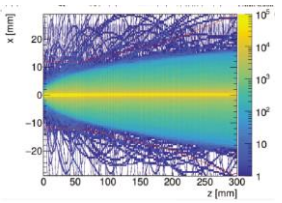
Disk	θ_{min}	θ_{max}
1	10.1°	36.7°
2	7.6°	23.8°
3	6.2°	25.5°
4	5.5°	16.5°
5	5.1°	12.1°
6	5.0°	9.5°
7	4.8°	7.8°

Figures per layers						
Layer	0	1	2	3	4	5
Layer Radius (mm)	16	18	37	39	58	60
Layer $\lvert z\rvert max$ (mm)	61.9	61.9	123.8	123.8	123.8	123.8

Polar θ (°)	>25.5	25.5-17	17-10	10-5
VXD hits	6	4	0	0
FTD hits (disks)	0	2-3 (1-2-3)	4 (1-2-3-4)	4-6 (2 to 7)

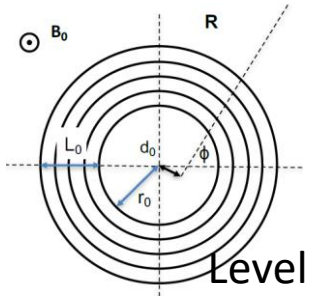
Background updates ?

- **Relevant sources of beam related backgrounds:**
  - ✓ news on beamstrahlung since TDR ? (D.Jeans/A.Miyamoto studies)
  - ✓ other phenomena: synchrotron radiation, infra-red radiation, ...
  - ✓ are there potential transitory backgrounds ?
  - ✓ consequences of potential luminosity upgrade (change in optics ?)

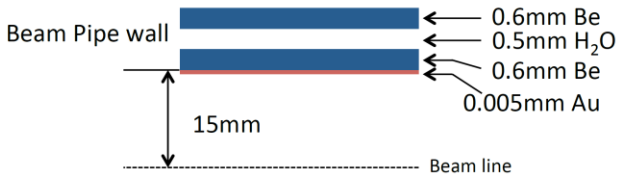


- **Which are the suspected sources of uncertainty** on the prediction of beam related backgrounds:
  - ✓ beamstrahlung generators: γ & $e^{\pm}$ rates, momentum spectrum
  - ✓ other phenomena: synchrotron radiation, infra-red radiation, ...
  - ✓ **corresponding safety factors ? x3-5 ?**
- **Beam parametres:**
  - ✓ beamstrahlung envelope at small polar angle prevents reconstruction of shallow tracks close to IP
  - ✓ at SuperKEKb (and FCCee < Sync. radiation) beam pipe cooling is considered as mandatory: Why not at ILC ?
    - Cooling ⇨ beam pipe material budget x 2 (~0.15%X_0 ⇨ 0.3%X_0)
  - ✓ At FCCee they consider reducing the inner radius (more material budget, lower magnetic field w.r.t. ILC)
    - Is it worth considering it ?

$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}}\sqrt{1+\frac{8r_0}{L_0}+\frac{28r_0^2}{L_0^2}+\frac{40r_0^3}{L_0^3}+\frac{20r_0^4}{L_0^4}}$$

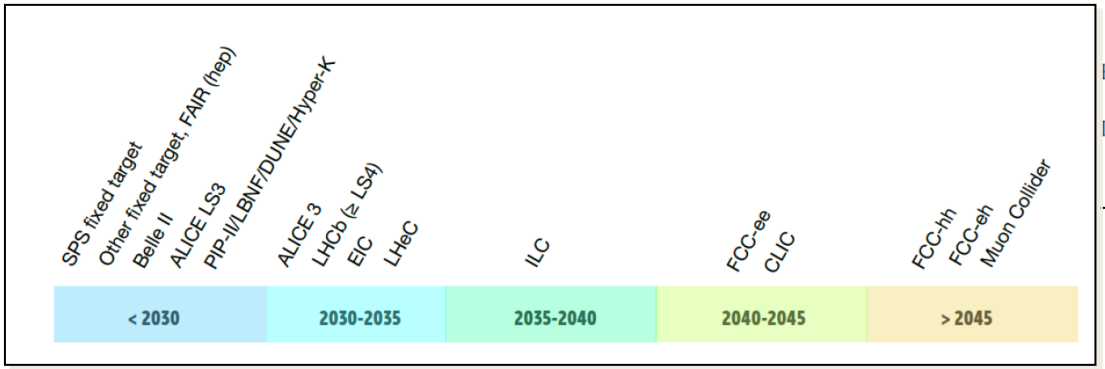


Level arm !



FCCee beampipe

Detector R&D Roadmap: themes (DRDTs)



References: ECFA/RC/21/510
CERN-ESU-017
DOI: 10.17181/CERN.XDPL.W2EX

< 2030 | 2030-2035 | 2035-2040 | 2040-2045 | > 2045

Solid state

- **DRDT 3.1** Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors
- **DRDT 3.2** Develop solid state sensors with 4D-capabilities for tracking and calorimetry
- **DRDT 3.3** Extend capabilities of solid state sensors to operate at extreme fluences
- **DRDT 3.4** Develop full 3D-interconnection technologies for solid state devices in particle physics

DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.

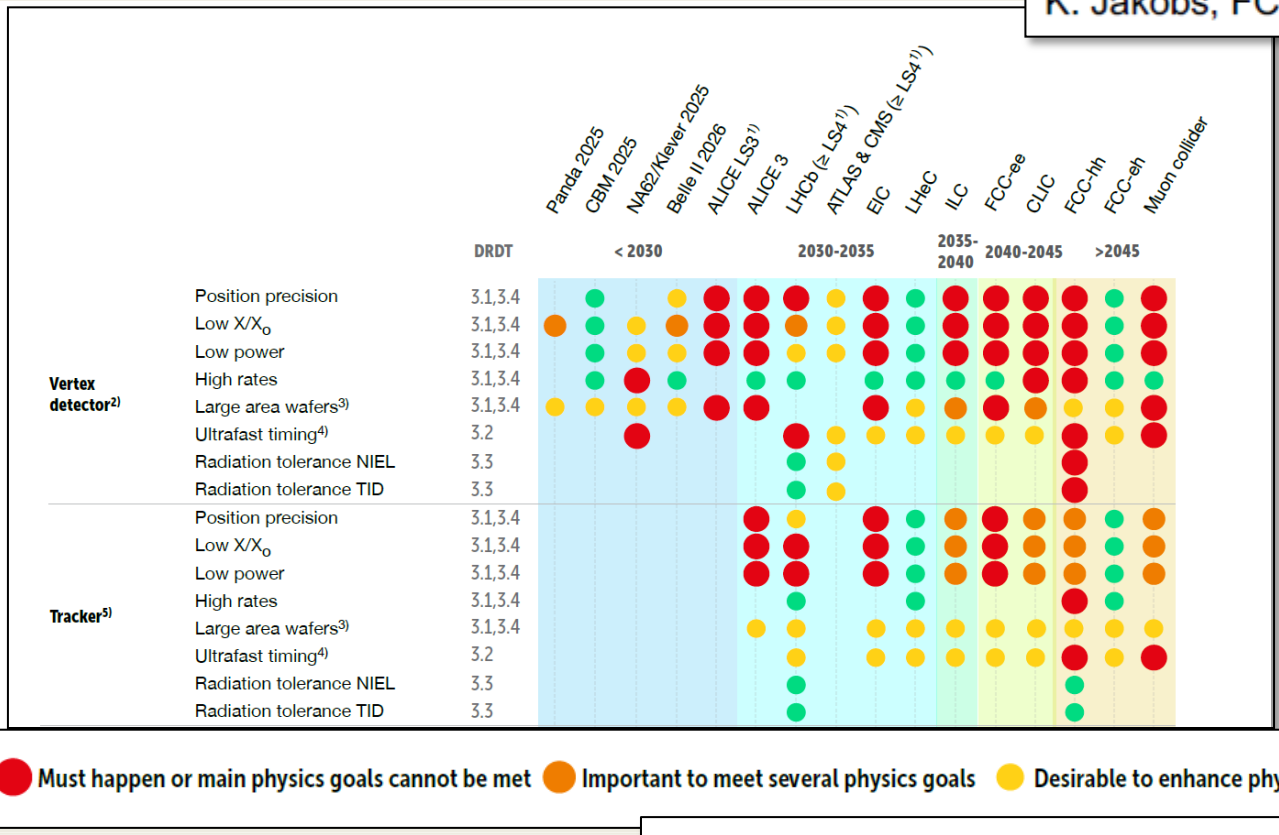
Developments of Monolithic Active Pixel Sensors (MAPS) should achieve very high spatial resolution and very low mass aiming to also perform in high fluence environments. To achieve low mass in vertex and tracking detectors, thin and large area sensors will be crucial. For tracking and calorimetry applications MAPS arrays of very large areas, but reduced granularity are required for which cost and power aspects are critical R&D drivers. Passive CMOS designs are to be explored, as a complement to standard sensors fabricated in dedicated clean room facilities, towards hybrid detector modules where the sensors is bonded to an independent ASIC circuit. Passive CMOS sensors are good candidates for calorimetry applications where position precision and lightness are not major constraints (see Chapter 6). State-of-the-art commercial CMOS imaging sensor (CIS) technology should be explored for suitability in tracking and vertex detectors.

Synergies

ECFA recognizes the need for the experimental and theoretical communities involved in physics studies, experiment designs and detector technologies at future Higgs factories to gather. ***ECFA supports a series of workshops*** *with the aim to* ***share challenges and expertise, to explore synergies in their efforts*** *and to respond coherently to this priority in the European Strategy for Particle Physics (ESPP).*

Goal: bring the entire e^+e^- Higgs factory effort together, foster cooperation across various projects; collaborative research programmes are to emerge

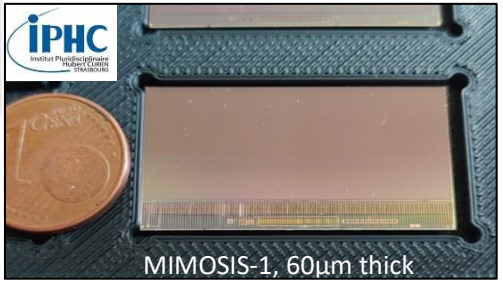
K. Jakobs, FCC Physics Workshop, Feb 2022

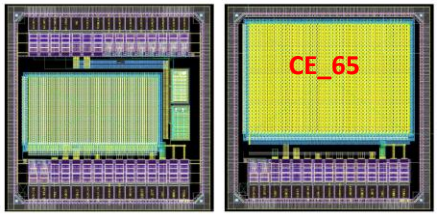


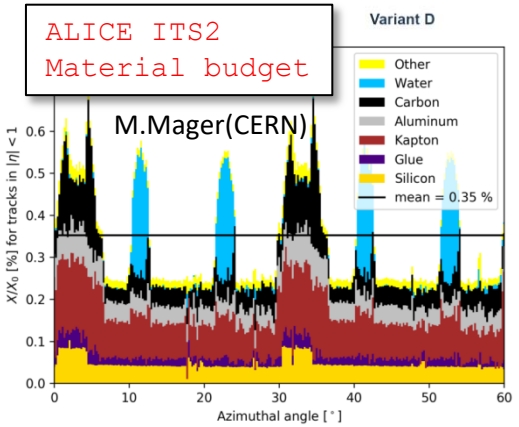
+ integration know-how (e.g. ALICE, Belle-2)

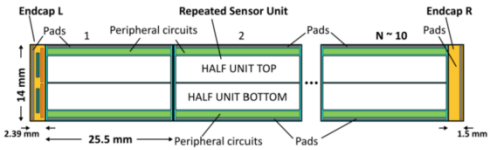
CMOS R&D status: present plans

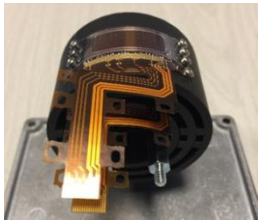
- Main R&D lines:
  - ✓ 180 nm technology: **MIMOSIS chips** for CBM-MVD @ FAIR
    - = a milestone for Higgs factories **(5µm spatial res./ ≤5µs time res./ 60µm thickness)**
    - MIMOSIS-1 (1st full scale prototype) under tests (promising preliminary results).
    - 3 test beam campaigns performed in 2021
    - Results match expectation
  - ✓ **65 nm tech. Exploration**
    - Main driver: CERN EP R&D WP 1.2 & ALICE ITS-3 upgrades (IPHC involved) ⇨ LS3 ~ 2024-26
    - Priority: Validate the technology then optimize time resolution & granularity
    - Test beam being analyzed (CE_65 prototype)
    - 65 nm detects charged particles !
  - ✓ **Stitching** & large surfaces for very low mass detectors
    - Priority for Higgs factories in the future ⇨ Material budget & Large pixelated surfaces
    - Reassess double sided approach ?
    - Next submission in 65 nm technology (eng.run 1) with CERN in Q1 2021: prototypes to explore stitching (MOSS/MOST)
  - ✓ Bent sensors (with ALPIDE – ALICE ITS-3)
    - Cf. M. Mager Seminar: *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS sensors*
    - https://indico.cern.ch/event/1071914/











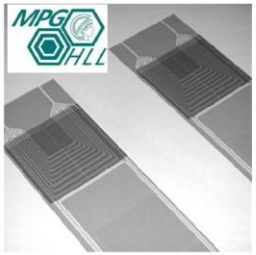
Integration

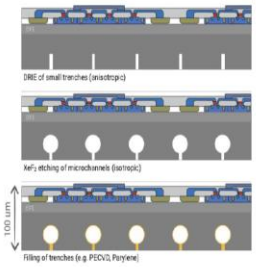
WP10 - CSIC report

Carlos Marinas, Marcel Vos (IFIC – UVEG/CSIC – Valencia),
Miguel Ullan (CNM-IMB Barcelona)

- Cooling, MCC, thinning

- 2016: Developed process to integrate micro-channels in DEPFET Silicon sensor (with MPG-HLL, JINST11(2016) 06)

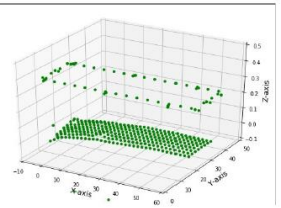




M. Boscardin et al., NIM A, 2013
C. Lipp, MSc Thesis, EPFL, 2017
I. Berdalovic et al., JINST 13 C01023, 2018

2019: Buried micro-channels in working MALTA CMOS sensor (CERN, EPFL)

Thinned multi-chip CMOS sensor, I. Peric (KIT) & IZM



Thinned Ladder (units in mm)		
Frame	Thickness	0.428 ± 0.008
	Planarity	0.01647
Center	Thickness	0.09 ± 0.04
	Planarity	0.0176

Mechanical characterization of thin sensors, planarity/thickness (grains & deformation), dynamic response under air flow (vibrations)
C. Marinas, G. Vidal, A. Catalan, IFIC Valencia

Bonding progress

- Successful realization of microchannels in silicon wafers by dry etching of silicon wafers (DRIE process)
- Successful compatibilization with wafer bonding process to create integrated microchannels
- Optimizing different wafer bonding technologies
- Plan to develop integrated microchannels compatible with metal layers
  - Successful development of anodic eafer bonding process at reduced temperature (< 400 ºC)
- CMOS process compatibilization in the longer term

Aim: integrate micro-channels in “large” CMOS ladders for Belle 2 upgrade and Higgs factories (and wherever else they may be useful)

Develop (eutectic) low-temperature bonding at CNM compatible with CMOS post-processing (hiring one engineer with AIDA-innova funding)

IFIC to focus on design and characterization of prototypes (hiring a new student or engineer)

Small steps: mechanical prototypes & dummy CMOS wafers before we sacrifice actual sensors

Integration example: Belle-2 upgrade R&D

UNIVERSITÄT BONN

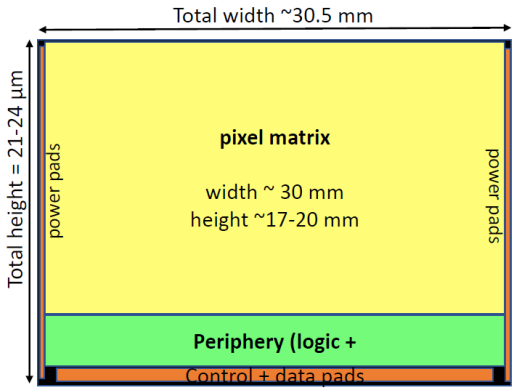
IVTX DEMONSTRATOR STATUS UPDATE

M. Vogt

OBELIX, Optimized BELle II CMOS pIXel sensors

	Belle-II VTX
Spatial res.	< 10 µm
Mat. budget	0.10 % X_0
Hit rate	<150 MHz/cm^2
Time stamp	<100 ns
Trigger (freq) (delay)	30 kHz 5-10 ns
Rad.hard. (TID) (fluence)	<1 MGy <10^{14} n_{eq}/cm^2

	OBELIX
Pitch	33 to 40 µm
Signal ToT	7 bits
Time stamp	7 bits
Integration time	25 To 100 ns
Bandwidth	< 1 Gbps
Power	< 200 mW/cm^2



jerome.baudot@iphc.cnrs.fr, hemperek@uni-bonn.de

Goals:

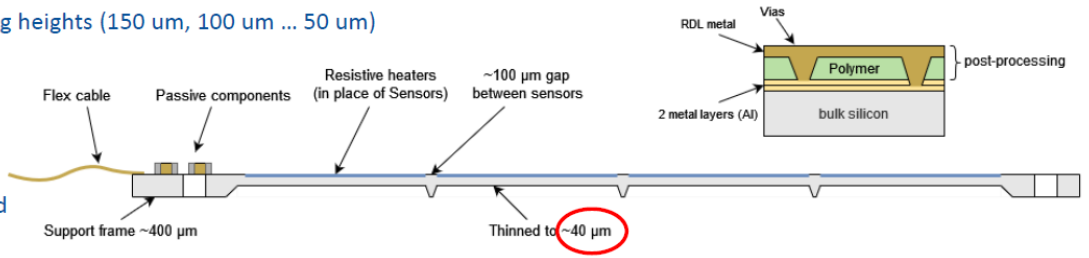
- process evaluation
- thermal studies, mechanical stability
- signal quality, power delivery, component assembly

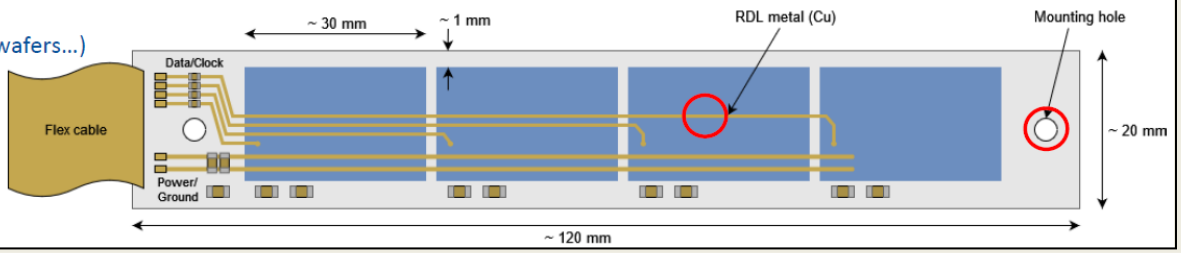
Plan: 2 runs

1. Proof of concept for the **RDL**, heaters etc.
   - Unthinned wafer
   - **Electrical studies**
2. Evaluation of the **thinning process**
   - Several wafers thinned to different decreasing heights (150 um, 100 um ... 50 um)
   - Same mask set as run 1
   - Thermal and mechanical studies

Potential issues raised by IZM

- **Mounting holes** → Gluing/clamping preferred
- **Thinning** the active area to 40 µm
  → ~20 µm process variation, homogeneity
  → Asked to think of alternatives (SOI, gluing wafers...)
- Length of RDL metal lines:
  Minimum width of ~20 µm can lead to interruptions along the module
  → wider traces





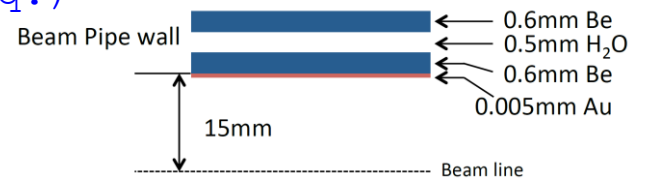
Software related issues(from a non-expert)

- Software tools are there
  - ✓ Lot of efforts made (training tutorial, fast-sim, etc.)
- What do we need ?
  - ✓ Compare performances for different technology/design choices
  - ✓ Different levels of figure of merits:
    - ⇨ Impact parameter resolution : not a challenge
    - ⇨ object performances (e.g. flavor-tagging performances, low pT tracking performances, etc.)
    - ⇨ impact on physics observable (e.g. H-cc coupling, etc.).
- What can be done
  - ✓ Some studies don't need heavy changes
    - Spatial resolution, time resolution, etc.
  - ✓ Some studies needs a different geometry
    - Material budget mapping, impact of geometry changes
    - Different tracking algorithms ? Different flavour tagging training ?
  - ✓ Main issue:
    - R&D people usually not heavily involved in software to implement reallistic alternative geometries

⇨ Experience in common activities with other Higgs factories

Being generic: ILC & FCC differences

- Beam structure: « continuous » vs trains
  - ✓ Power Pulsing: allows a factor O(10) reduction in average power
  - ✓ ILC: However, avoiding PP is desirable (alignment)
- Beam pipe shape and material
  - ✓ ILC: ~0.14% X_0 for the beam pipe (500 μm)
  - ✓ FCCee: Sync. Radiations ⇨ Cooling of the beam pipe ⇨ higher Mat.Budget
  - ⇨ 800 (2 pipes) + 400 (water) ~ 1200 um Be eq.)
  - ⇨ Smaller inner radius @ FCCee ?



- MDI:
  - ✓ CLD: Forward acceptance limited to 150 mradian (8.6°)
  - ✓ ILD: Froward acceptance (disks) ~ 5°
- TeraZ vs Giga Z
  - ✓ Specific timing and impact parameter resolution ?
    - e.g. lower radius ?
- Magnetic field:
  - ✓ ILC: 3.5/4 T (R_{max} ~1.8m)
  - ✓ CLIC: R_{max}(CLIC): 1.5m
  - ✓ FCC: 2 T max ⇨ compensate by larger level arm (R_{max} ~ 2.15m)

⇨ Overall most of the R&D can be fruitfully made common

Open issues and Pending activities

- Chip Designs
  - ✓ Full scale prototyping specifically optimized for a ILD vertex detector (or any Higgs factory) could only be triggered by political signs.
    - Rely on generic R&D for granular and thin sensors.
    - Rely on mid-term applications (CBM, ALICE upgrades, Belle-2, EIC, etc.)
- Simulations & Detector design
  - ✓ Technology breacktroughs could imply a complete reassessment of the design
  - ✓ No manpower in the Detector R&D community to perform dedicated simulation to optimize the VXD parameters w.r.t. physics analysis benchmarks
  - ✓ Global design not frozen (e.g. Faraday cage, anti-DID, forward region, etc.)
    - Room for dedicated optimization and open to other Higg factories.
- Integration
  - ✓ R&D groups mostly focused on chip designs.
  - ✓ **Many integration questions remains open**
    - Mechanics, cooling, Powering (& Power Pulsing), read-out, Alignement, EMC, Monitoring, connectors, cable routing, etc.
    - One should welcome new groups here.
    - Could benefit from mid-term experiments (ALICE upgrades, Belle-2, etc.)
      - e.g. ALPIDE Bent sensor studies @ CERN
- Synergies:
  - ✓ Turning the R&D more opened to other Higgs factories can be done naturally.
  - ✓ Encouraged by funding agencies
- The CMOS technology evolves quickly and this could impact the VXD design strategy
  - ✓ Stay open for new ideas