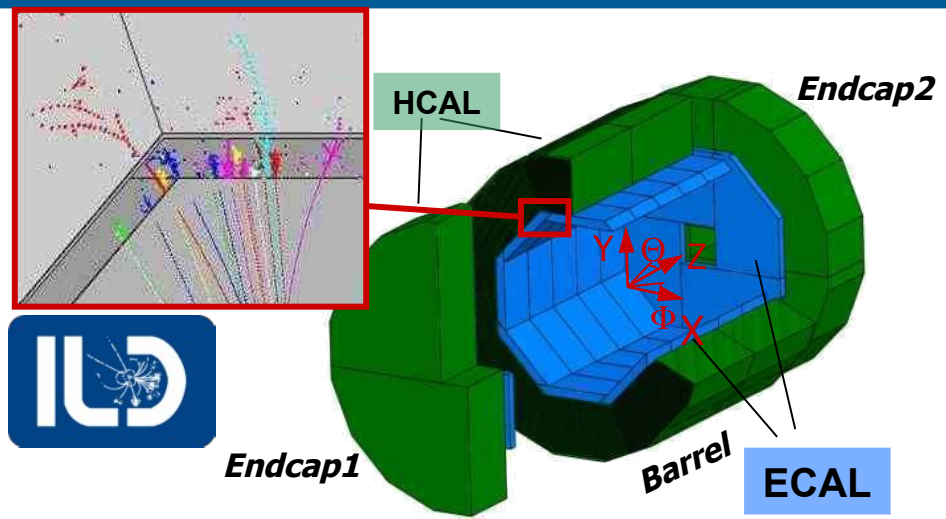
ILD Technical Convener Meeting

Vincent Boudry for the SiW-ECAL groups

Institut Polytechnique de Paris

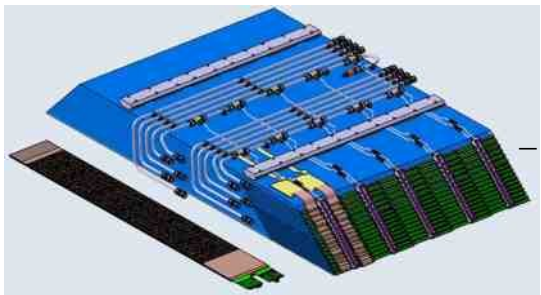
ILD Technical Convenor Meeting, 23/03/22

An Ultra-Granular SiW-ECAL for experiments



Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability (E, (θ,φ), t)
- PFlow requirements:
  - Extremely high granularity
  - Compacity (density)



SiW+CFRC baseline choice for future Lepton Colliders:

- Tungsten as absorber material
  - X_0 = 3.5 mm, R_M = 9 mm, λ_I = 96 mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design: Sensor+RO≤2mm
  - Allows for ~any pixelisation
  - Robust technology
  - Excellent signal/noise ratio: ≥10
  - Intrinsic stability (vs environment, aging)
  - Albeit expensive…
- Tungsten–Carbon alveolar structure
  - Minimal structural dead-spaces
  - Scalability

To be assessed by prototypes

Not included: general services

ILD Building blocks: SLAB's & ASU's

R&D for "mass production" and QA

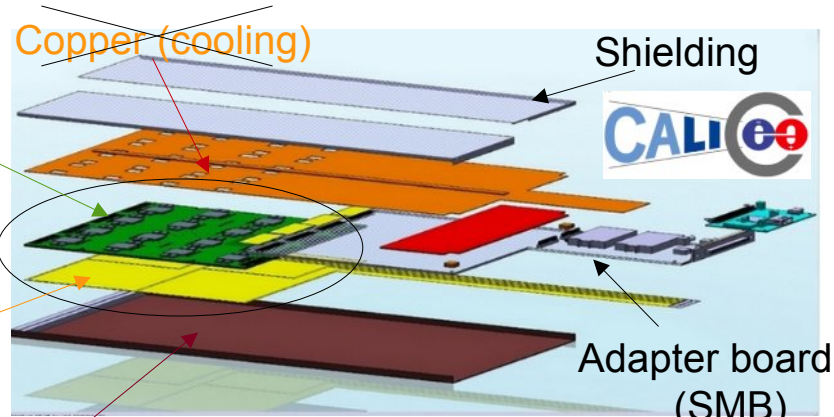
- Quality tests & preparation of large production
- Modularity → ASU & SLABs
- Choice of square wafers
  - (≠ from hex: SiD, CMS HGCAL)

Numbers (R_{ECAL} = 1,8 m, $|Z_{Endcaps}|$=2,35m)
(likely to be reduced by 30–40%)

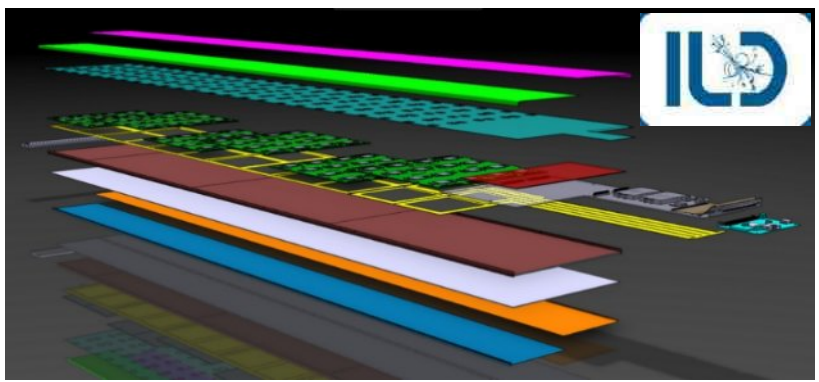
- Barrel modules: 40 (as of today all identical)
- Endcap Modules: 24 (3 types)
- ASUs = ~75,000
  - Wafers ~ 300,000 (2500 m²)
  - VFE chips ~ 1,200,000
  - Channels: 77Mch
- Slabs = 6000 (B) + 3600 (EC) = 9600
  - ≠ lengths and endings

Tests of producibility

Tests of feasability



U layout of a **short slab**

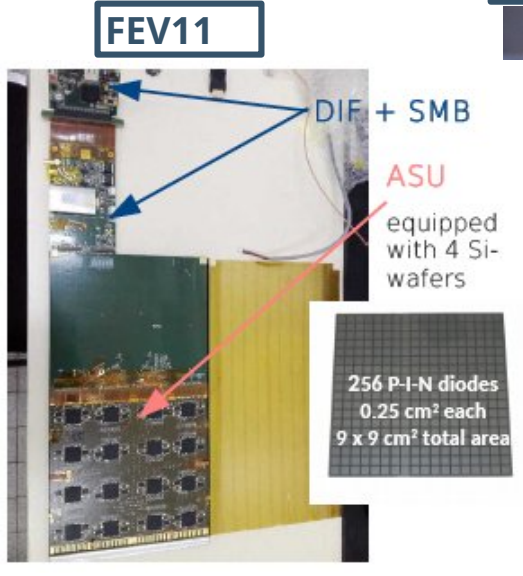


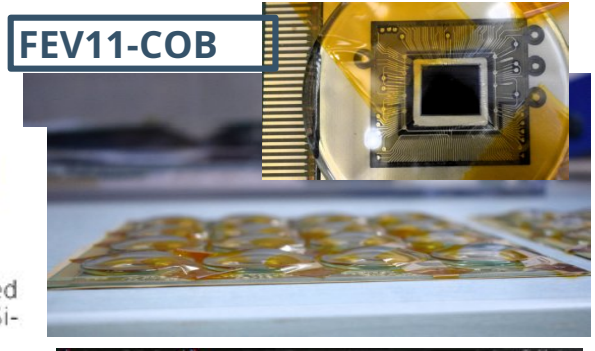
U layout of a **long slab**

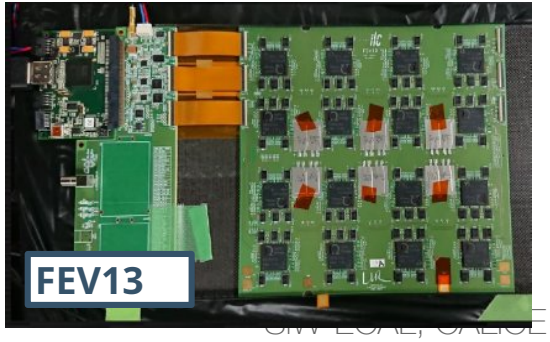
ASU R&D

Most complex element: electro-mechanical integration

- Distrib / Collect signals from VFE (ASICs), Analog & Digital
- Mechanical placer & holder for Wafers → precision
- Thickness constraints







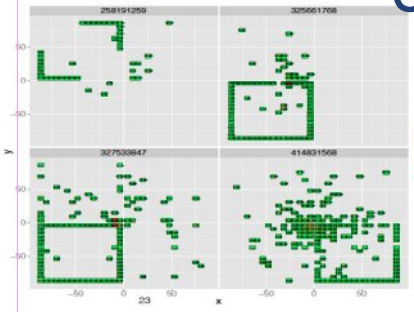
Milestone	Date	Object	Details	REM
1st ASIC proto	2007	SK1 on FEV4	36 ch, 5 SCA	proto, lim @ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st prototype of a PCB	2010	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	2012	FEV8	4 SK2 readout (256ch)	best S/N ~ 14 (HG), no PP retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, PP
1st full ASU	2015	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (High Gain) retrigger ~ 50%
1st SLABs	2016	FEV10 & 11	7 units	
pre-calo	2017	FEV10 & 11	7 units	S/N ~ 20 (12)$_{Trig,}$ 6–8 % masked
1st technological ECAL	2018	SLABvFEV10 & 11 & 13 SK2a+ COB + Compact stack	SK2 & SK2a (⊃timing)	Improved S/N Timing...

Calorimeter stack

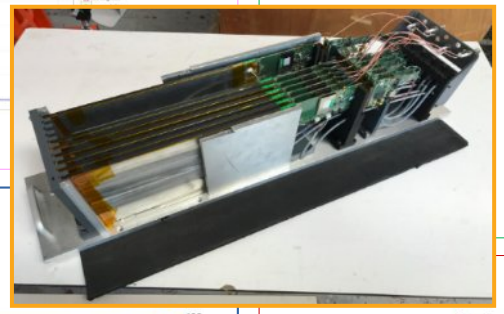
Beam-test 2015–2018

CERN 2015

"Naked FEV11"



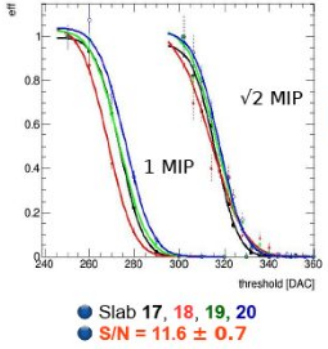
S/N_{ADC} = 16–17
(MIP – ped) / σ_{ped}
Defaults cataract :
- Negative signals
- re-triggers
- ~ high thr.
- sq events / 10

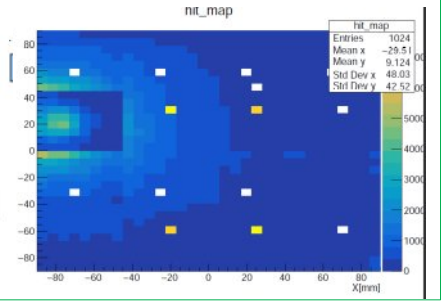


DESY 2018

7 FEV11 + 1 FEV13(650µm)

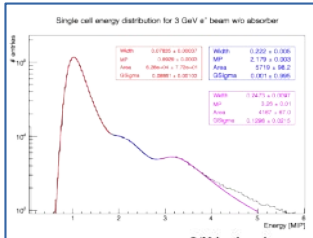
S/N_{Trig} ~ 11.6.±0.7
Trigger → ~1/3 mip (est.)
First comm. of FEV13

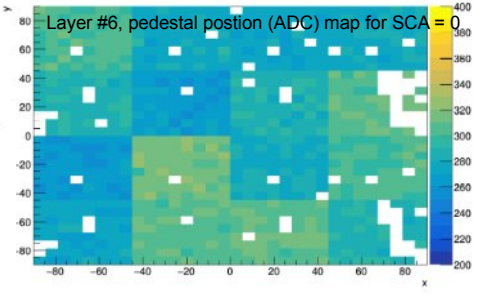


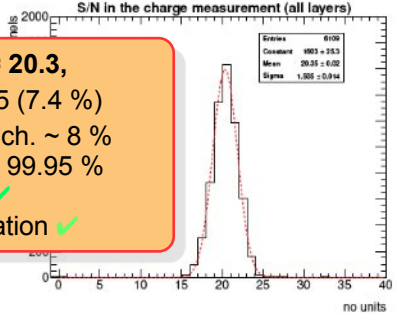


DESY 2017

7 FEV11





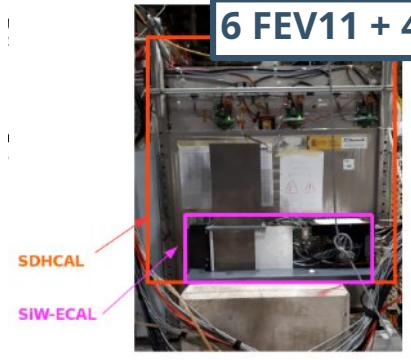


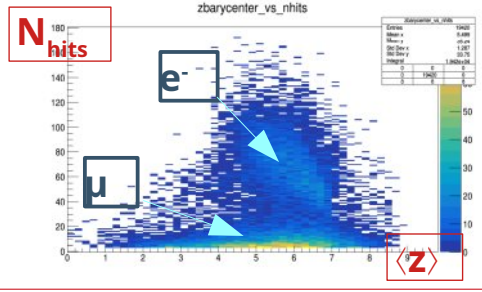
S/N_{ADC} = 20.3,
$\sigma_{S/N}$ = 1.5 (7.4 %)
masked ch. ~ 8 %
Hit eff. ~ 99.95 %
0°, 45° ✔
1T operation ✔

CERN 2018

Masked ch (FEV11) ~ 4 %

6 FEV11 + 4 FEV13(320 & 650µm) + 24X_0 W

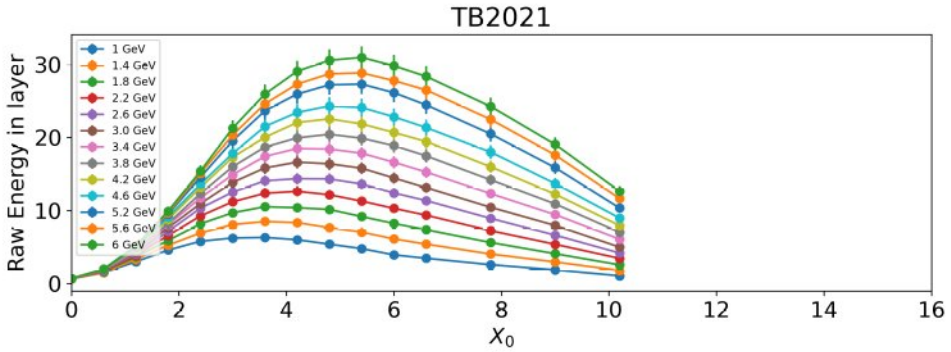


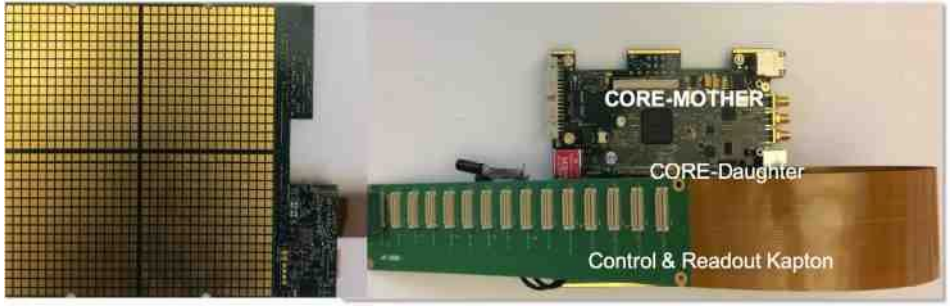


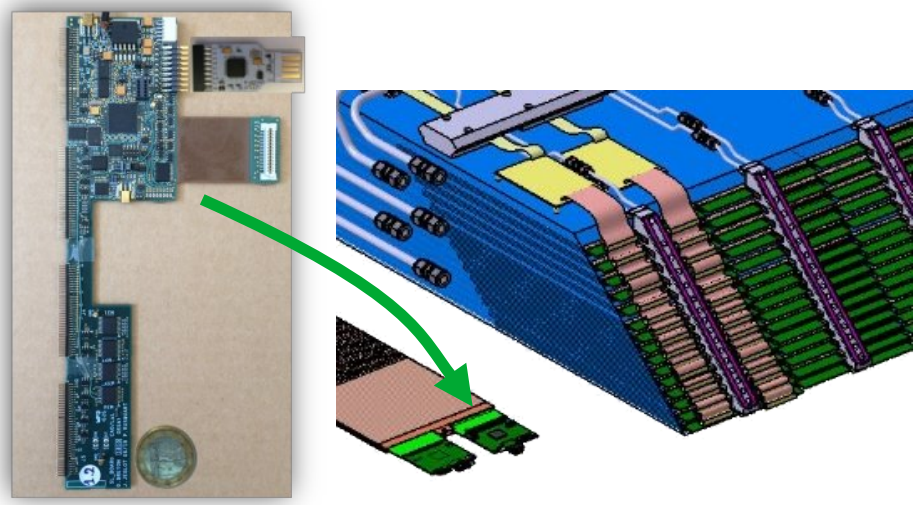
1st ‘full’ technological calorimeter

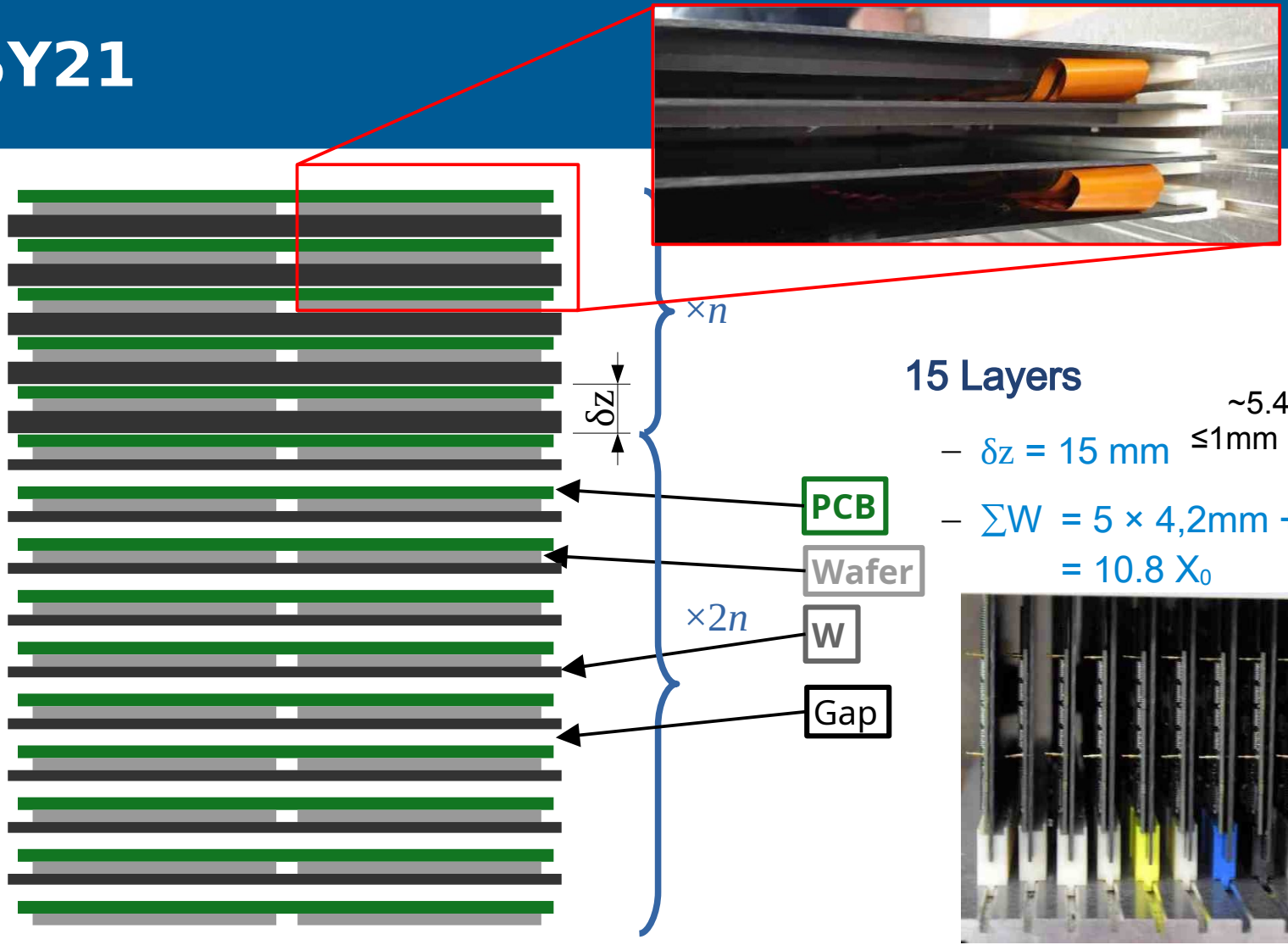
DESY Beam Tests

- November 2021 (due march 2020!), 2 wks
  - 1st 15-layers runs, 10.2 X_0
  - 4 types of Boards
  - Calibration (punch-though e-, showers)
  - low-E showers
    - Some defective layers (HV), low efficiency
- 1st use of new compatc DAQ “ILD-like”

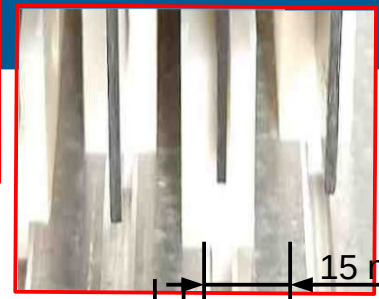








Gap ~ 1 mm ?



~5.4mm air gap from sim.
≤1mm due to SLboard pins, ...

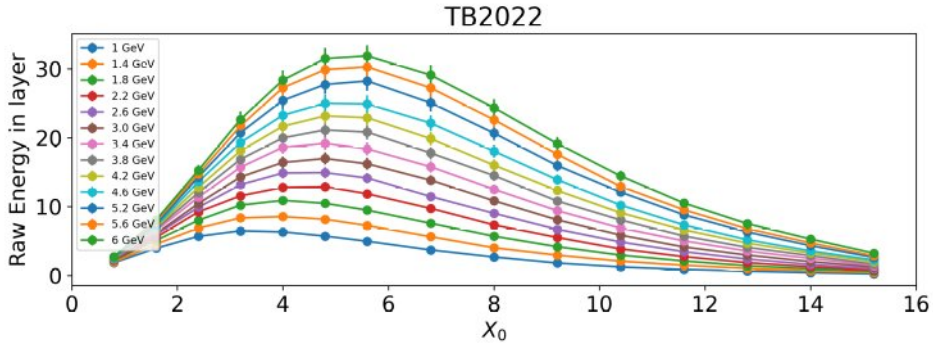
15 Layers

- δz = 15 mm
- $\sum W$ = 5 × 4,2mm + 9 × 2,1mm
  = 10.8 X_0

1st full calorimeters

DESY Beam Tests

- March 2022 (on-going), 1 wk
  - 2nd 15-layer run, compact DAQ
    - improved Monitoring (next slide)
  - 5 types of FEVs : FEV10–13 + COB
  - W: 7×2.8mm + 8×4.2mm = 15.2 X_0



TB 2022-03 (22/03/2022 22:00)

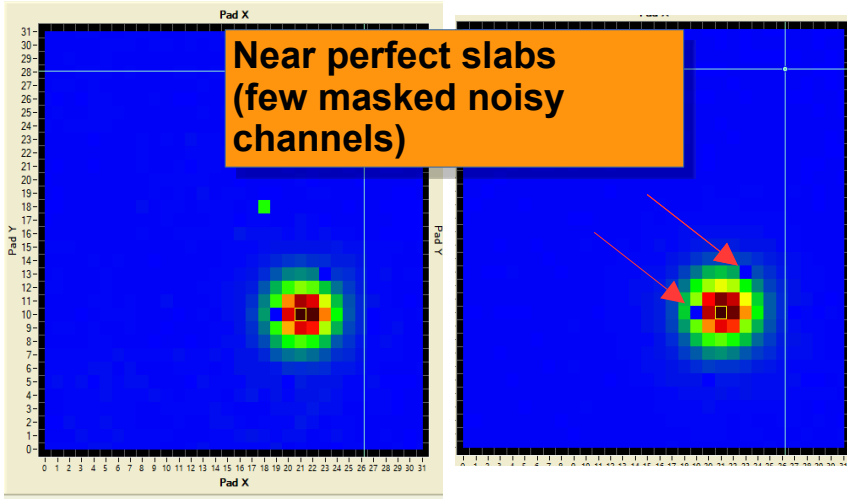
coreKapton slo	Layer position	SLAB	SLB- ID	SLB-Add	ASU type	wafer
14	0	34	15	0	FEV13	650
13	1	35	16	1	FEV13	650
12	2	33	20	2	COB	500
11	3	29	22	3	COB	500
10	4	19	13	4	FEV11	320
9	5	20	11	5	FEV11	320
8	6	21	14	6	FEV11	320
7	7	30	19	7	FEV12	500
6	8	31	17	8	FEV12	500
5	9	24	7	9	FEV12	500
4	10	25	3	10	FEV12	500
3	11	22	4	11	FEV11	320
2	12	18	2	12	FEV11	320
1	13	23	6	13	FEV10	320
0	14	17	10	14	FEV11	320

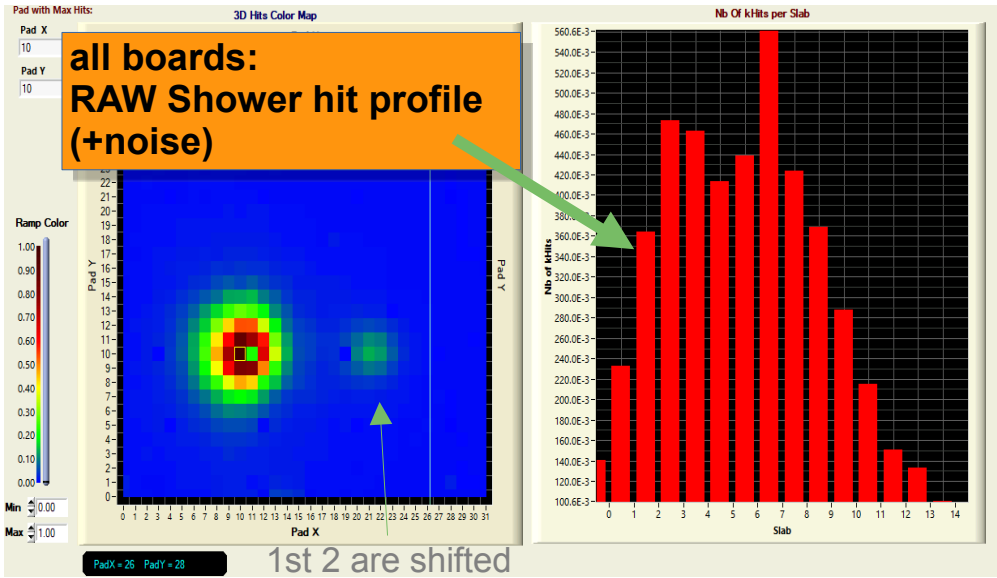
Main goal:

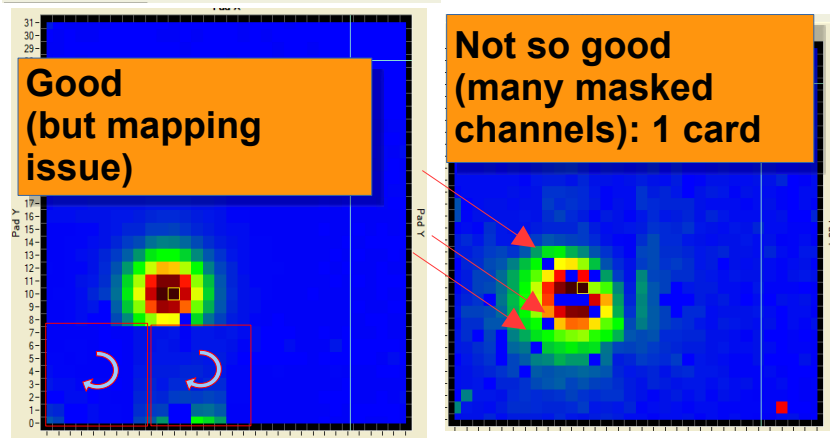
- Shower studies, lin(E), σ(E), σ(θ) @ 1–6 GeV
- To be complemented at CERN SPS 10–300 GeV (prelim June 22)

+ 1 week combined tech running with AHCAL

Online Hit Maps (≥~0.5 mips)



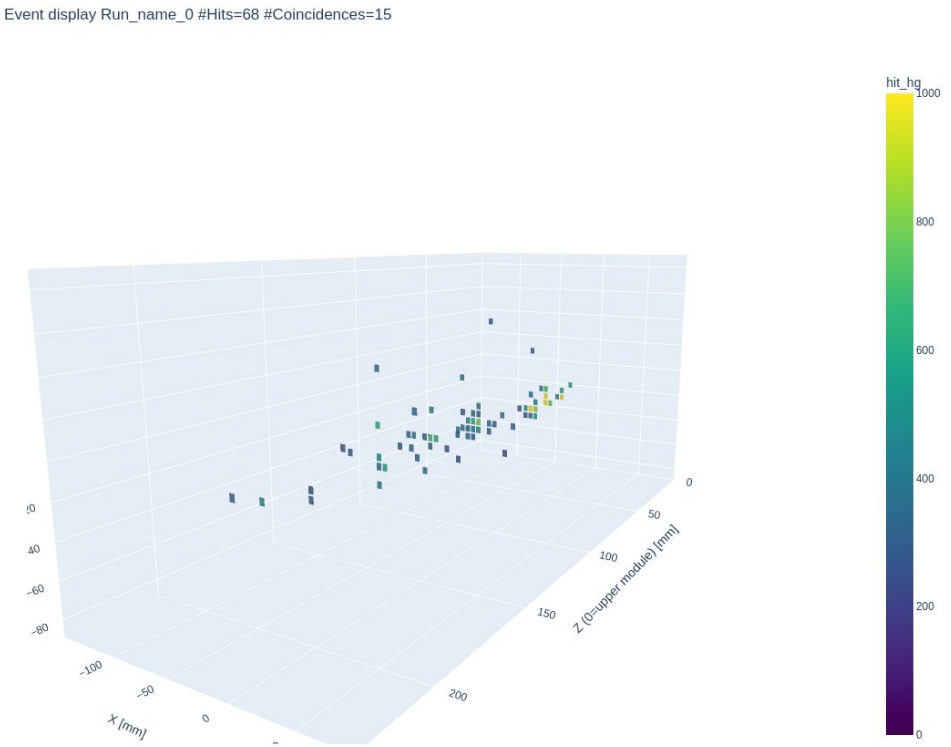


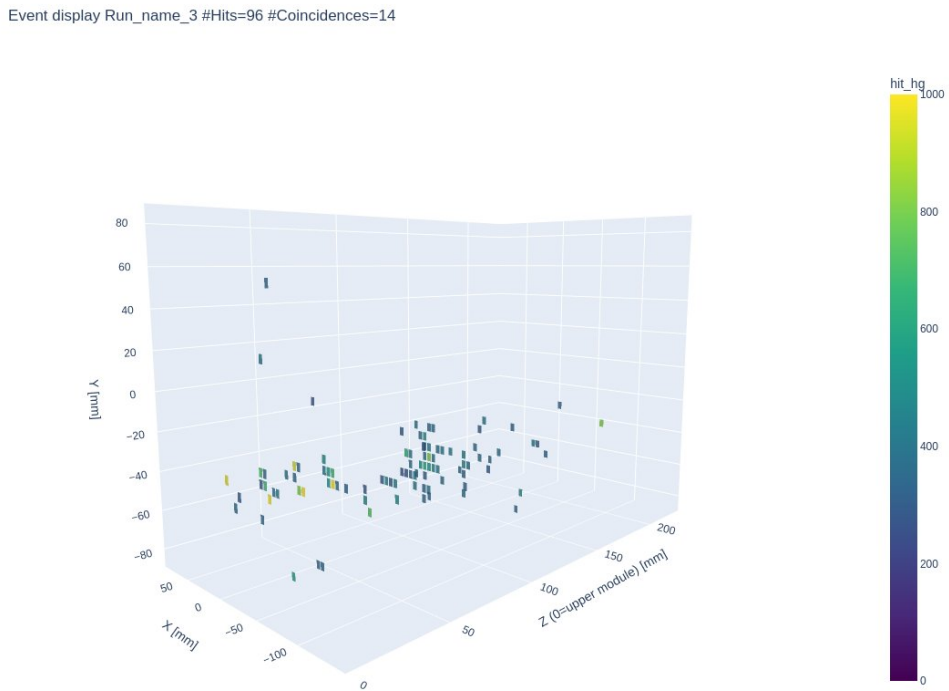


Almost all layers very good (despite some aging)

- installation in 1 day

Event displays



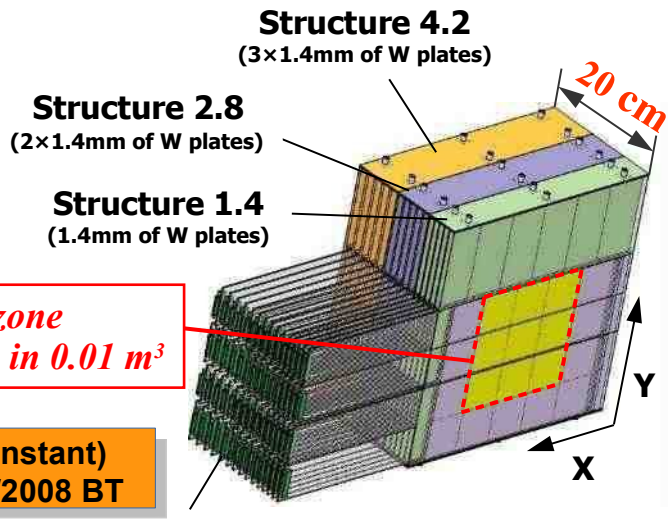


CALICE SiW ECAL: Physics & Technological prototypes

Physics prototype: 2005–2011

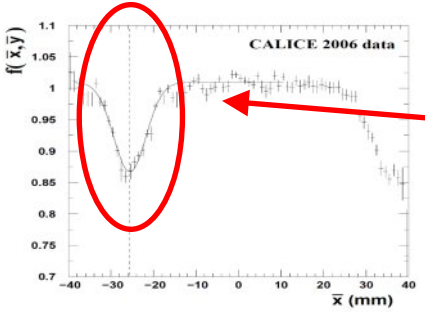
PFA proof of concept with comparison to MC
Electronics outside

- 1 × 1 cm² pixels

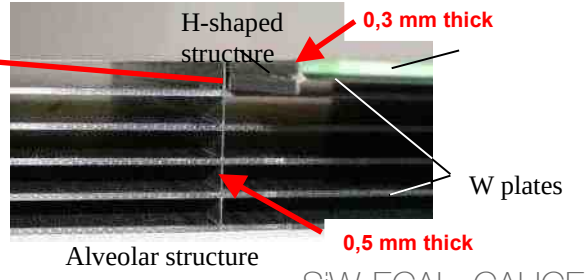


Active zone
~10000 pixels in 0.01 m³

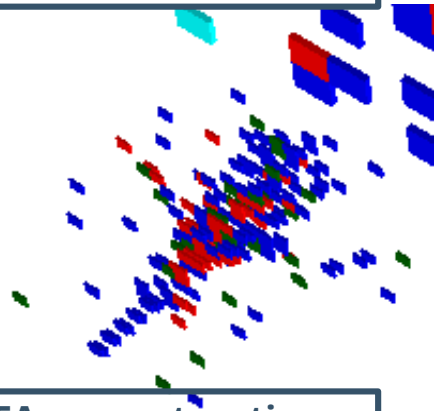
16.5%(stochastic) 1–2% (constant) with 1–45 GeV e⁻/e⁺ at 2006/2008 BT



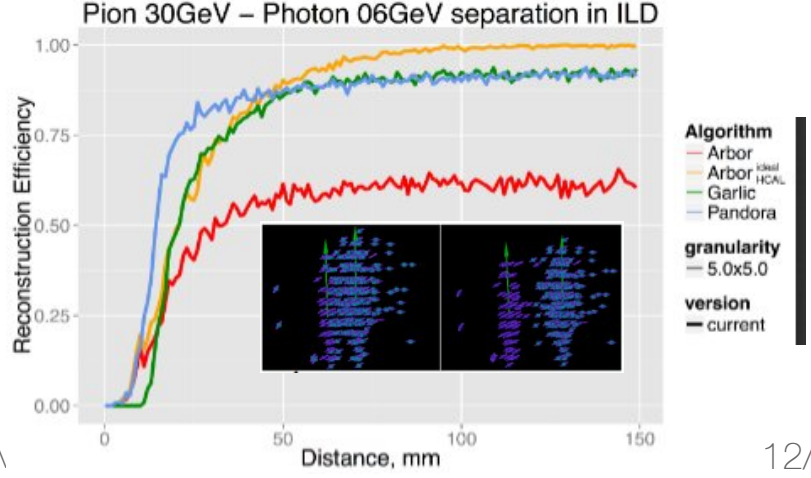
Detector slab (x30)



GEANT4



PFA reconstruction



‘Long Slab’

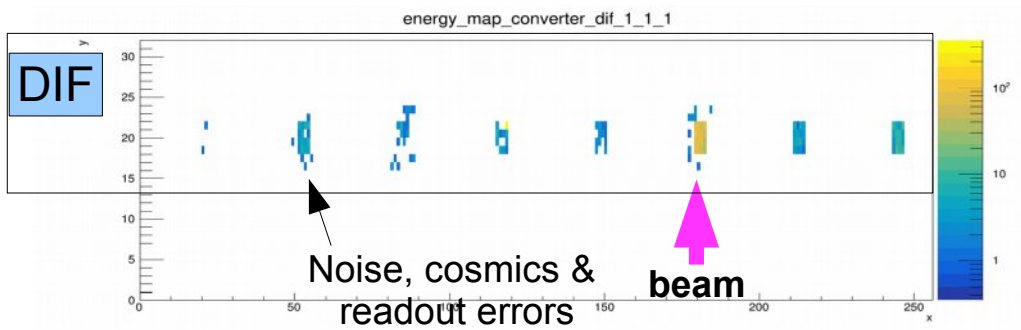
1st "electric long slab" (2018)

M. Anduze, F. Magniette,
J. Nanni, G. Fayolle

Support of interface boards + 12 ASUs (DBD)

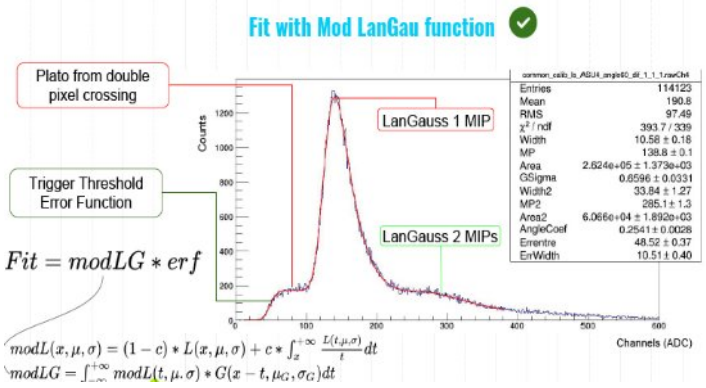
- 2+6+4 ASUs = ~3.2 m
- Rotatably along long axis (for beam test)

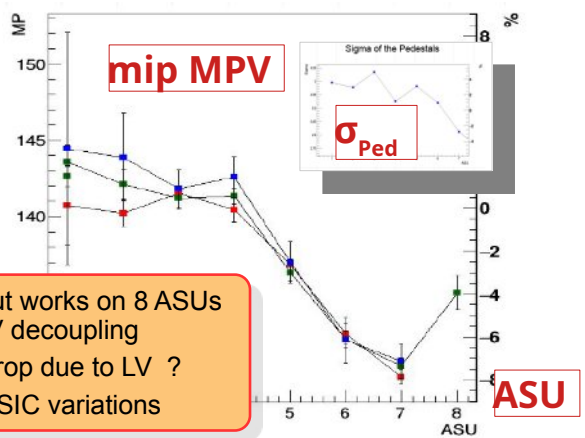
  Rigidity : ≤ ~1 mm per ASU
- Total access to upper and lower parts
  - 320µm Baby wafers (4×4 pixels) on the bottom



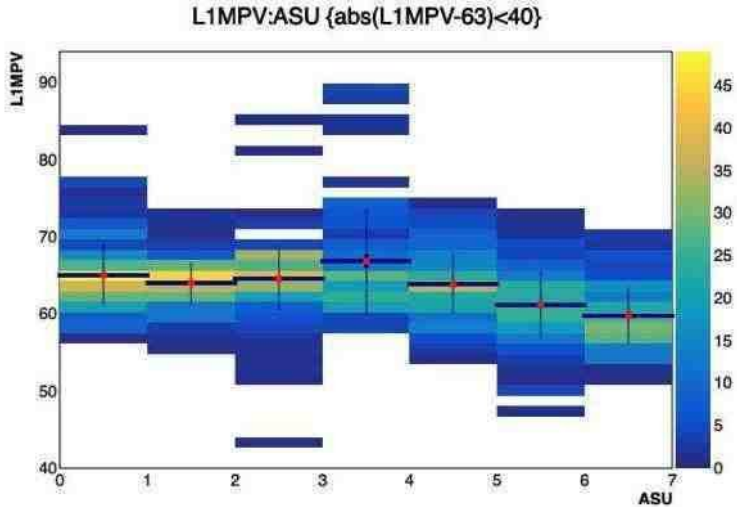
DESY-2018 beam test

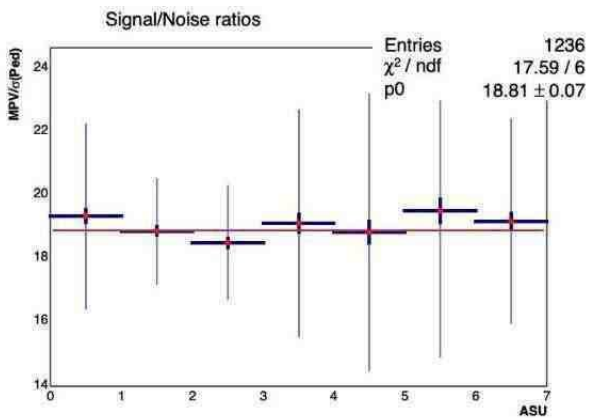
Mip response vs SLAB





- Readout works on 8 ASUs with HV decoupling
- 50 % drop due to LV ?
- 50 % ASIC variations





Electronics adjustments

Path length induced reflexions on clock line

- Fluctuation over logical level
- Extra clock tick → bad ASIC configuratior
- RC filter adaptation (Sigrity simulation)

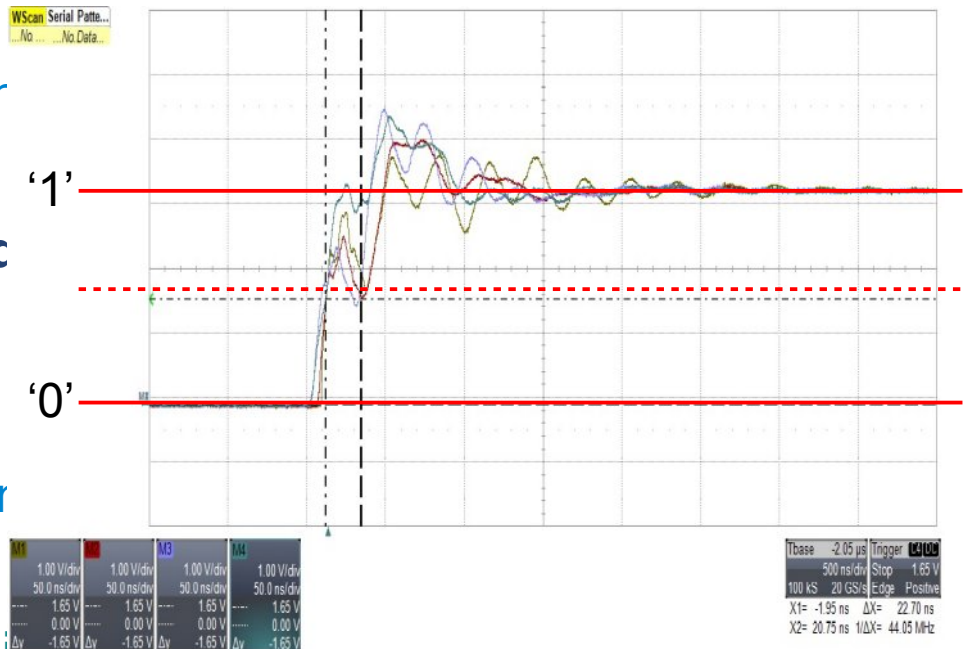
Impedance adaptation required depenc

- **Limited to 8 FEV12** + baby-wafers

Noise in the signal

- High frequency perturbation in the HV lir
- Solved by RC filters on the HV line
  - Possible back-propagation of ASICs noisy channel through HV ?

Also issues on the data routing...

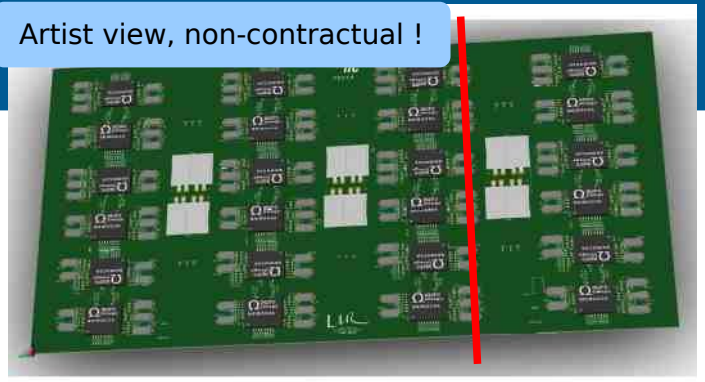


FEV2.0

FEV2.0

HPK « No 8'' wafer bef. end 2021 »

Artist view, non-contractual !



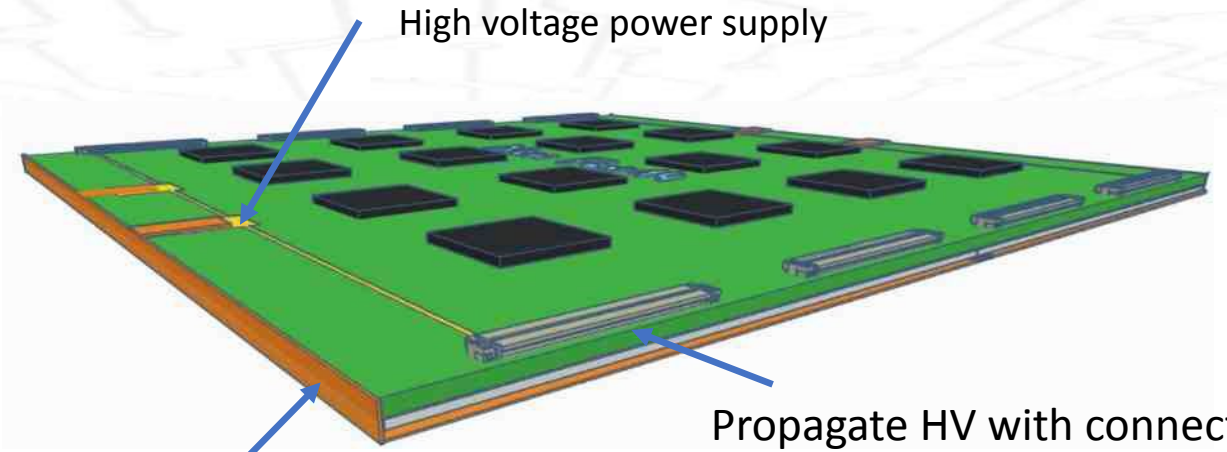
Requirements

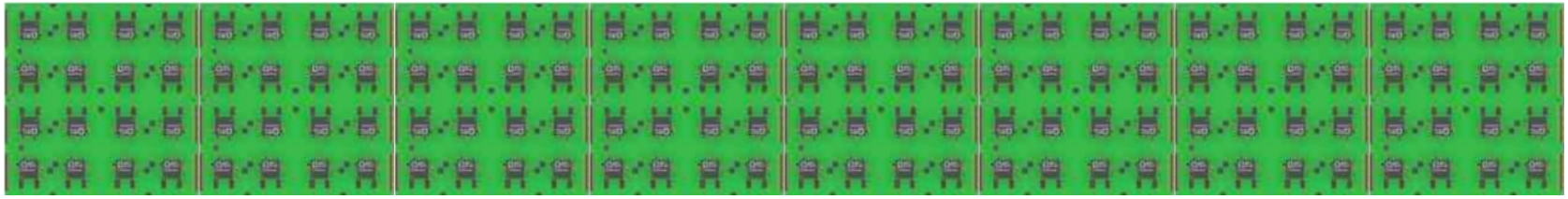
- Compatible ~~8''~~ et 6'' wafers ; Compatible with FEV1*
  - ~~6 Matrices 6'' OR 2 × 1,5 Matrices 8''~~
- ~~24 ASICs vs~~ 16 ASICs
- Improved mecanics, scalability & maintenance
  - Connectors
  - HV distribution & Filtering on PCB
  - 1 HV per card ⇒ independent test, exchangeability
- LV Regulation on board with LDO
  - Power-pulsing : DIF ➡ FEV, lower currents
- Corrected data & clock distributions
  - Must be OK for 2,1 m (EndCaps) = 8 FEV
  - Timing ≤ 0,1 ns ? → for SK3 ?
- Compatibility new DAQ
- Improved noise & decoupling

HV individuation → allow for operation in stack (single or double) and long slab

Mechanics

- Kapton is enlarged to protect sides during insertion or sliding in the support.
- High voltage is driven by the board instead of the kapton for assembly, maintenance and costs reductions.





Example of faulty board

To unplug: slice to the right

A Long Slab with FEV2

Adaptative design wrt FEV12

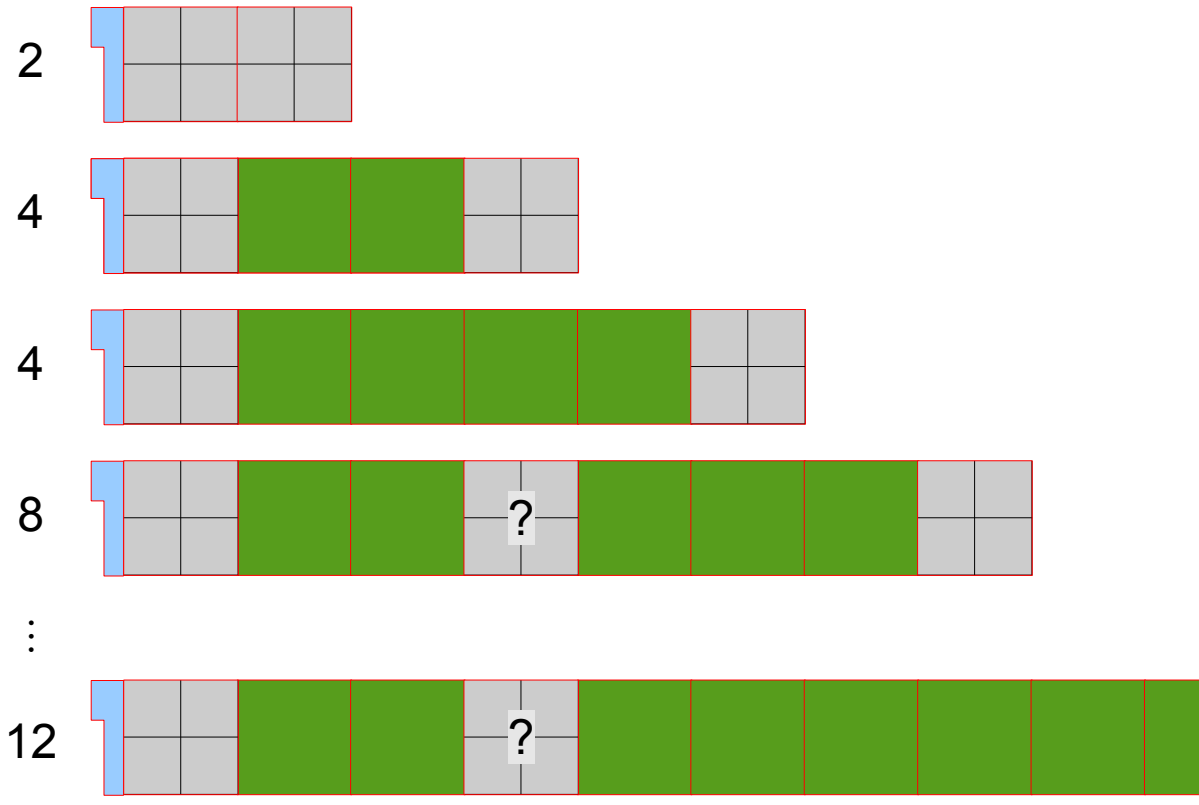
- Integration of new DAQ with Power Scheme
  - (see Jihane presentation)
- Possibility to include FEV13b-COBs in LS

Modular design :

- Incremental length

Full equipped ends of SLAB

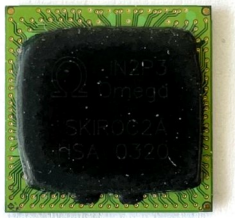
- 1st and Last ASU
- Regulators / Decoupling on each ASU
  - Shower response at end of SLAB
- Possible integration new ASU's in stack



New packaging for SKIROC2A ch

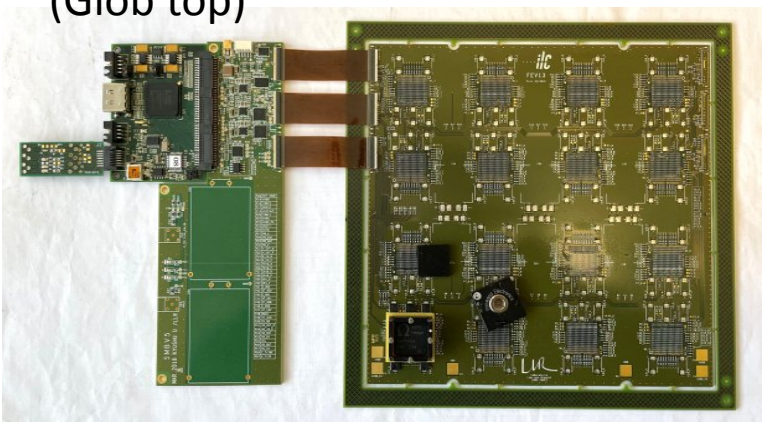
- “Historic” Novapack stopped BGA encapsulation activities (Apple’s fault ?)
- Replacement hard to find for small quantities
- Swiss-based Aptasic

  → No conclusive results
- Contact with a new Chinese company (recommend by Omega)
  - Package BGA size: 17mm × 17 mm
  - Thickness: 1.2mm



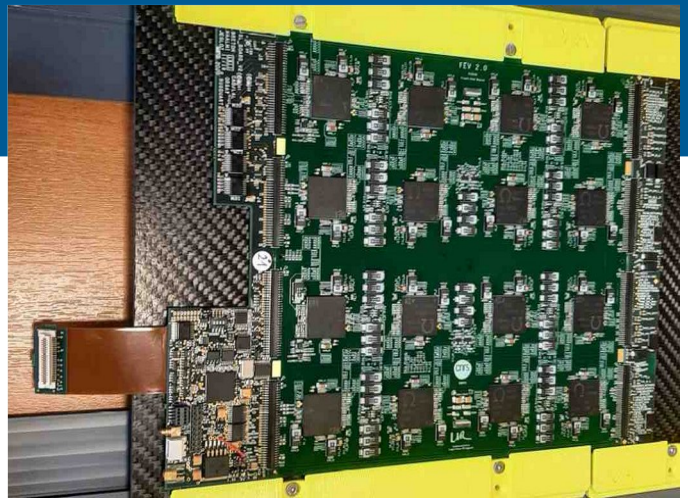
Aptasic solution
(Glob top)

Awaited solution



Upgrade bench of unique chip

FEV2.0



Design (fall 21) by LLR and IJCLab

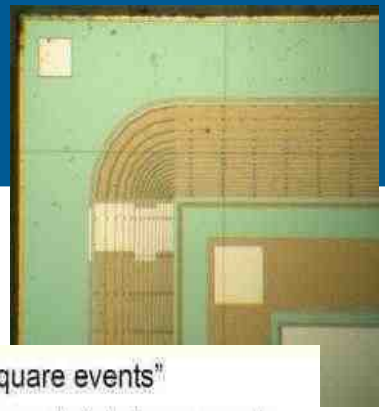
Pre-serie (Feb. 22)

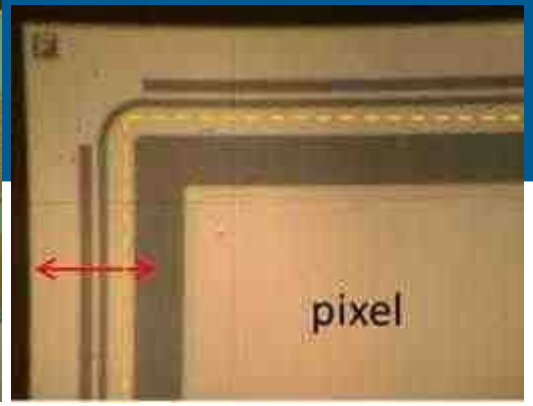
- 1 board soldered in IJCLab elec. workshop
  - Difficulties with heat inertia (mass planes w/o heat bridges) ➡ being corrected
- Very good “raw” noise results
  - Being investigated with unglued sensors

Fake-FEV

- electrical model (no ASICs, etc)
  - HV leakage current of 5 FEV ~ 1 sensor

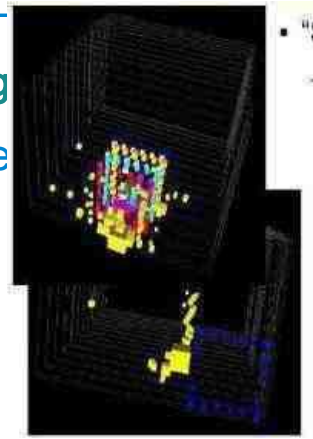
Silicon Sensors



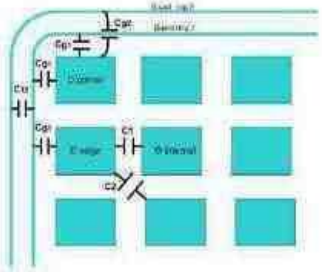


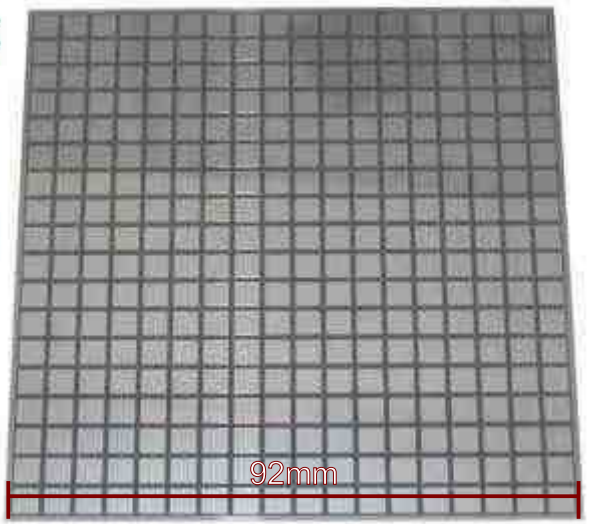
Cost driver

- ~30% of the total cost of the SiW-ECAL
  - ⇒ Units Cost reduction(**CALIIMAX prog**
- Decoupling of Guard Ring (Square Eve
- new design of ILD detector



- "Square events"
  - cross talk between guard rings and pixels

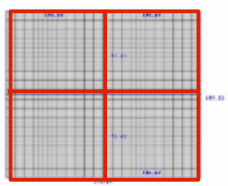


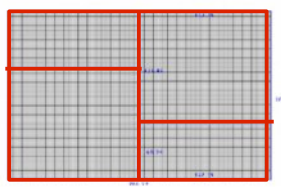


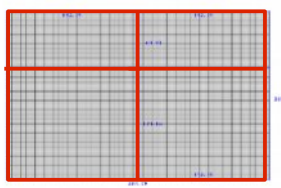
'quantum unit' of ILD dimensions (here 6" wafer)

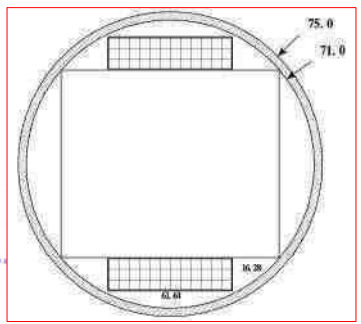
Command Sensors (@ Hamamatsu)

- ⚠ Minimal cost of Command ≥ 20k€
- direct contact with HPK engineers
- Possibility of design for 8" in 186mm alveola 320 →





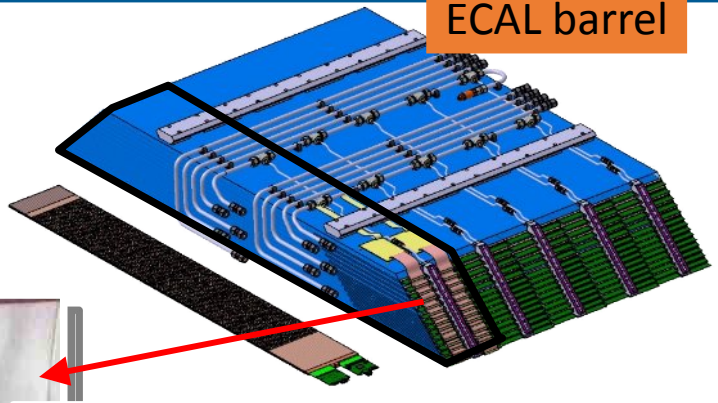


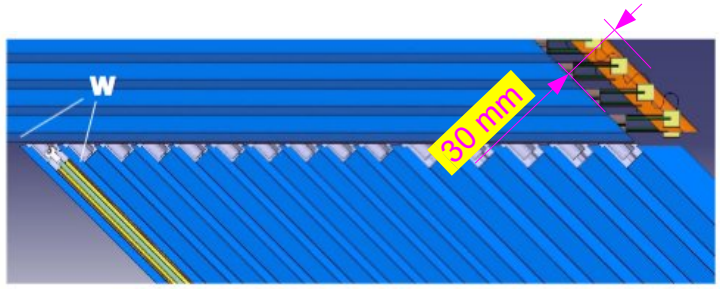


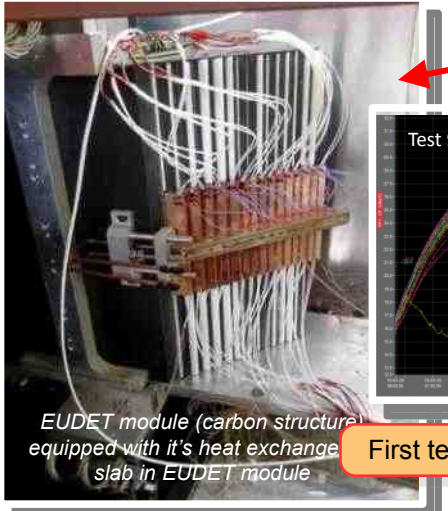
ECAL Services

Cooling

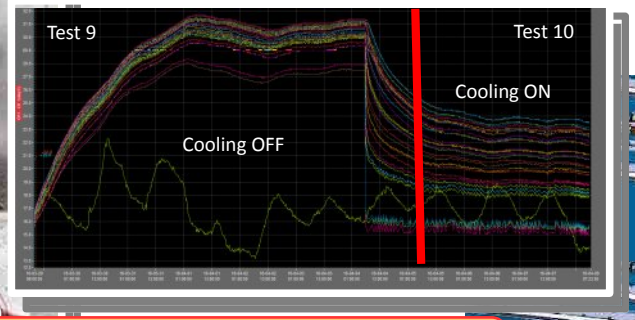
ECAL barrel





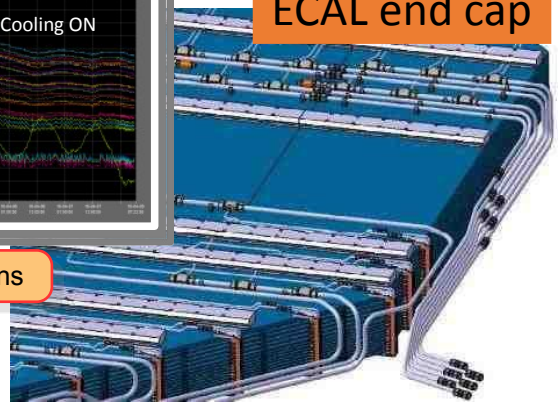


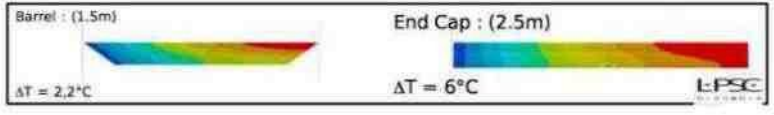
EUDET module (carbon structure) equipped with it's heat exchange slab in EUDET module



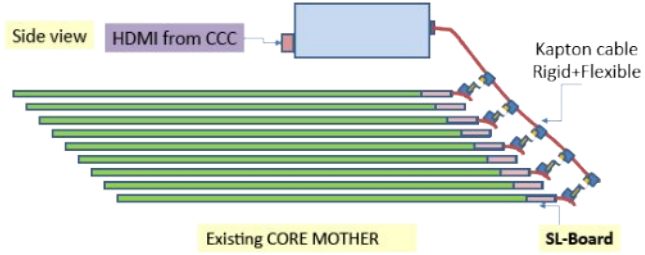
First tests results in line with simulations

ECAL end cap



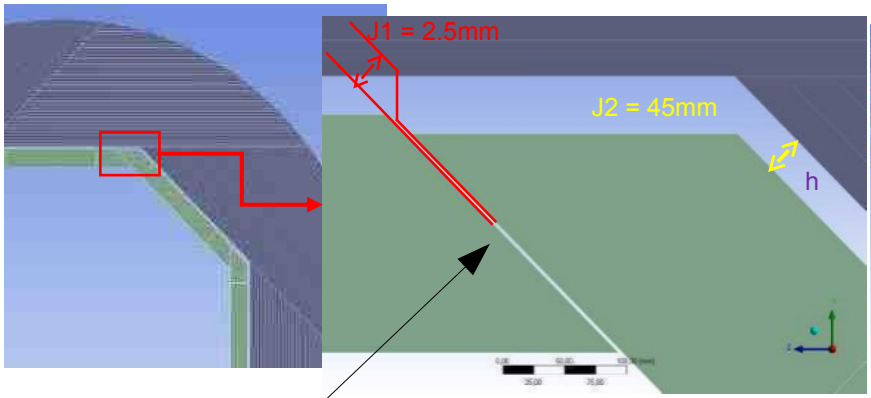


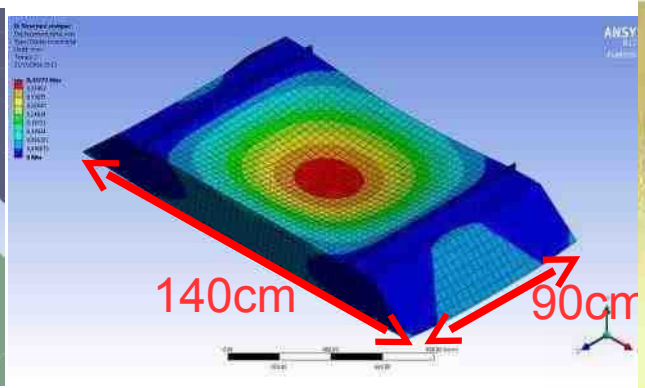
DAQ

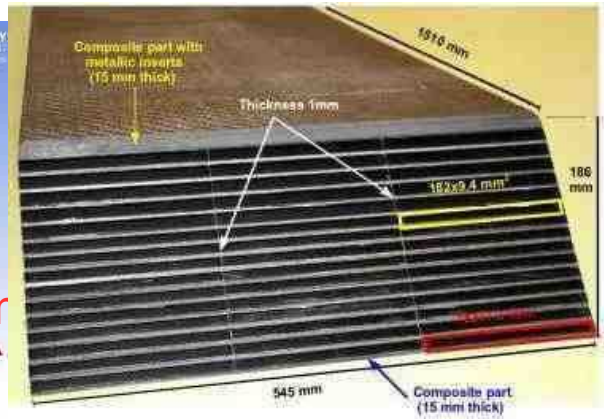


CFRC+W Structures

H. Videau, M. Anduze, T. Pierre-Émile, D. Grondin, J. Giraud



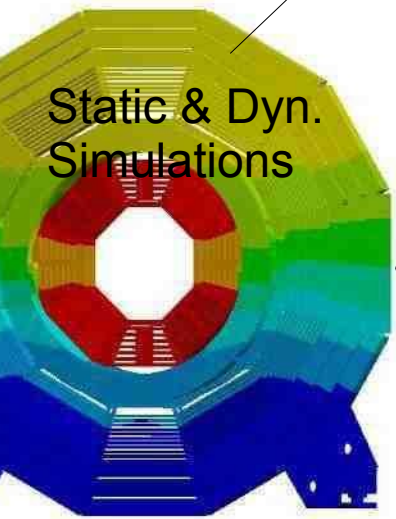




J1 = clearance between modules for the ECAL

J2 = Clearance at ECAL edges between ECAL and HC

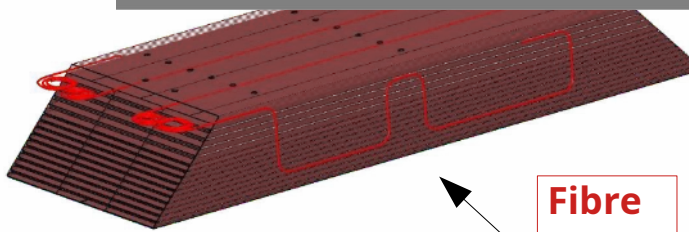
h = height of the rails 30mm



Static & Dyn. Simulations

Thick Carbon HR plate Th. 13 mm , with inserts and composite rails done by thermo-compression

Moulding of one layer of 3 alveoli **L = 2.490 m** wall thick. = 0.5mm



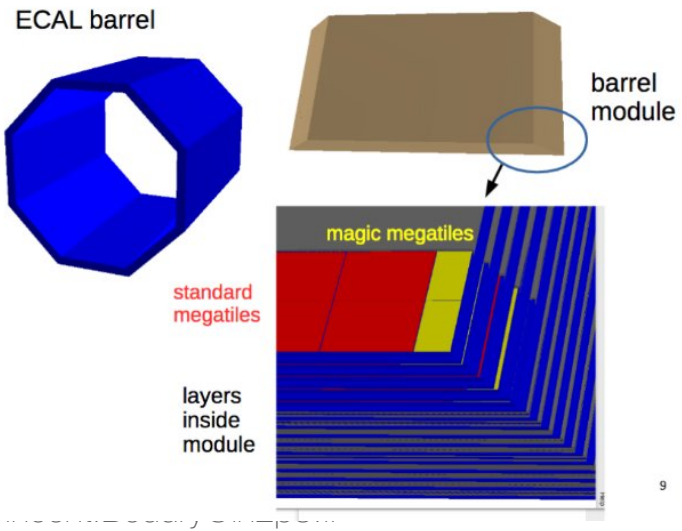
Fibre Bragg-Grated

measurements still to be done...

Simulation

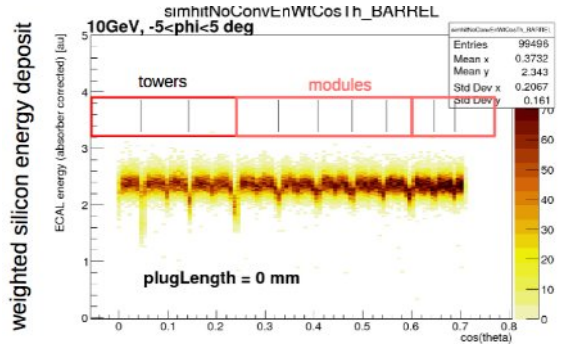
ECAL driver used in ILD models has been largely re-written (➡ DD4HEP)

- more modular code:
- less duplication Barrel & Endcap
- more configurable…

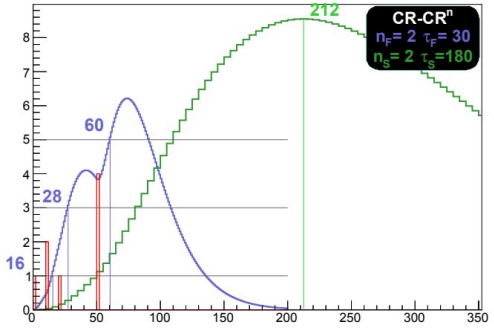


Effect of cracks [RAW= no correction at all!!]

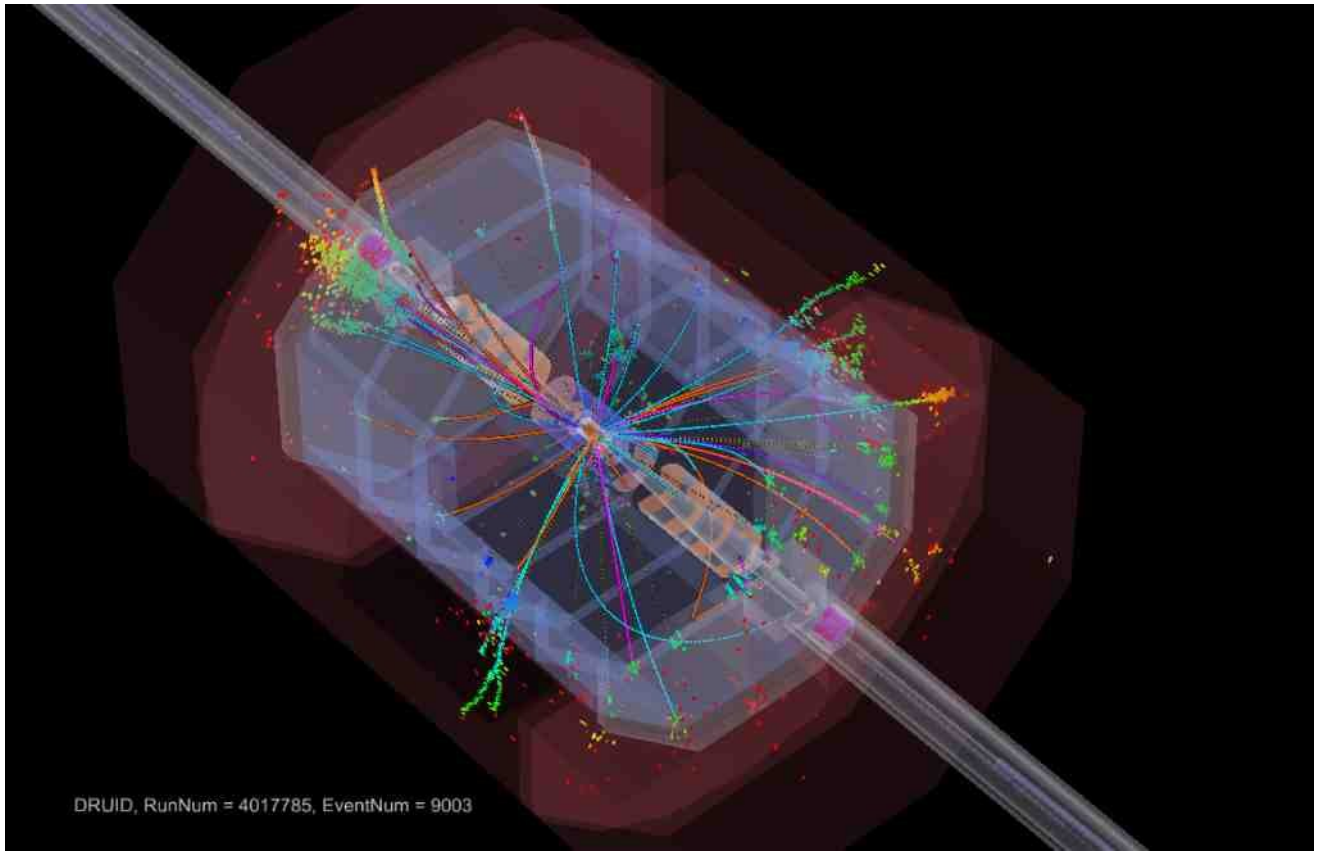
- Drop ~ 15%

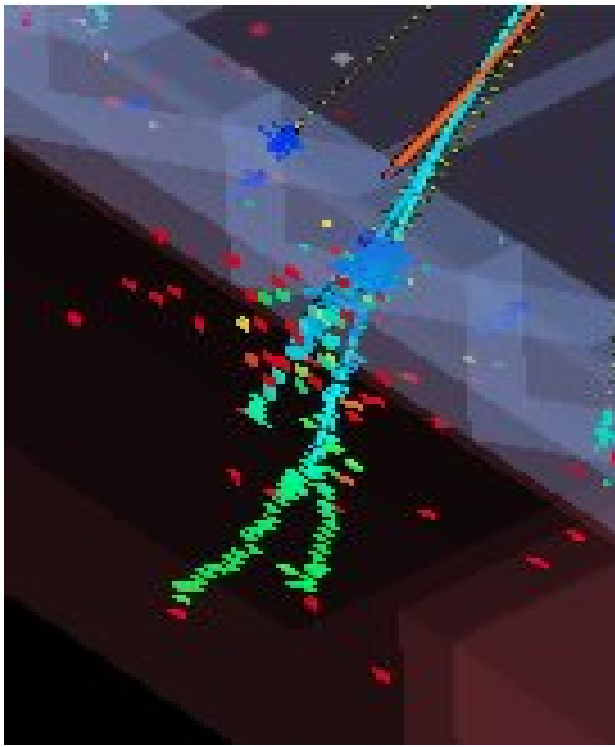


Improved digitization, modelling the SK2 (& beyond) ➡ ⊃ timing



Timing requirements: reflexions on-going





Implication of HL schemes

Higher $\mathscr{L} \Rightarrow$

- Occupation / bunch train ↗
  - More memory for events
    - But large margins

Higher repetition rates × longer bunch

- Power = $f_{rep} \times \sum P_{ASIC\_part} \times \tau_{spill\_part}$
  - $\tau_{spill} = \tau_{Ramp\text{-}up} + \tau_{Train} + \tau_{Conv}$
    $= \mathcal{O}(\mu s) + \{...\} + \mathcal{O}(100's\ \mu s)$
    - $\tau_{Train} = \Delta T_{bunches} \times N_{bunches}$
    - $\tau_{Conv} \propto$ (occupancy + Noise > thr.)

Critical also for Power budget

⇒ Full ZERO suppr. needed

HL-ILC:

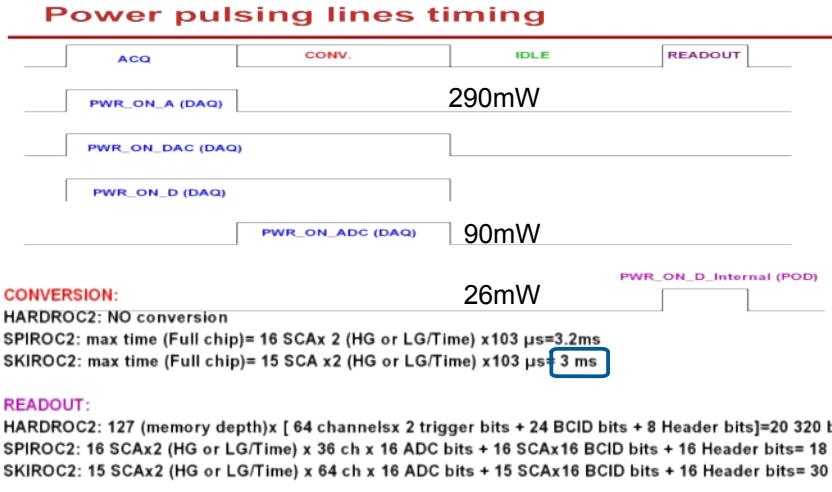
- $\mathscr{L}$ × 4 (6)
- $N_{bunches}$ × 2 : τ_{Train} : 1 → 2 ms
- f_{rep} ×2 (3): 5 → 15 Hz

Dominated by ACQ time:
P(~25µW/ch) × 6

HL-CLIC:

- $\mathscr{L}$ × 2
- $N_{bunches}$ → : τ_{Train} : 176 ns
- f_{rep} ×2 : 50 → 100 Hz

Dominated by Set-up & Conversion time: P (~82µW/ch) ×2



SK2 chips

64 ch full conversion

Detector Parameters: scaling rules

- Cell lateral size
  - Shower separation (EM~2×cell size)
  - Cell time resolution (1 cm/c ~ 30 ps)
    - Time performance for showers
      - ParticleID, easier reconstruction
- Longitudinal segmentation
  - sampling fraction
    - E resolution (ECAL ~15%/√E)
  - shower separation/start
- ECAL inner radius; Barrel Z_{Start}
- ECAL–HCAL distance
- Barrel–Endcap distance
- Dead-zones sizes (from Mechanics, Cooling)

Number of cells ↗ ⇒ Cost ↗ (1/size²)
Cell density ↗ ⇒ Power consumption ↗
Time resolution ↘ ⇒ Power ↗

threshold, passive vs active cooling
dead-zones ↗

NEED TO BE FULLY RE-EVALUATED for EW region

Inner Radius ↗ ⇒ Tracking performance ↗
Cost ↗² (⊃ Magnet, Iron)
Gaps ↗ ⇒ PFlow performances ↘

Review of physical implication (from TeV): see Linear collider detector requirements and CLD, F. Simon @ FCC-Now (nov 2020)
Physics Requirement studies @ 250 GeV: see Higgs measurements and others, M. Ruan @ CEPC WS, (nov 2018)

Summary of Activities: Present and To come

Beam Test operation (finaly !)

- DESY20-03 ➡ DESY21-11, DESY22-03 (CERN22-06)
- Many results to come
  - 15 layers ➡ 22–26 layers

New FEV design

- Improved Power, HV, noise, flexibility
- Workhorse for all operation
  - Stack with single / double ASU layers
  - Long SLab v2 (~all equipped)
- Availability limitd by €€€ for sensors
  - bunch from 2021's travel money

Many issues to be looked at:

- validation of thermal scheme (global simulation)
- Validation of mechanical scheme from existing prototype.
- Estimation of optimal of timing
- optimisation of power/performances
- requirements for a SK3

They all depends on the machine (⊃ HL-ILC)

- circular ≠ linear
  - manpower on system is wanning

BACK-UP

Electronics & DAQ

Ωmega ASICs:

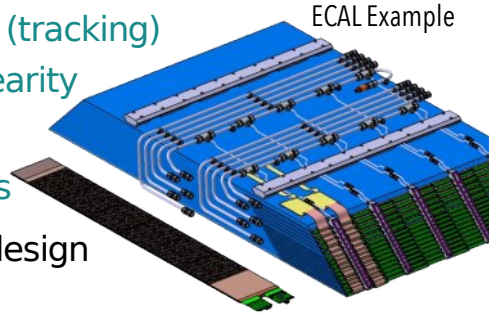
- A set of ASICs adapted for all CALICE large scale prototypes
  - Gradual improvement
  - Purely digital DAQ
- suitable for ILC conditions
  - **low power** consumption using **power-pulsing (~1%)**
  - **low noise** pre-amp, dual gain 12-bits ADC, ns TDC
  - **self-trigger** with local storage, **delayed** digitization and read-out
  - **high integration** (36–64 channels), daisy **chaining**

R&D:

- will required update for final integration: ~3⁺ years of dev
  - full zero-suppression, I2C bus, new technology
  - Improvement of Timing ? **Learning from CMS-HGCAL ASIC**
- **new scheme needed for circular colliders** (power, readout)
  - **Decision on DAQ Scheme : continous vs triggered ?**
    Central trigger → lower noise requirements, **feasible ?**

Technical requirement on prototypes:

- Integration in cassettes 150 – 300 cm long
- 12k – 27k cells (200–500 ASICs), power pulsed
  - sensitivity to mip signal (tracking)
  - uniformity, stability, linearity
- Reproducibility
  - Typically ~20–50 layers
    - will be ~ 10^4 in final design
- Ex: HGCAL HCAL



DAQ:

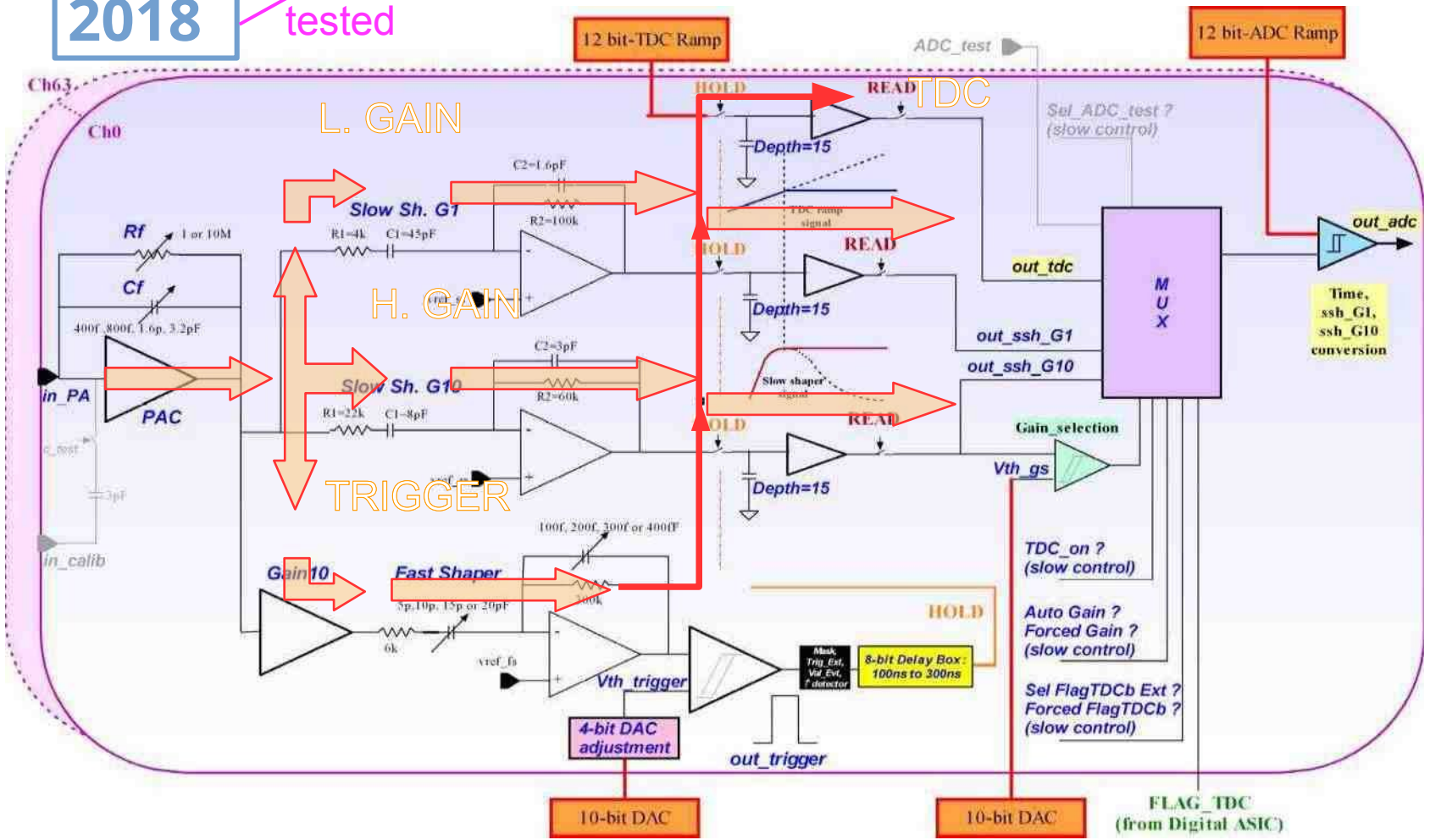
- Low power, Small size interfaces
  - ECAL–HCAL = 3 cm, HCAL–Coil or Barrel–Endcap ~ 5-6 cm
- Single side readout

~~**ILC: Pulsed Powering in 2–4T field…**~~

- ~~Passive cooling, local power management~~

SKIROC2 / 2A Analogue core

2018 tested

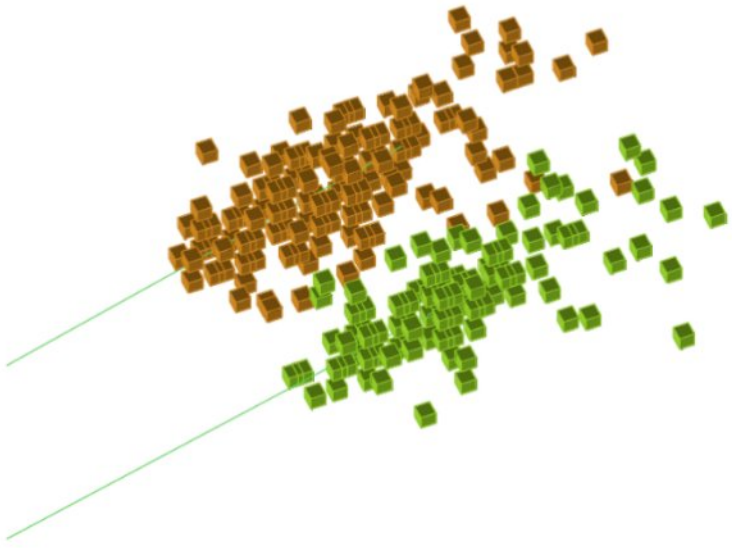


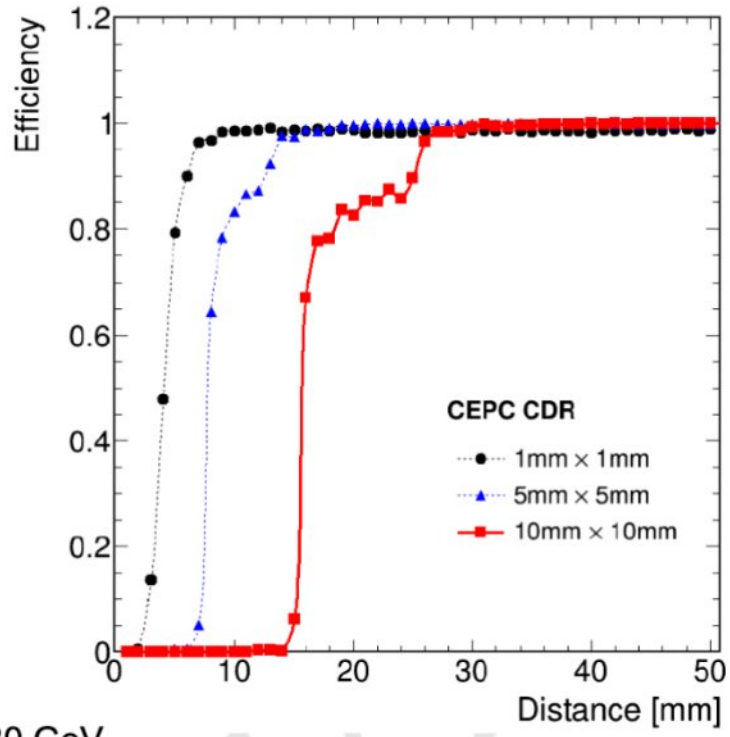
Similar to SiD Kpix

- 64 channels
- Preamp
  + 2 (auto)Gains
  + **TDC** (~1.4ns)
- Auto-triggered
  - per cell adj.
- 15 (×2) analogue memories
- Low consumption
  - 25 µW/ch with 0.5% ILC-like duty cycle
- Power-pulsed

Not final chip
(full 0-suppr.)

Clustering



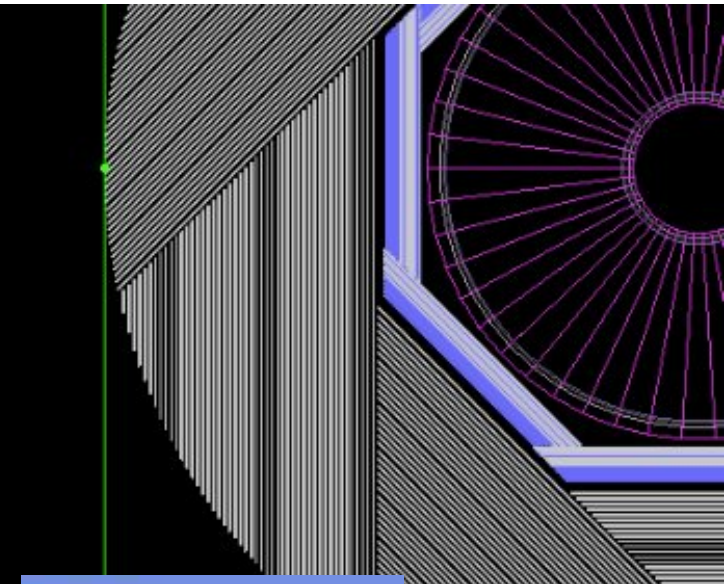


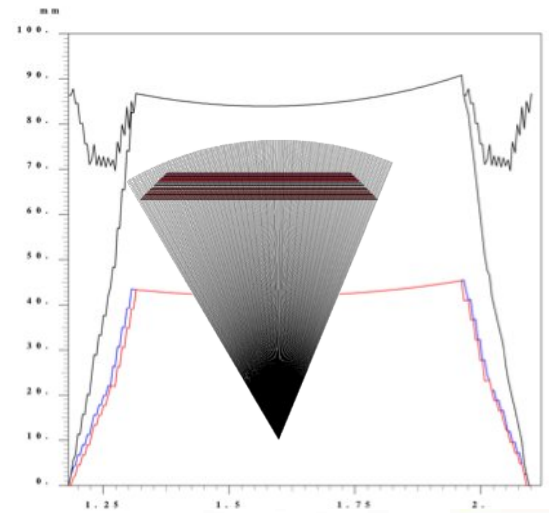
Critical energy to separate an evenly decay π_0: 30 GeV

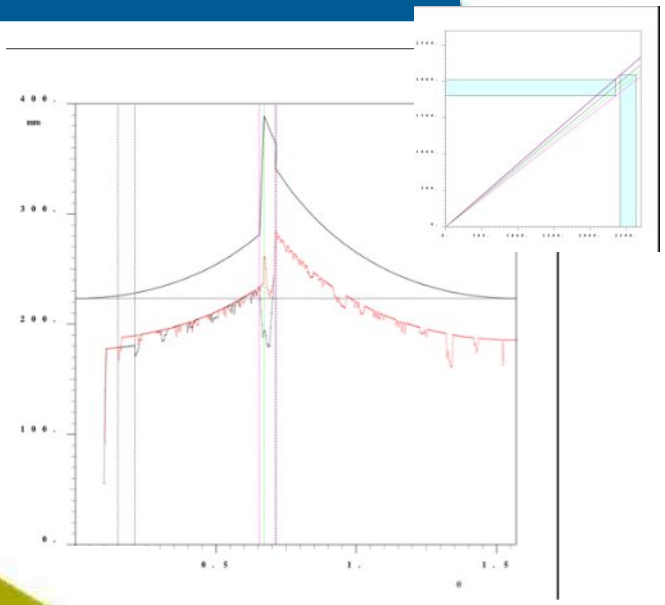
See Hang Zhao's talk

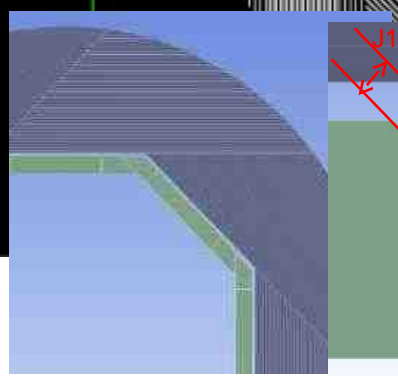
18/11/19 CEPC WS@IHEP 27

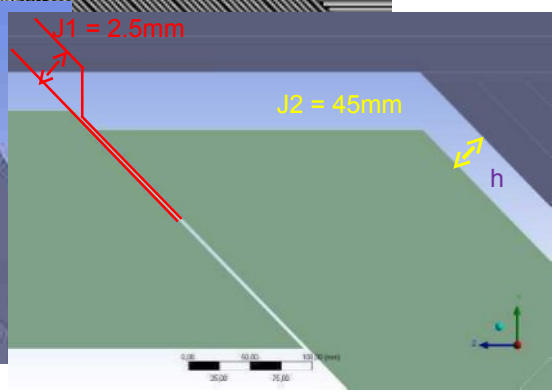
A crack-less ECAL geometry

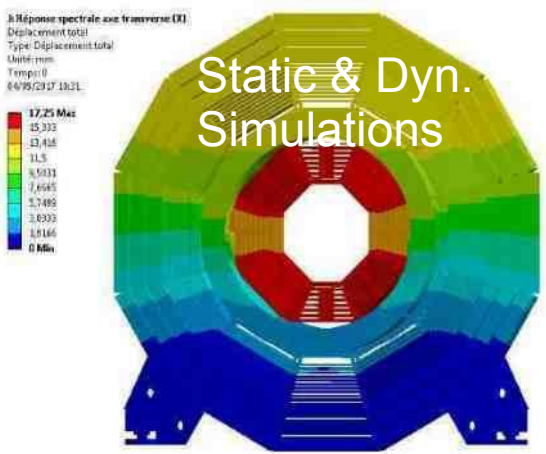


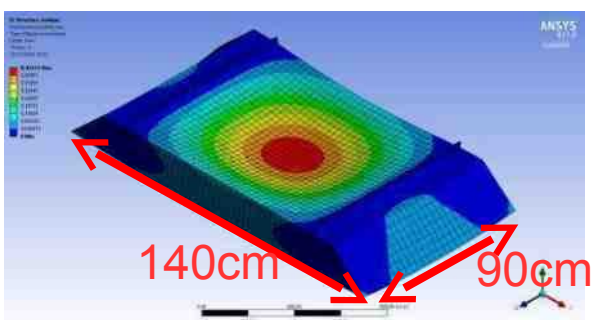




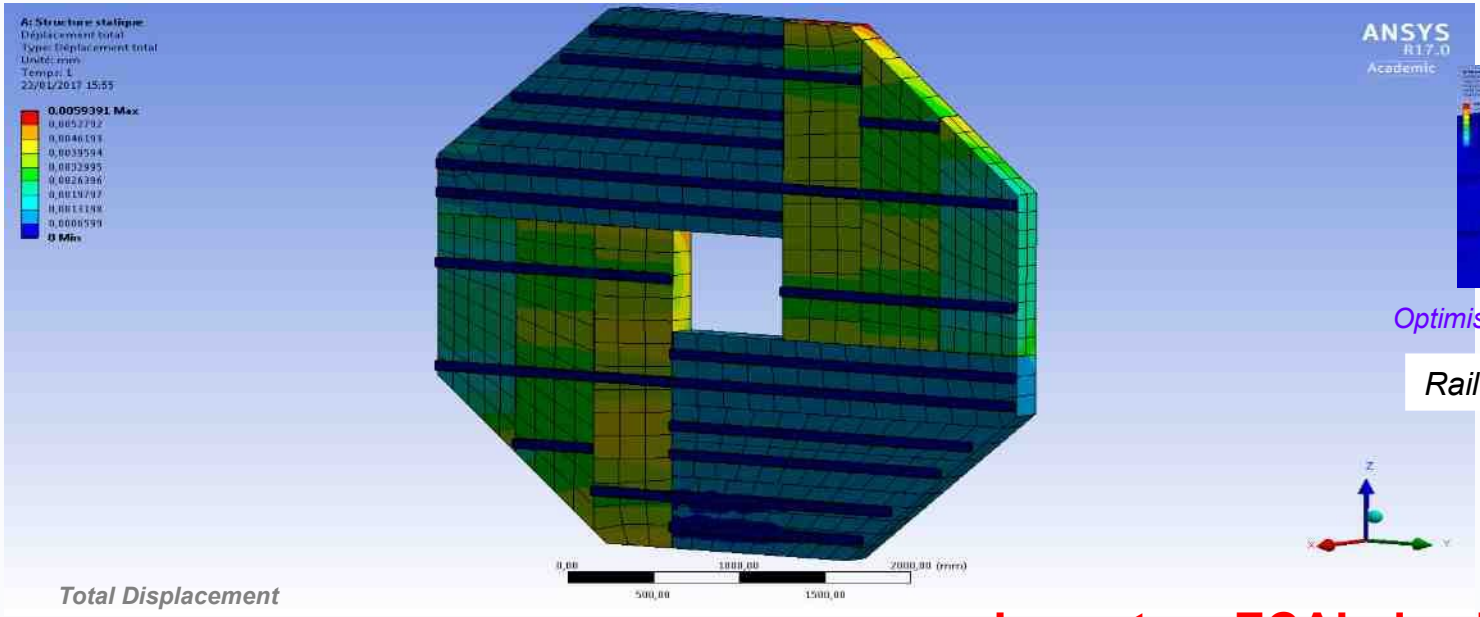




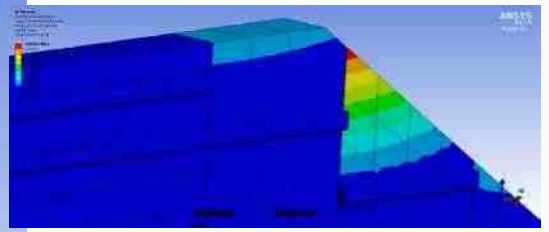




Structure composite & séisme



Total Displacement

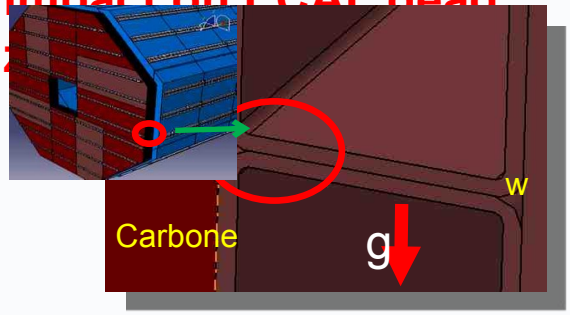


Optimisation on going / rails localisation/ on going

Rails fixed

Mode	Fréquence [Hz]
1,	203,56
2,	204,24
3,	206,17
4,	208,13
5,	211,64
6,	212,02

Problem of bending stress of alveoli skins: influence / evolution of thickness of outer plies



Shearing tests stress in the structure

Safety coefficient

- Static: Sufficient / to the stress induced by weight of modules
- just sufficient / seism (s =3.2 for Japan?)
  / risks during integration and transport

-> increase nb of ext. plies... Impact on ECAL dead zone=0,5mm= 1 extra external ply on modules