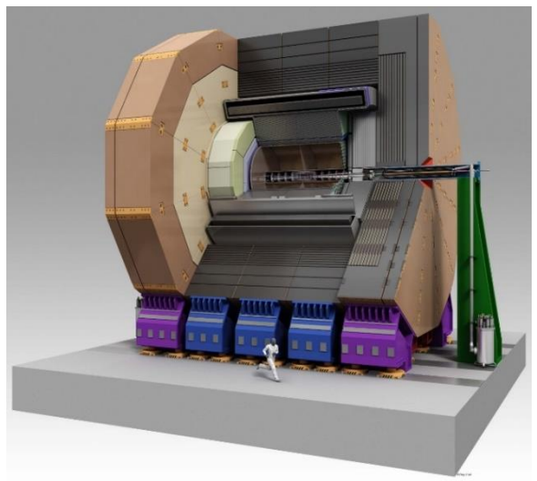
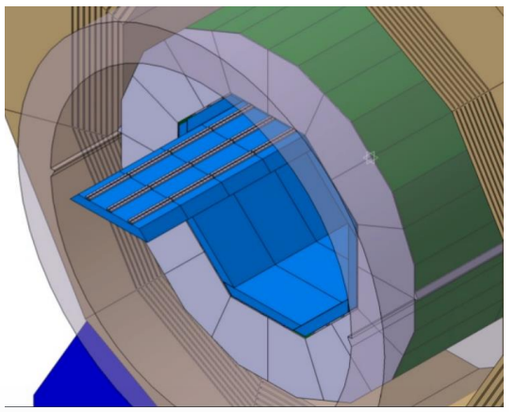
Status of SiW Ecal Digital Readout Electronics and news about new FEV 2.0

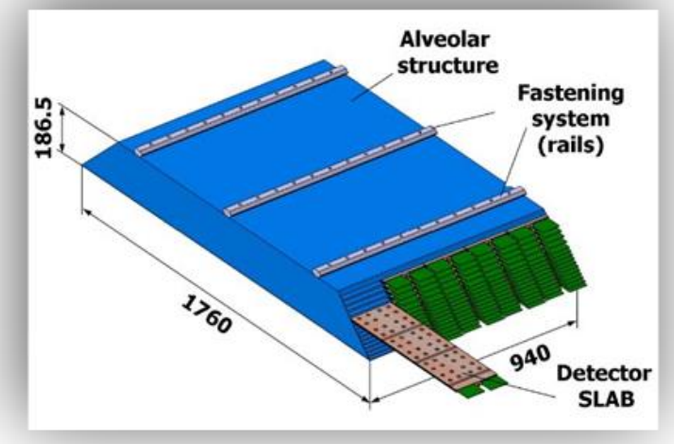
Jihane Maalmi on behalf of the SiW Ecal Team

Introduction





- Update on Siw Ecal digital readout electronics and DAQ software
- Two test beams with 15-layers prototype
  - Nov 2021
  - March 2022 : one week synchronized data with AHCAL prototype.
- New Front End Board FEV2.0
- Future plans



Reminder:
Constraints on Readout Electronics

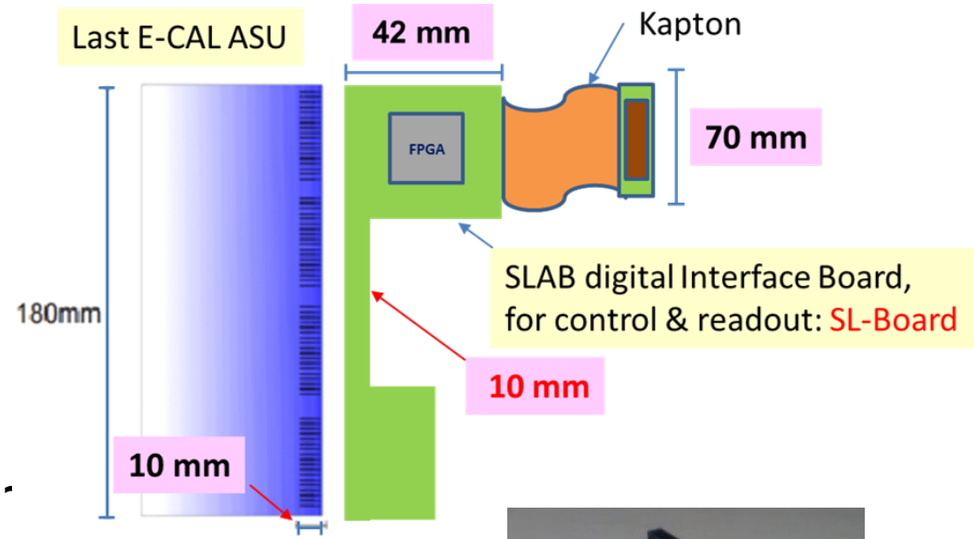
Spatial constraints for the Active Sensor Units (ASUs)

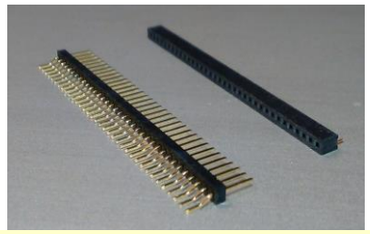
- Very limited space **between layers (depending on the total number of layers)**.

➢ Two protoype versions have been realized with different SKIROC packaging and thickness:

✓ BGA option : PCB + components*(1,2 mm)* + connectors = **3,2 mm**

✓ COB (Chip On Board) option : PCB and ASICs **= 1,2 mm** + connectors = **~2,3 mm**

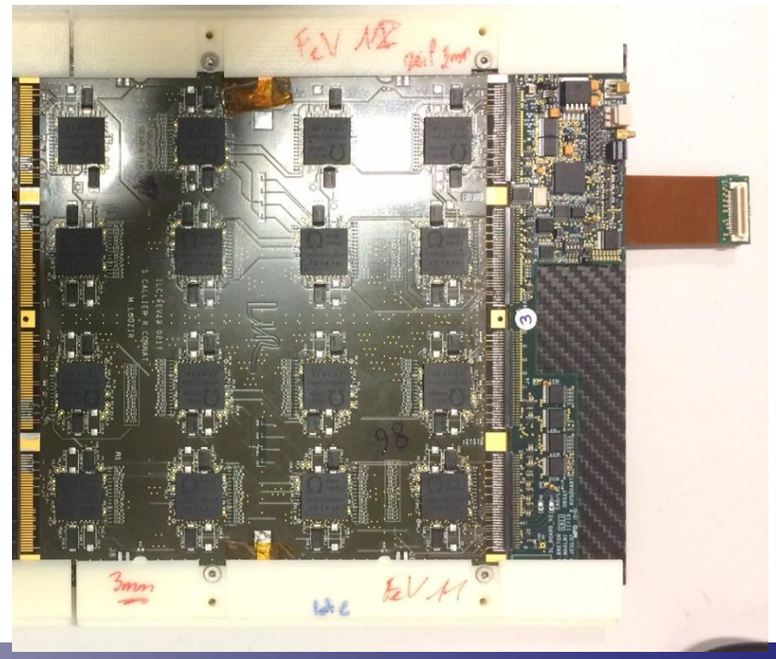




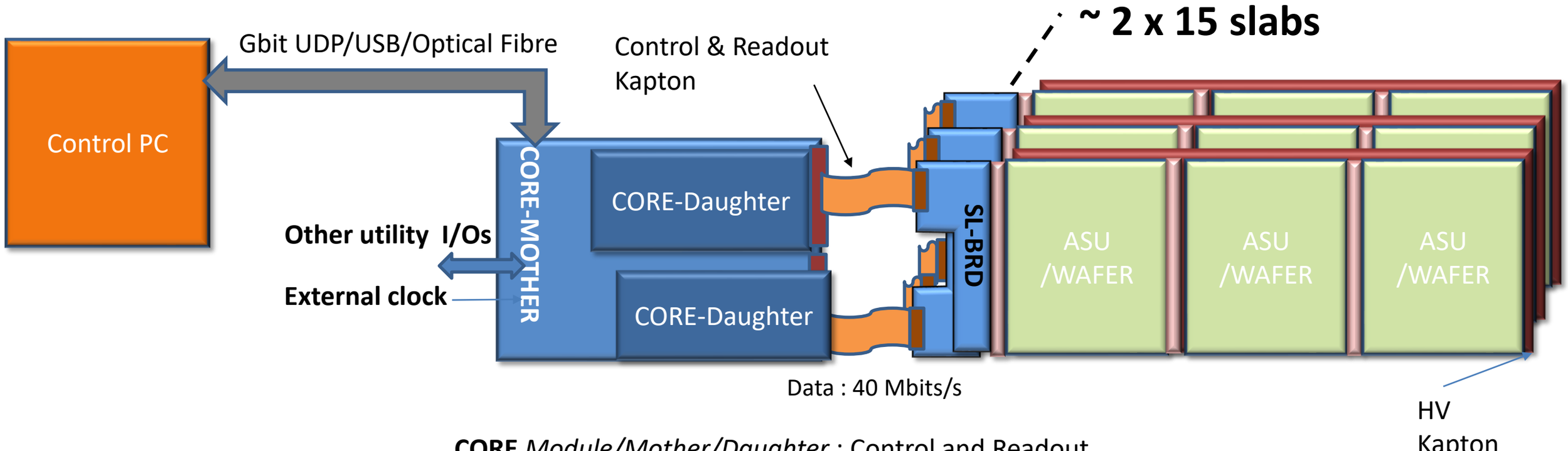
Antelec connectors (1,5 mm high)

Constraints for the Slab Interface Board (SL-Board)

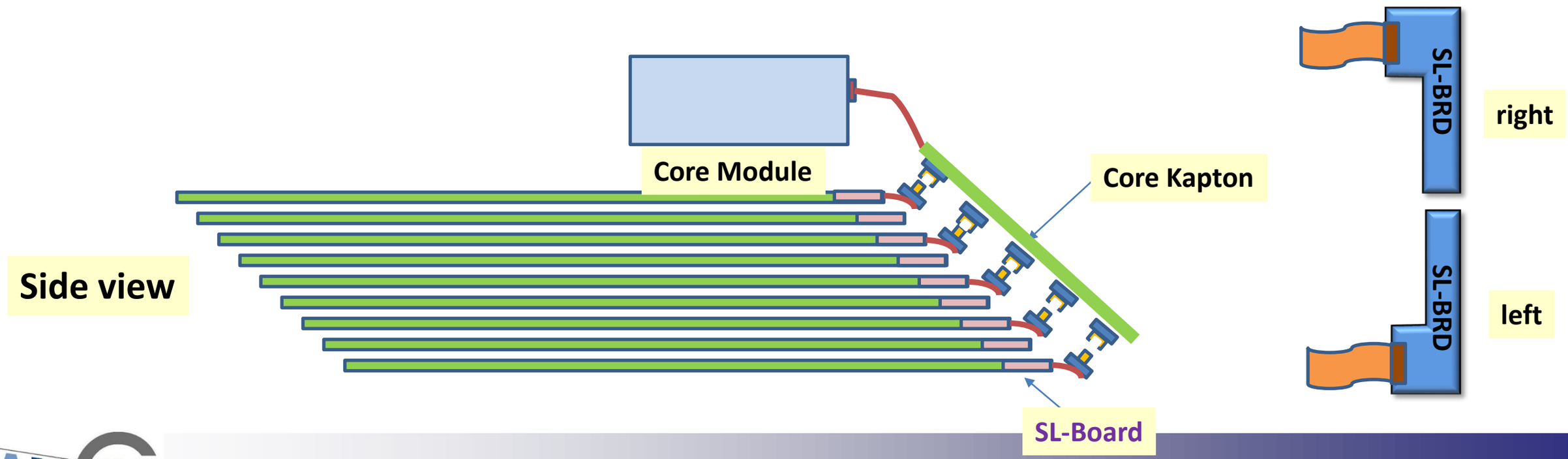
- The Sl-board will be installed between ECAL and HCAL, separated by only 67 mm
- L-shape because of the cooling system
- Maximum Height : **6 to 12 mm depending on the location**
- **Control & Readout electronics at the extremity of the Slab**
- Signal Integrity over a Slab : up to 15 interconnected ASUs
- Very low Power consumption (~ 150 mA/ Slab) : needs to run in **power pulsing mode**



Global Architecture Scheme



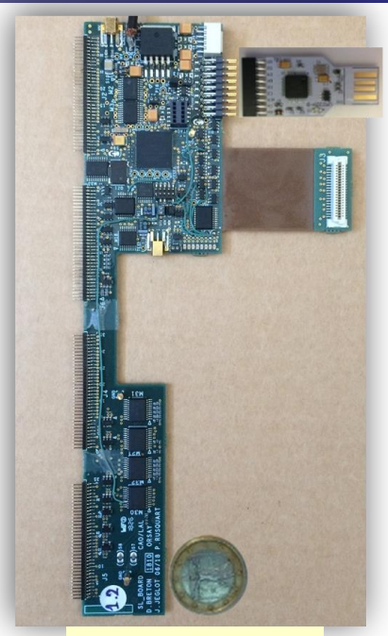
CORE *Module/Mother/Daughter* : Control and Readout
SL-BRD : Interface board to Slab



The SL-Board (V1 → V2)

The **SL-Board** is the sole interface for the **~10,000 channels of a slab :**

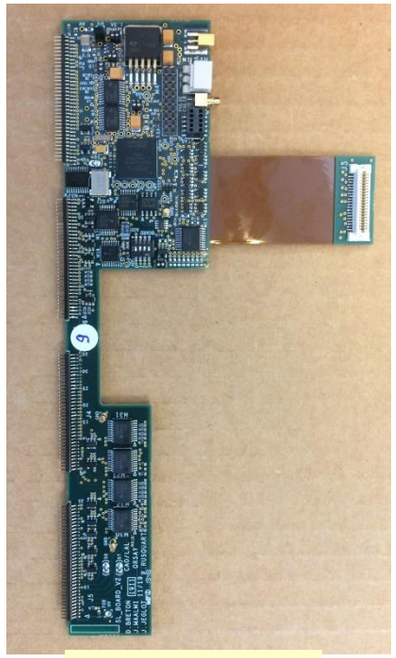
- It delivers the **regulated power supplies,** including **High Voltage**, **controls** the SKIROC ASICs, and **perfoms the full data readout**.
- It is connected to the CORE-Kapton via an internal **kapton layer** and a 40-pin connector.
- It is based on a **MAX10 from ALTERA**, which is a mix of CPLD and FPGA.
- It includes an ADC which will be used to monitor the pulsed power supply.
- Very size **limited:** 18 cm in width, 10 to 42 mm in length.
- Its **own power** consumption is **< 1W**
- It can also be an **autonomous system** with direct computer access for testing and characterization purposes (using the **FTDI USB module**).



SL Board V1

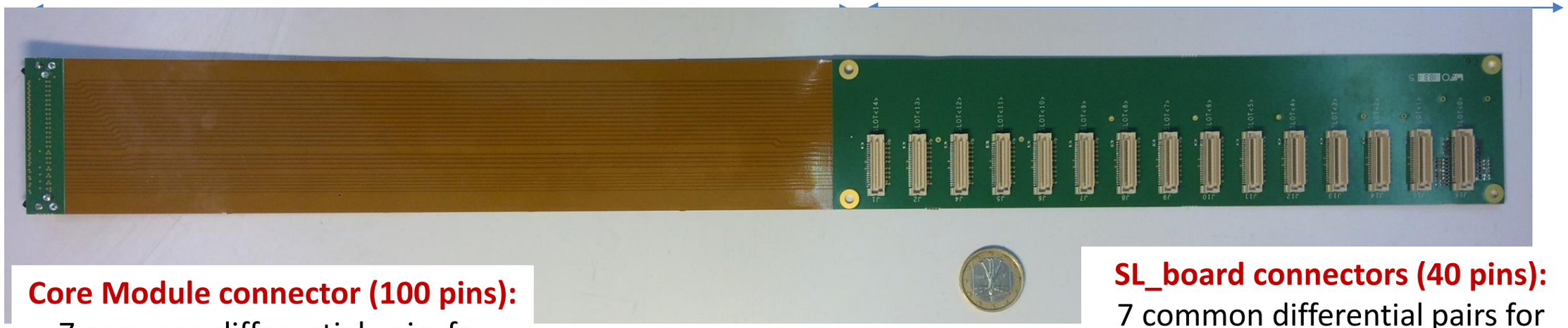
Going from V1 → V2:

- All useless circuitry has been removed and the rest optimized
- more robust LV connector
- A **switch** has been added to encode the **slot number**
- **a Flash EEPROM for permanent information storage: Serial Number**
- Kapton length has been raised from **40** to **48 mm**
- **a DAC for SKIROC ADC calibration**
  → **The FPGA can produce pulses for autonomous functional calibration of both gains**
- **The HV will be made available on the SL_Board to ASU connectors (both sides)**



SL Board V2

The SL Board Core-Link (Core-kapton)



Core Module connector (100 pins):
7 common differential pairs for sensitive signals, *30 individual pairs* for control and readout, 14 common lines, GND

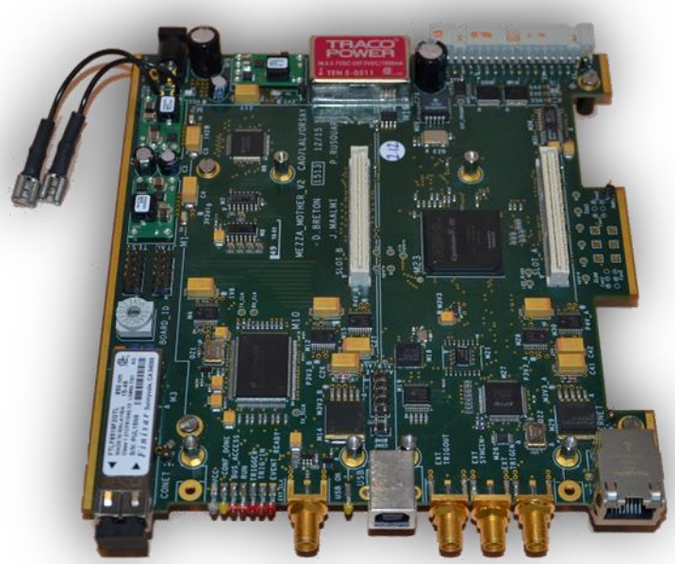
SL_board connectors (40 pins):
7 common differential pairs for sensitive signals, *1 individual pair* for control and readout, 14 common lines, GND

- The **CORE kapton** measures 40 cm. It is the **interface** between the CORE Daughter and the SL-Board. It permits driving and reading out **up to 15 slabs**.
- It transmits all the **clocks and fast signals**, and houses the control and readout links.
- It handles the **synchronisation** of the **15 slabs**.
- The Kapton Interface makes use of **asynchronous serial transmissions** in order to greatly simplify the synchronization of the numerous control and data links.
- The speed of the slow control and the individual readout links is : **40 Mbits/s**
- Reminder : readout link of the ASUs **: 2 x 5 MBits/s**

The CORE Module

The CORE Mother:

- The **Control and Readout Motherboard** have been developed for housing up to 2 **Mezzanines**: it permits separating the **acquisition** part from the specific front end part.
- **External** input and output signals permit **synchronising** or interfacing the module with other systems.
- The CORE mother sends common clocks and fast signals to the Core Daughters to keep the **system synchronised**
- The control and readout is possible through **USB(2.0)**, Ethernet (secured UDP) over copper **or Optical link**
- The CORE module **power consumption** is **5 W**

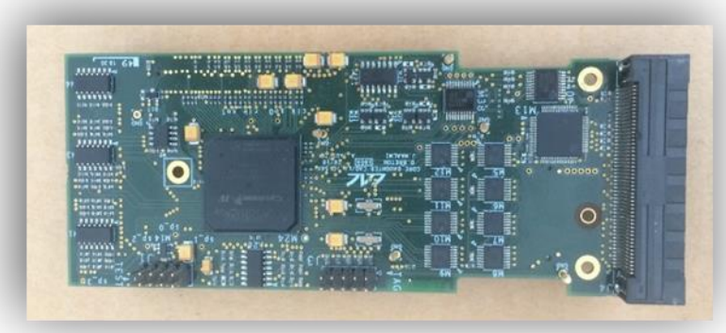


The CORE mother

The CORE module

The CORE Daughter:

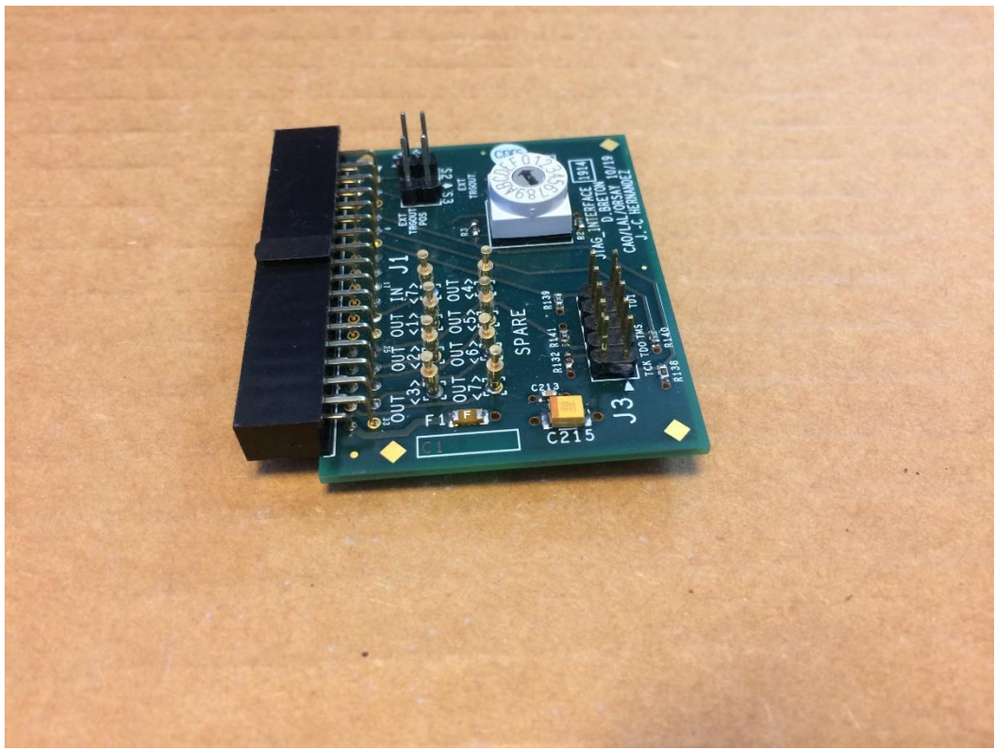
- The **CORE Daughter** is based on a Cyclone IV FPGA. It is the interface between the CORE motherboard and the Kapton which permits driving and reading out **up to 15 slabs**.
- It buffers all the clocks and fast signals, and deals with the control and readout links through the Kapton Interface.
- It houses the second level of **event buffers** (derandomizers)**.**
- Ctrl & Readout link between CORE Daughter and CORE Mother **: 60 MBytes/s** if USB**, and 125 Mbytes/s** if UDP**.**

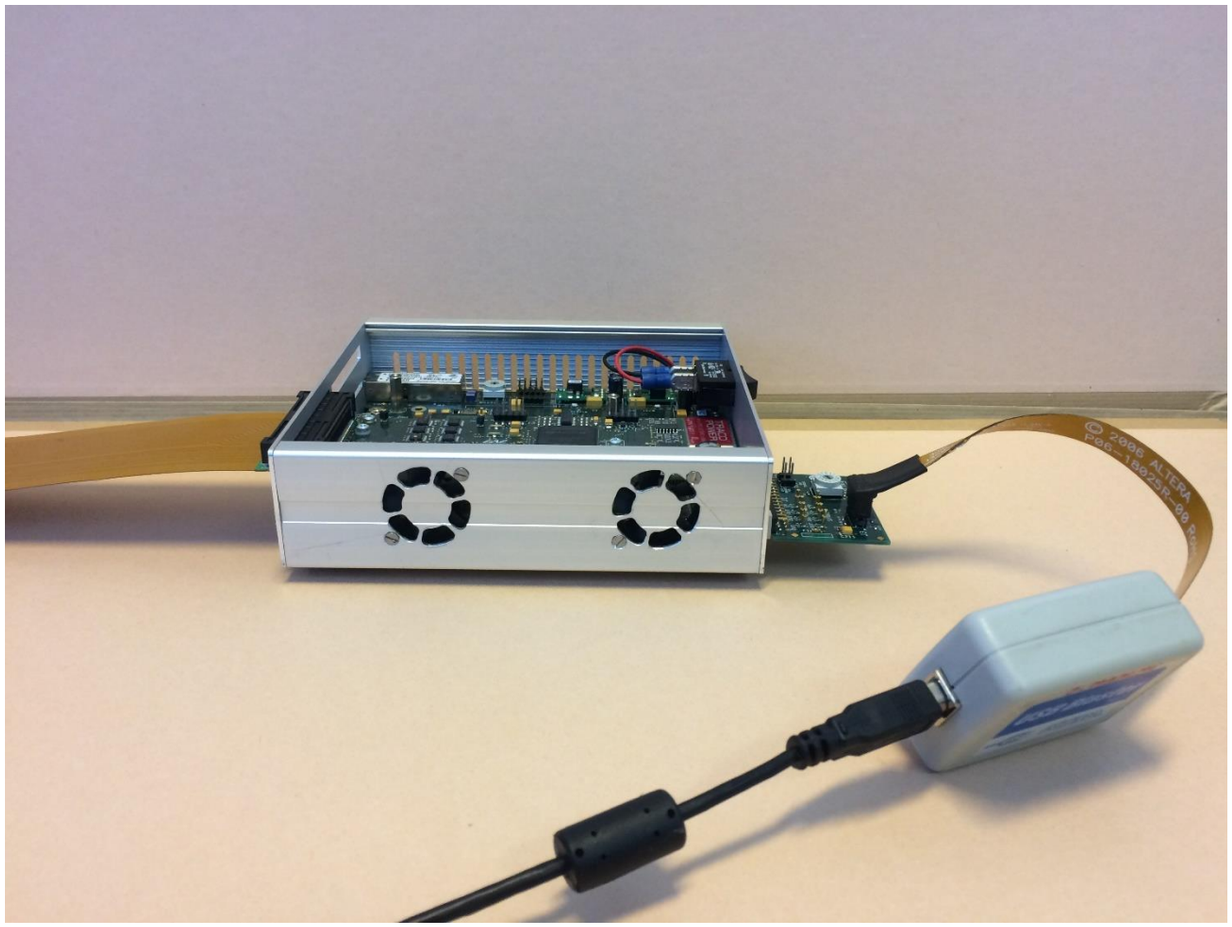


The CORE daughter

Programming Firmware through CORE module: The JTAG Interface Board

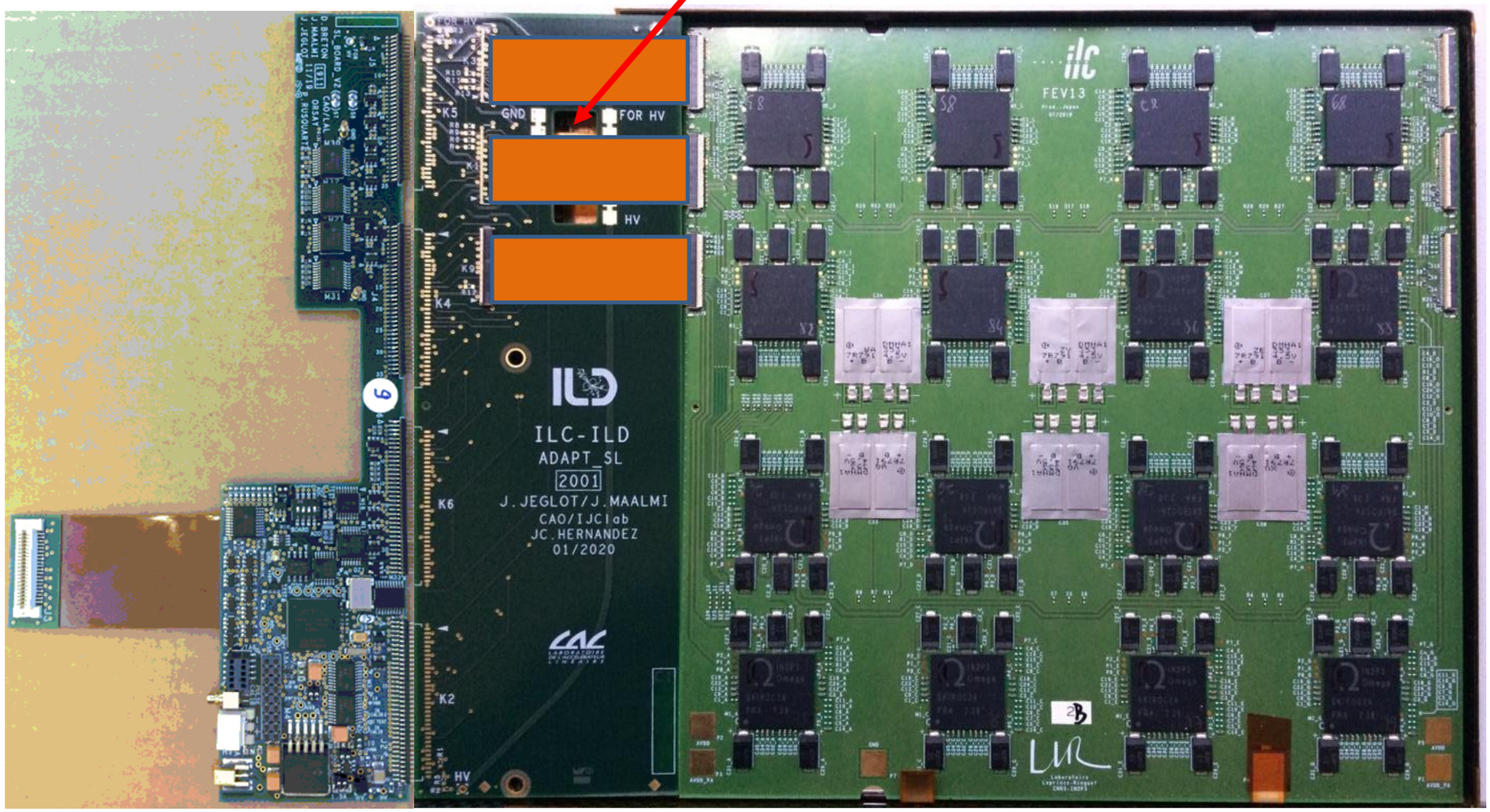
- We designed this board in order to program the SL Boards Firmware through the CORE Module via the Core Kapton.
- Unfortunately we can not program all SL Boards at once: need to use the encoding wheel to select the SL Board Address.

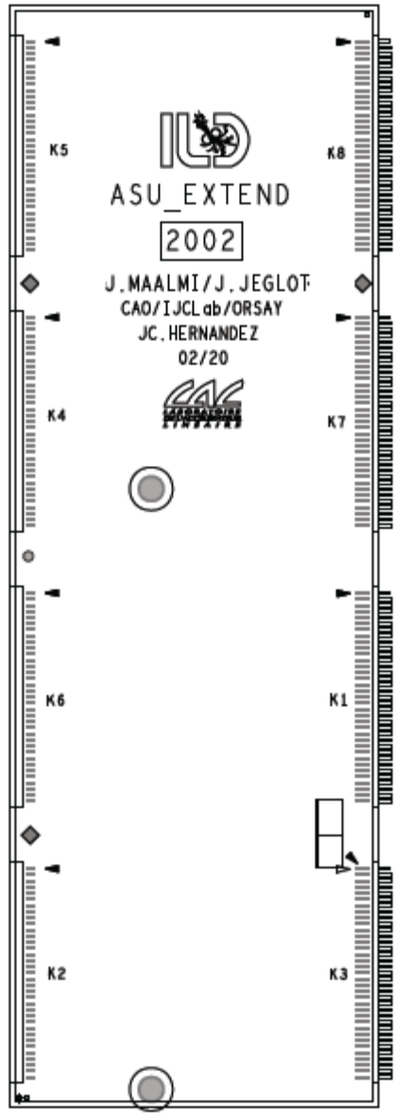




Interfacing SL_Board to FEV13:
design of the SL-ADAPT board

The new **SL-ADAPT interface** board permits the **control** and **readout** of a **FEV13** by a SL_Board. A **hole below the 3 kapton** cables permits connecting the high voltage for the wafers.

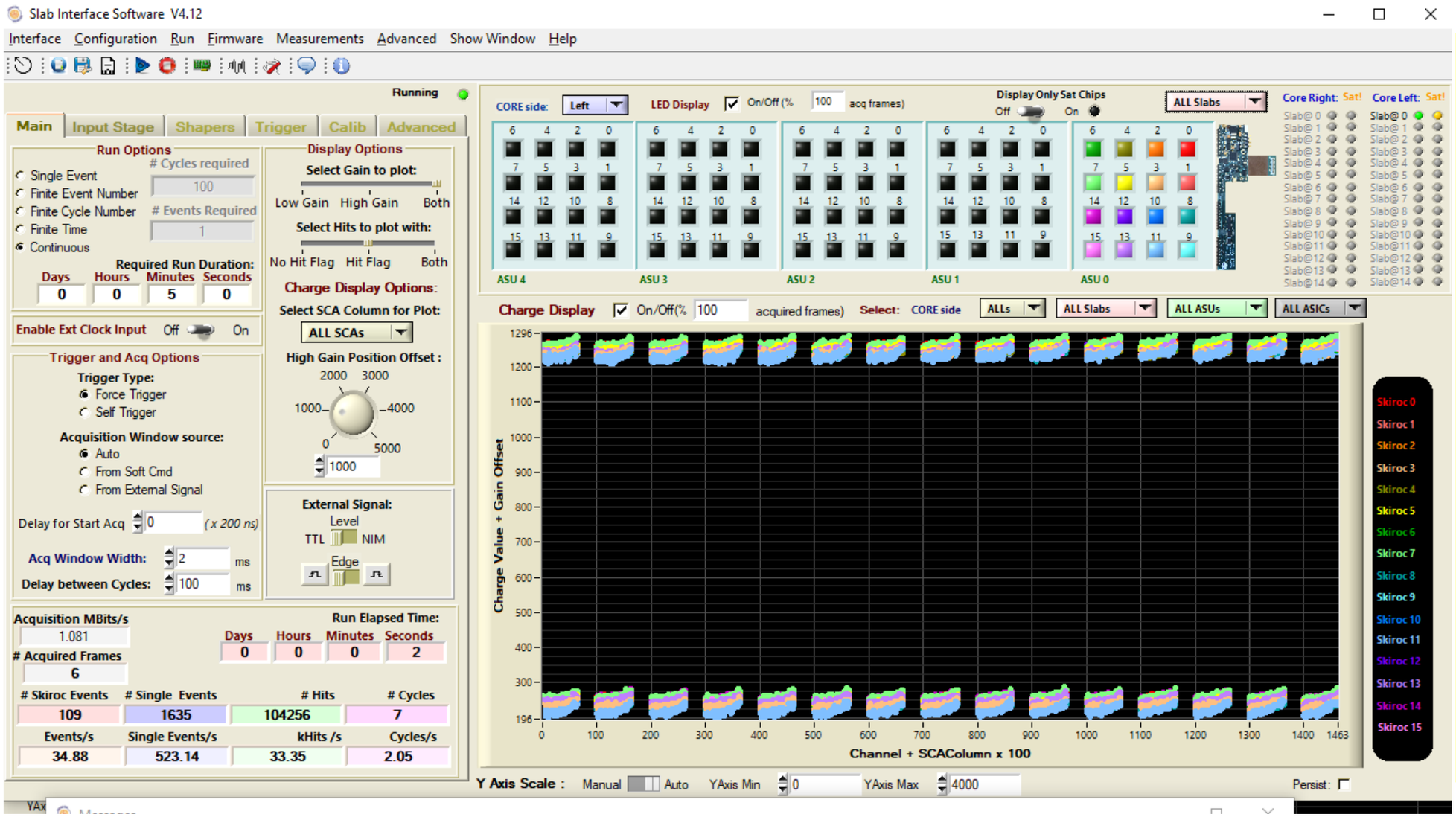




ASU_EXTEND Board

➔ To align all the FEVs11/12 with the FEV13

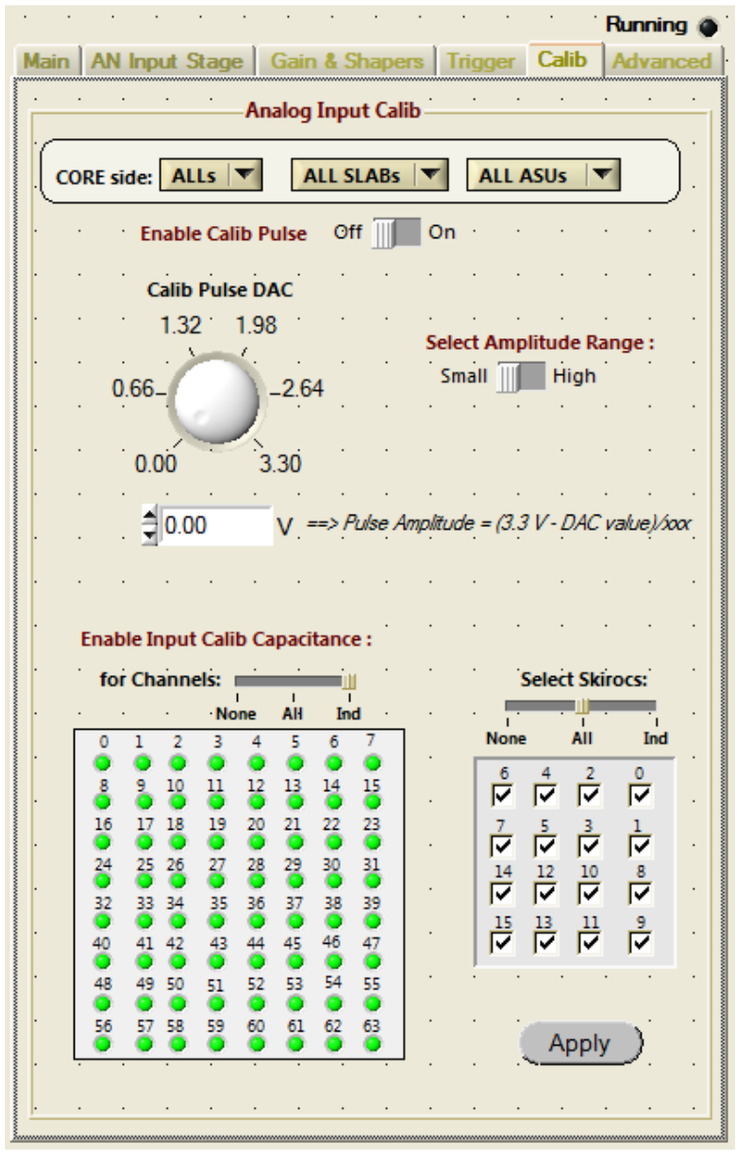
Acquisition Software



- The Software can handle the communication through FTDI connector **or** through **CORE Module**.
- It handles the **whole detector module**:
  - **Two sides with 15 SLABs each.**
  - **Each slab with up to 5 ASUs.**
- It written in **C** under **Labwindows CVI**
- Advanced measurements can be performed Online such as threshold scans…

- All the hardware components are detected automatically : **Number of daughter boards**, **number of SL Boards** connected to each daughter board, **FEV Type** (FEV 13 or 11/10 ..) and also the **number of ASUs** on each slab using **slow control readout**.
- **Slow Control**:
  - All necessary slow control **parameters** can be programmed through the Software
  - Slow control configuration is checked by writing twice the same values to the SKIROC shift regiser and reading back the pushed value on the SROUT signal.
- Control and data Readout with **direct connection** to the SL Board via FTDI module or through the **CORE module**.

Calibration Pulses

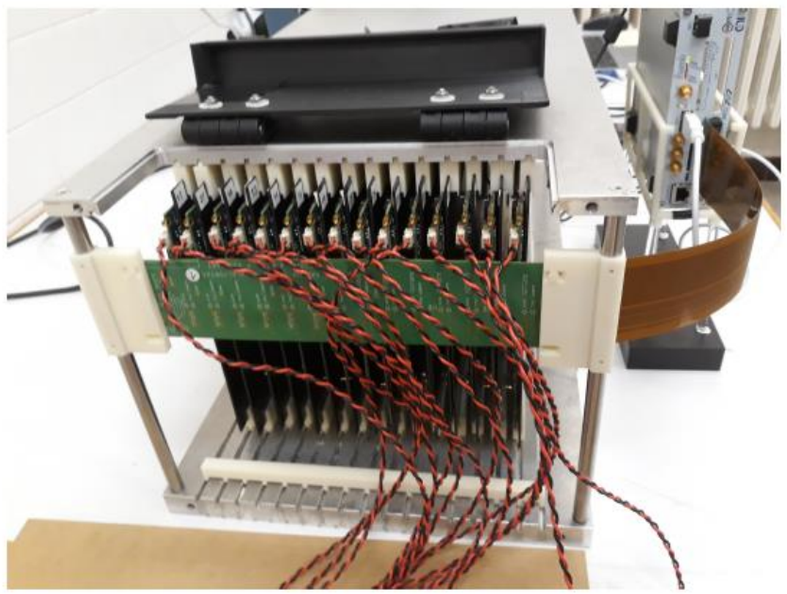


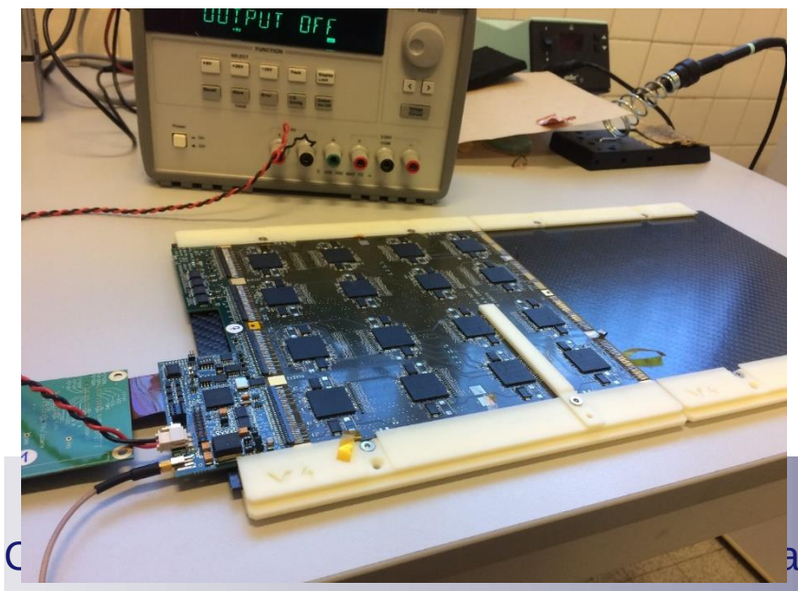
- We have two ranges of amplitudes: in order to test High and Low Gain.
- Thanks to the DAC on the SL Board, we can send Pulses with Amplitude from ~few mV to ~150 mV.
- The FPGA can generate equidistant pulses with known distance:
  - Permits testings the synchronization between multiple layers
  - we can study the Re-triggers…

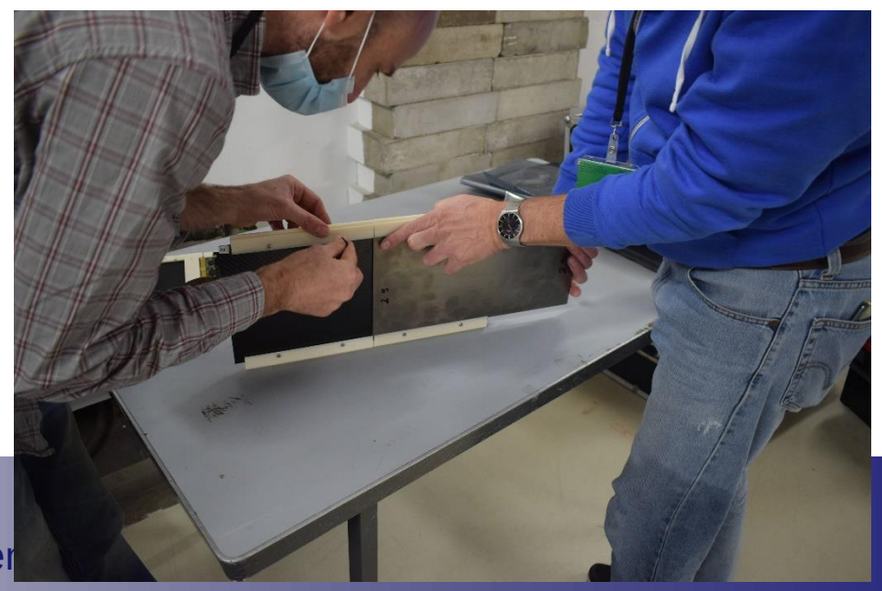
➔ Thanks to this feature we can adjust the Common Threshold/ ASIC and the individual thresholds for each channel to trigger on ~0.5 p.e

Test Beam at DESY in November 2021
First test with 15 Layers!

- We prepared this test beam **since 2020!**
- **Improved mechanics:**
  - Improvement of the prototype box: modification of the front panel for giving a better access to all connectors of the SL Boards.
  - Better fixation for the ASUs
- **Hardware** : SL Board V1→V2
- **Software:**
  - Online **hits histograming** per channel
  - Handling of **DESY Moving Table** (TCP/IP)
  - Auto-increment of run numbers
  - **Temperature/AVDD** monitoring
  - …



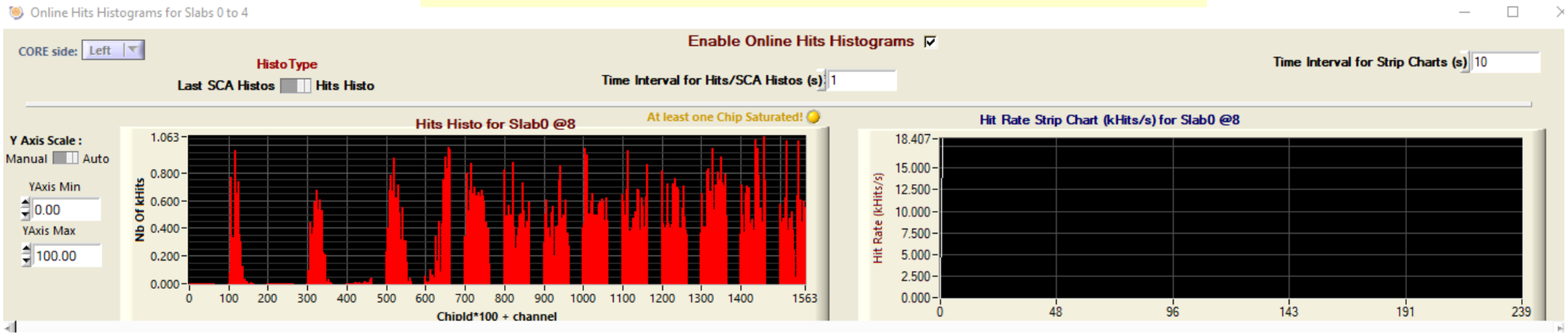




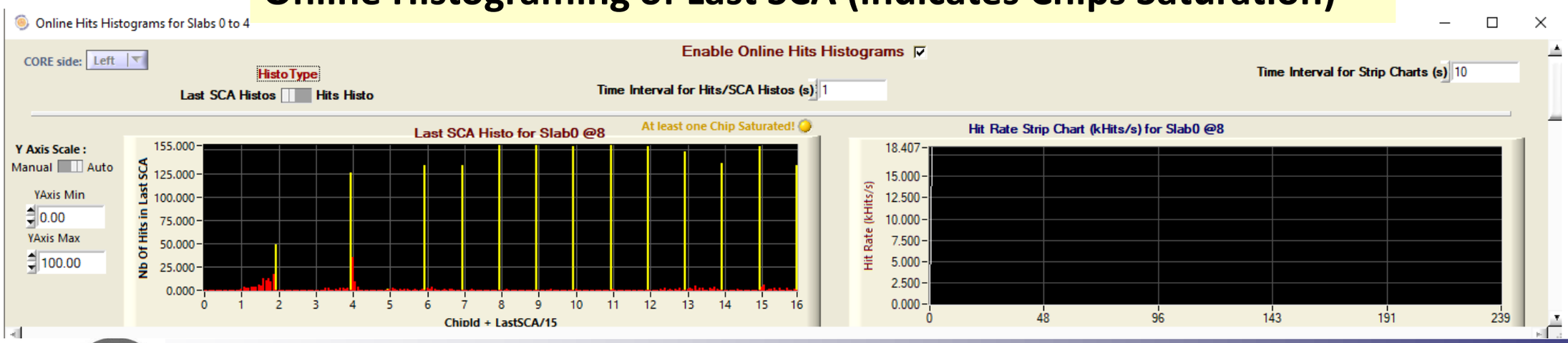
Improvements in preparation of test beam March 2022

- We learnt that we needed **more Online monitoring tools**
- Minor firmware bugs corrections
- We had to improve some **cablings** (HV cables an LV connectors on the patch panel)
- Need to use **Binary data files** to increase data rate.

Online Hit Histograming and Strip Chart

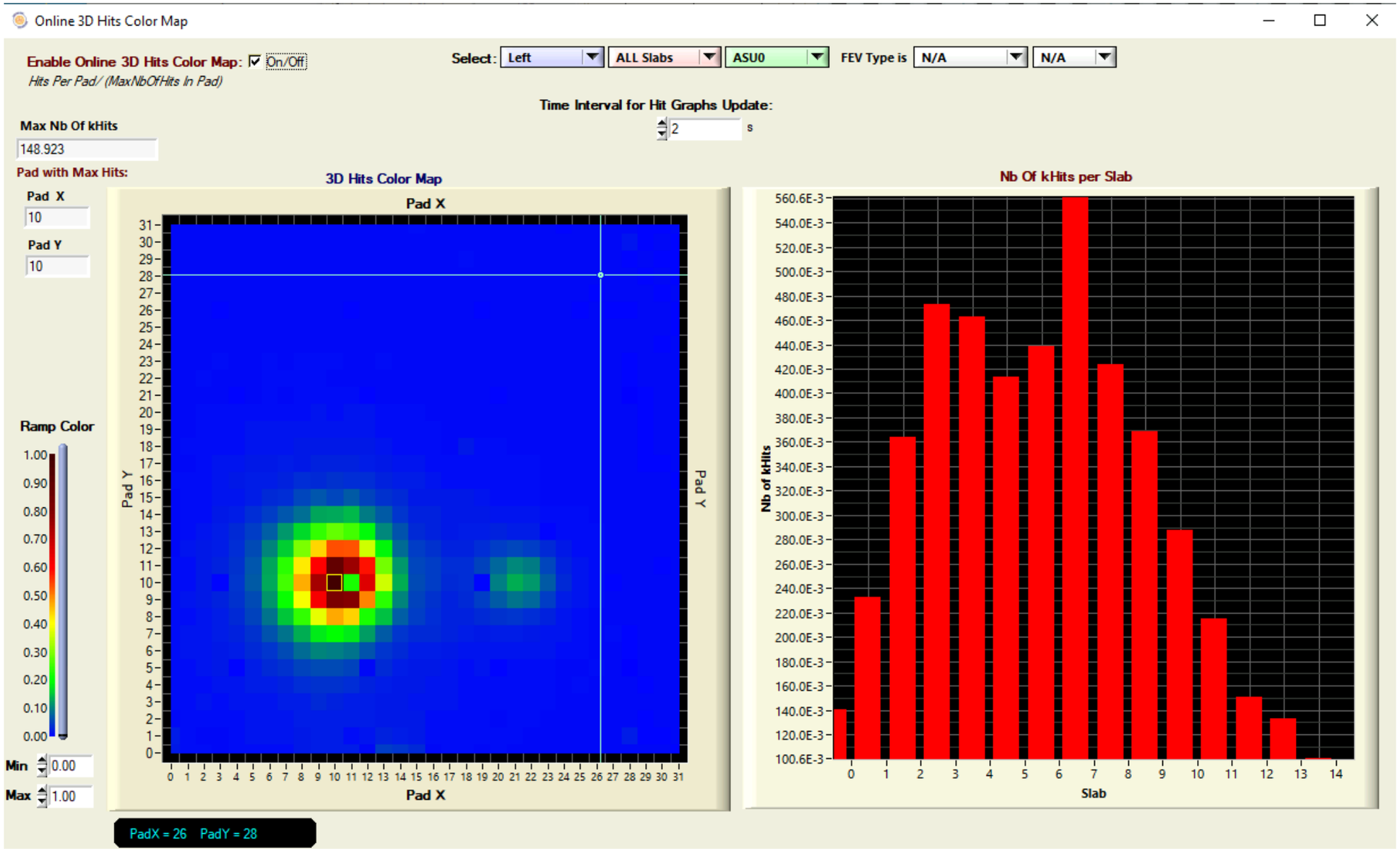


Online Histograming of Last SCA (indicates Chips Saturation)



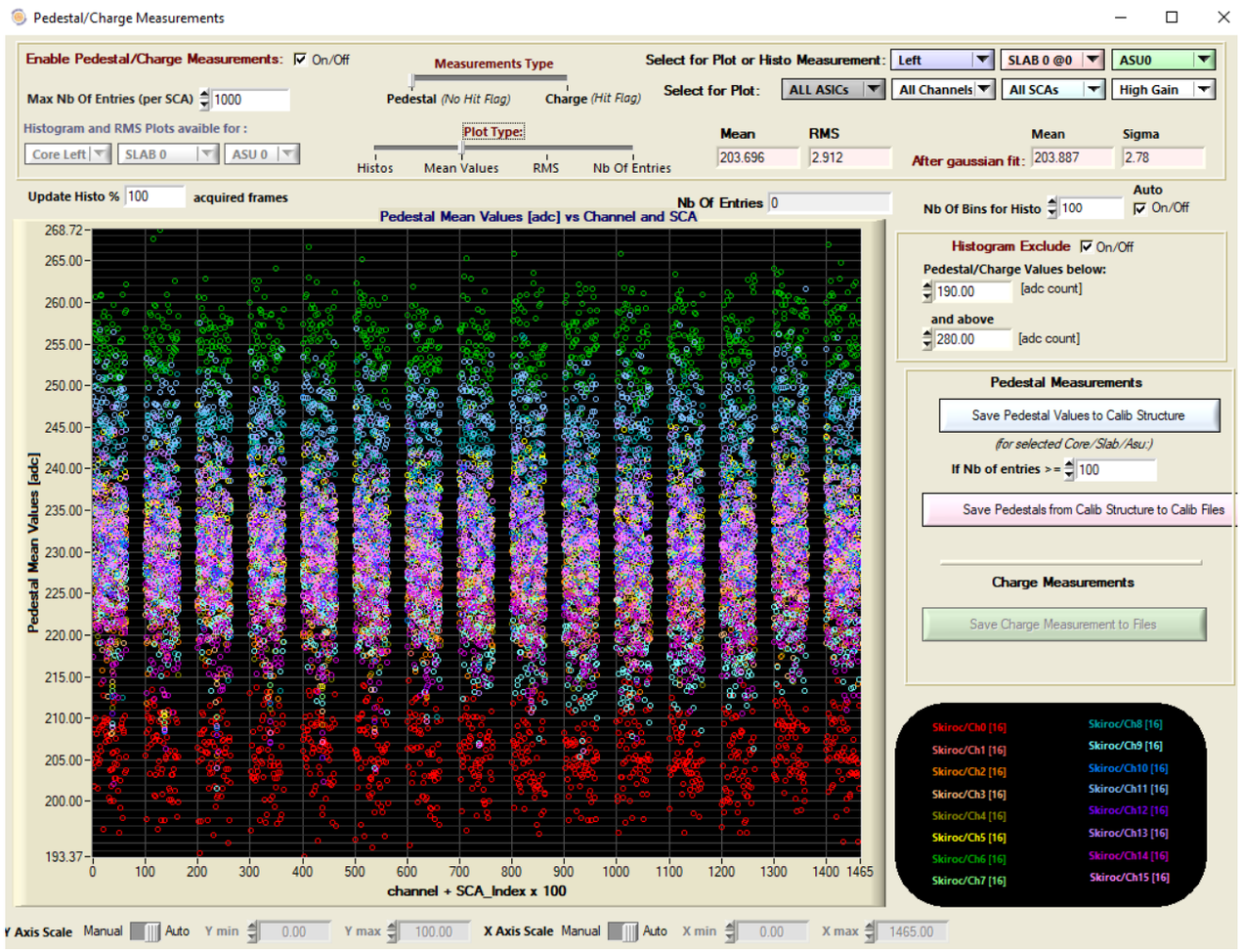
New online monitoring tools

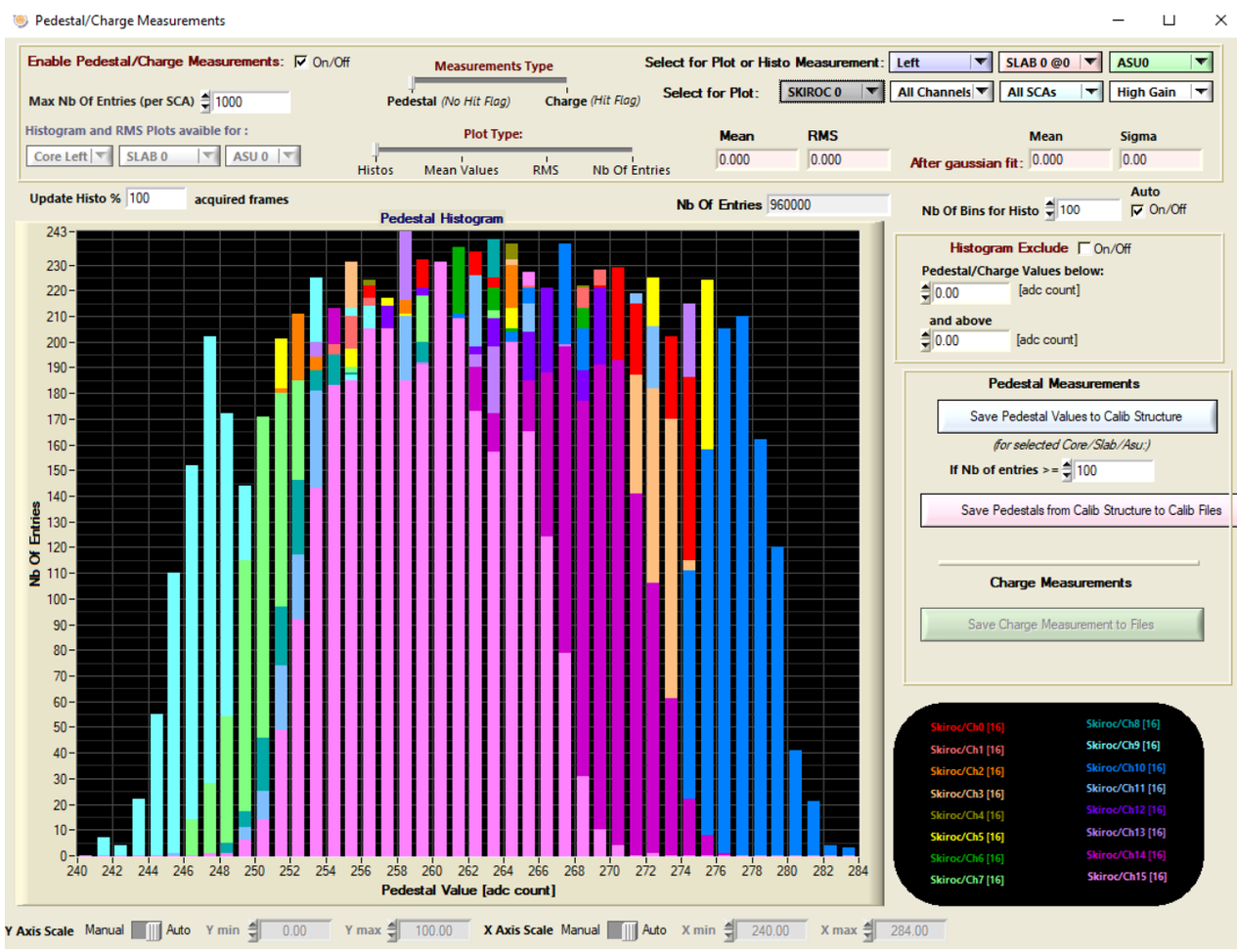
Online 3D Mapping for Hits and Charge + profile along layers



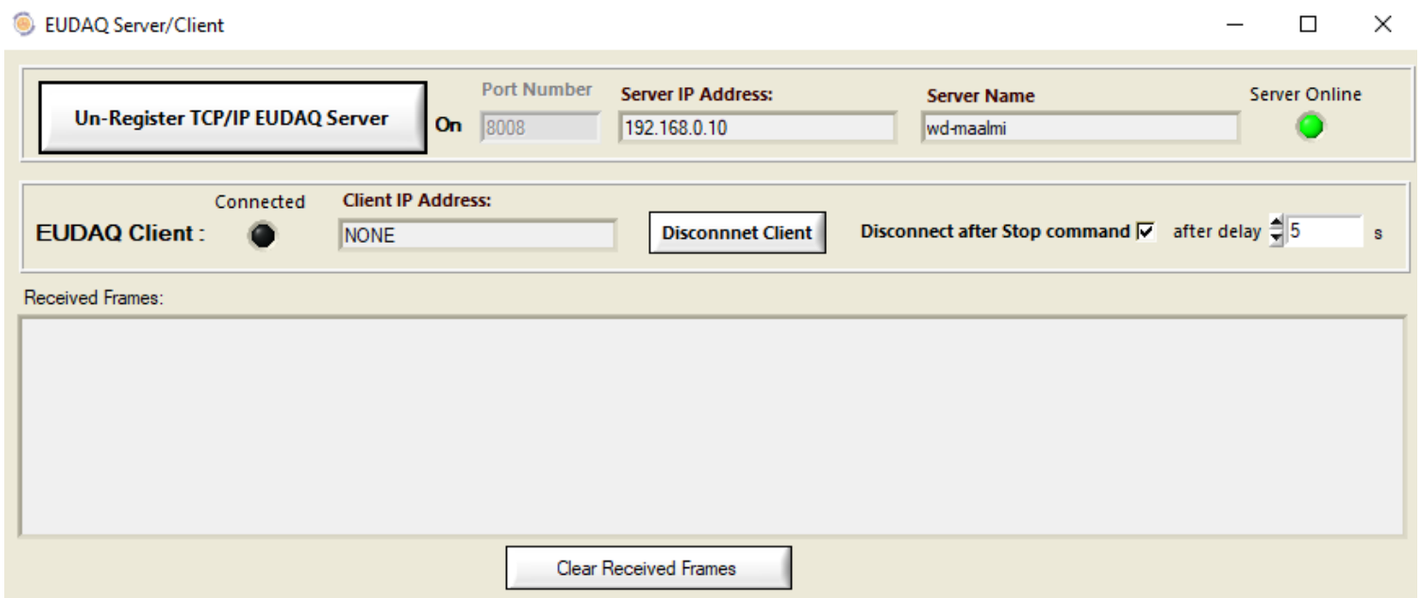
Other Measurements

- **Pedestal** Measurements and Histo and **Pedestal Correction**
- **Charge** Measurement and Histogramming
- **MIP Gain correction** (reading MIP gain files)

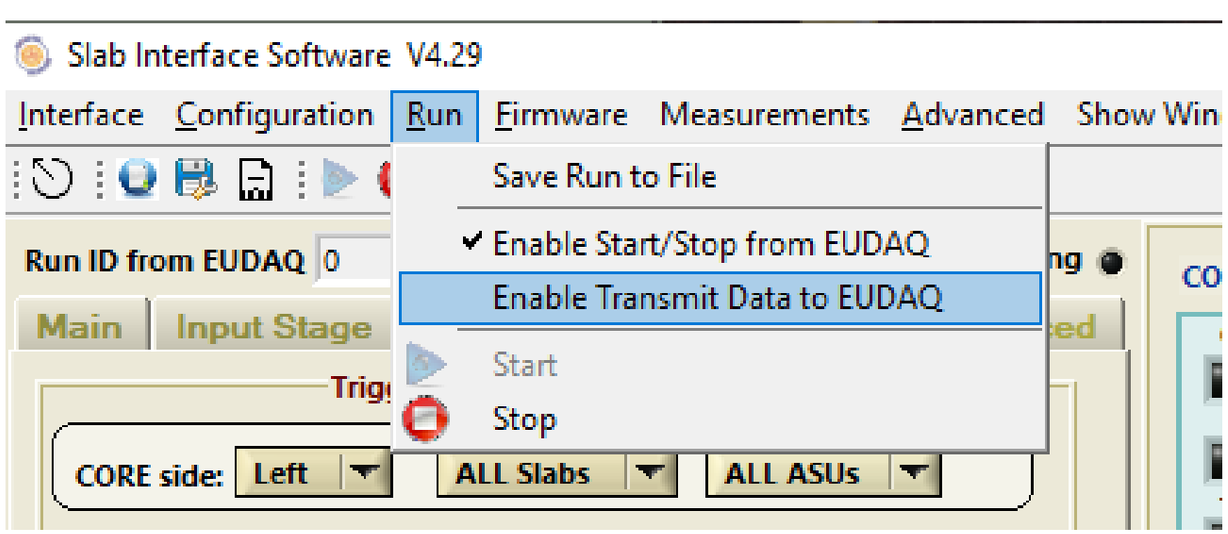




EUDAQ Interface



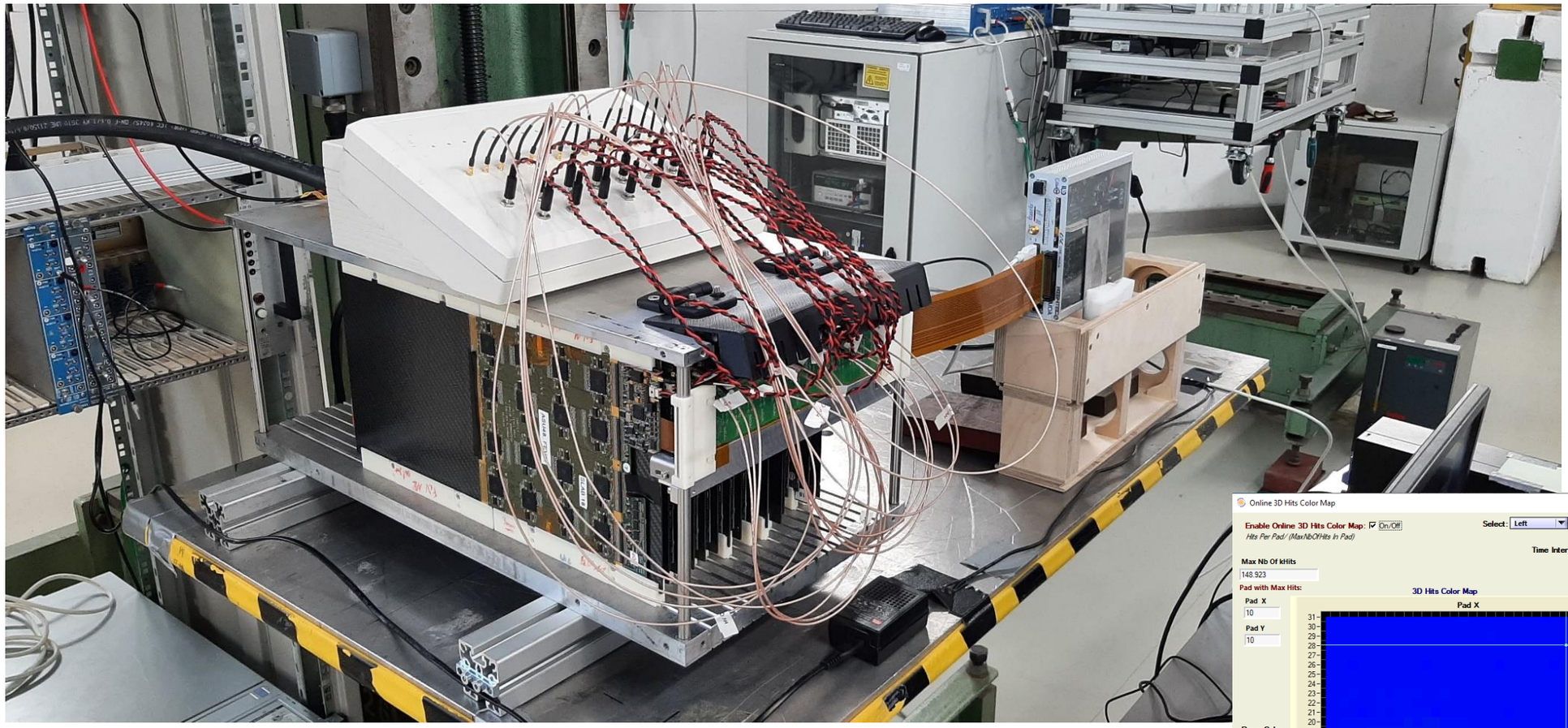
- **Added TCP server to handle EUDAQ TCP client**

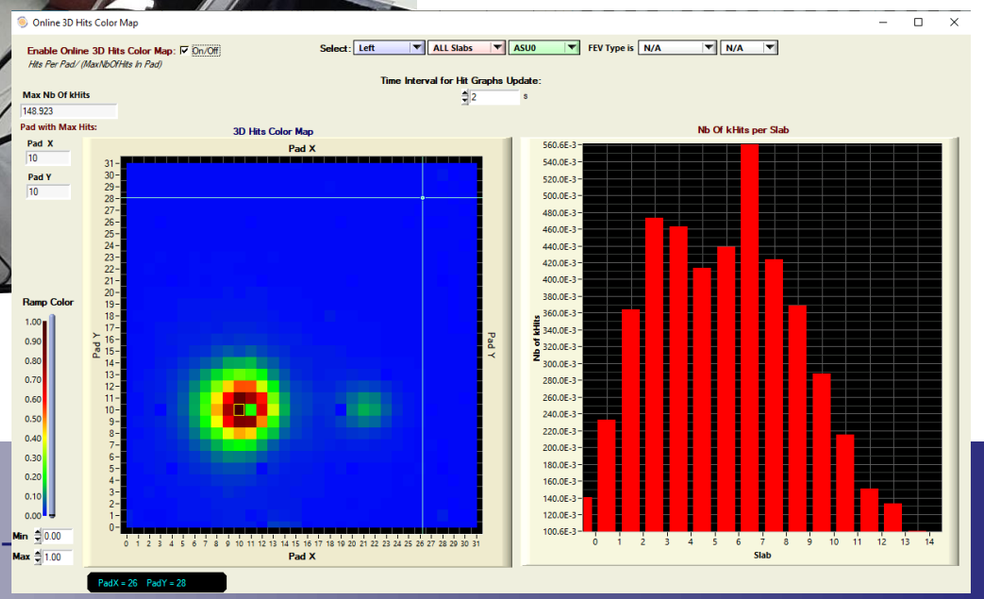


- Possibility to **START/STOP** with a specific run number from EUDAQ
- Possibility to **stream Data** to EUDAQ with/out saving Data to disk locally.
- **To be done**: add command **to LOAD SETTING FROM FILE**

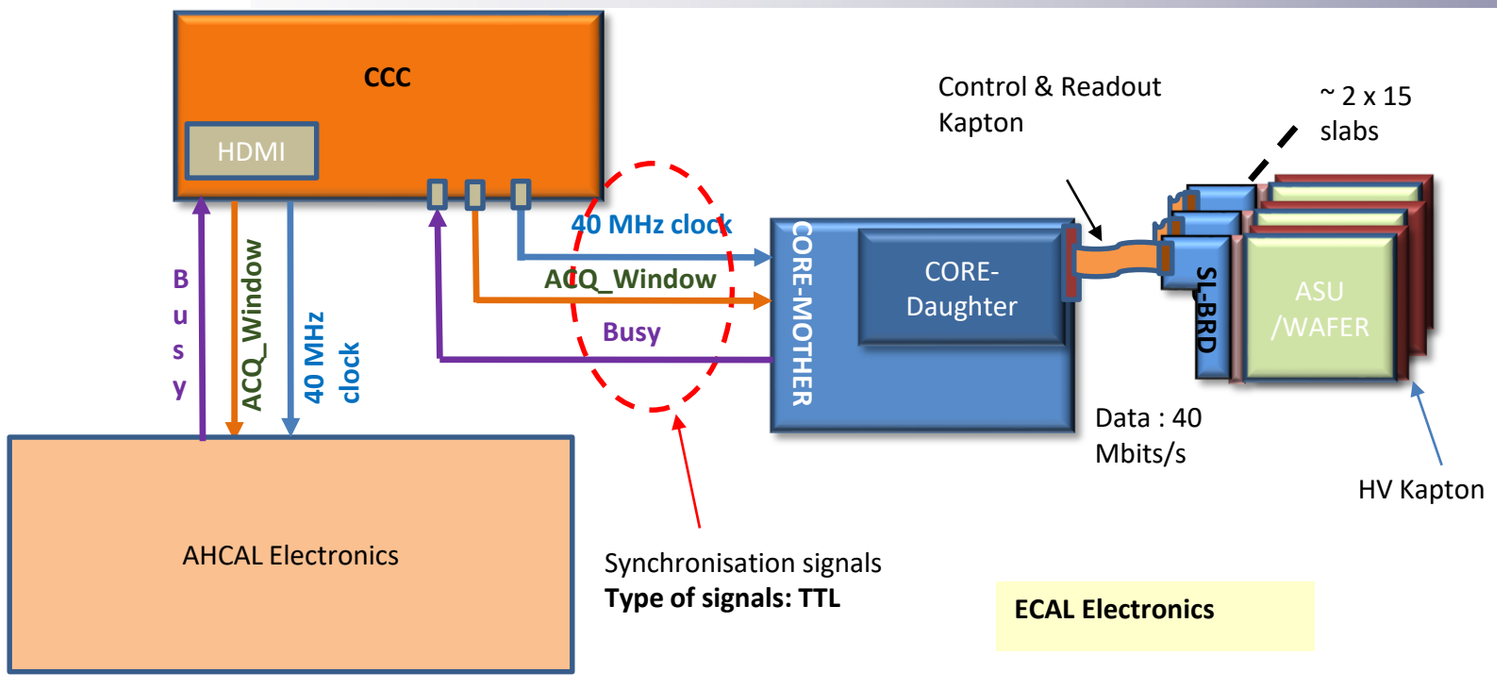
Test beam in March 2022

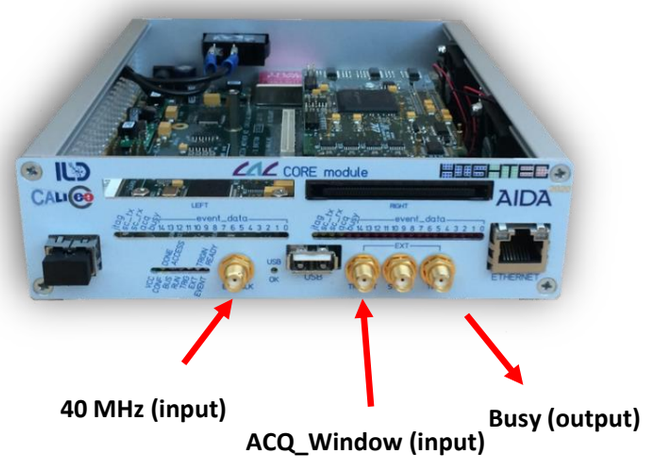
- **Successfull data taking during two weeks : ~450 GBytes of data**
- Raw binary data saving: ~8-10 times faster!
- Monitoring tools seem very helpful
- Successfull synchronous data taking with AHCAL





Synchronisation with AHCAL





- Common 40 MHz **Clock** and **AcqWindow** source.
- **Busy signal** (*corresponding to End of readout of All Skirocs AND buffers empty in SL-Board*) sent from CORE-Module to CCC
- Cycle ID and its timestamp sent with Data (gives fixed offset between systems)
- **Programmable Delay for the START_ACQ** sent to the ASICS in order to fully synchronise both systems.

New Front End Board: FEV2.0

Designed by LLR in collaboration with IJCLab
Based on Front-End ASIC : SKIROC 2A (Omega)

Improvements in the design of the FEV 2.0

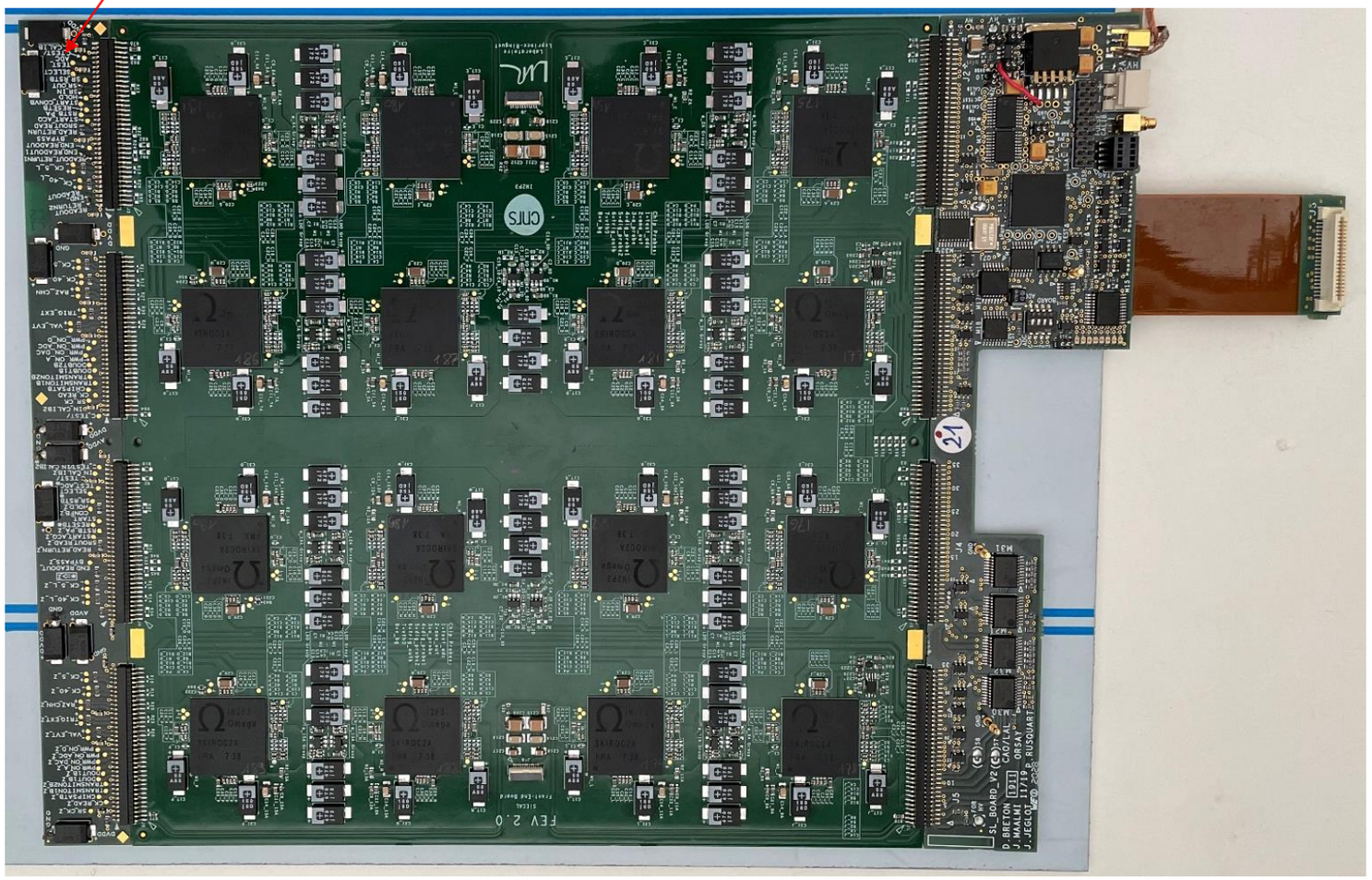
- ✓ **Improved Layout :**
  - ➢ Better shielding of AVDD and AVDD PA plans and minimisation of cross-talk between inputs and digital signals.

- ✓ **Power Pulsing Mode:** new philosophy
  - ➢ **we limit the current** through the Slab (current limiter present on the SL Board) which:
    - avoid driving high currents through the connectors and makes the current peaks local around the SKIROCs chips.
    - avoid voltage drop along the slab.
    - permits temperature uniformity
  - ➢ We add large capacitors with low ESR **for local energy storage** (around each SKIROC chip)
  - ➢ Generate **local power supply with LDO** (Low Drop Out) to remove voltage variations

- ✓ **Clean clock distribution** all over the slab :
  - for Slow Control and Readout Clocks
- ✓ Parallel configuration and readout over **2 partitions**. (< **Fev12 like**)
- ✓ Driving high voltage up to 350V for 750µm wafer (via the ASU connectors)
- ✓ Adding a filter for each wafer HV and **limit the current** in case of **wafer failure**

New Front Board FEV 2.0

SL END PLUG : for Slab extremity termination



New FEV 2.0

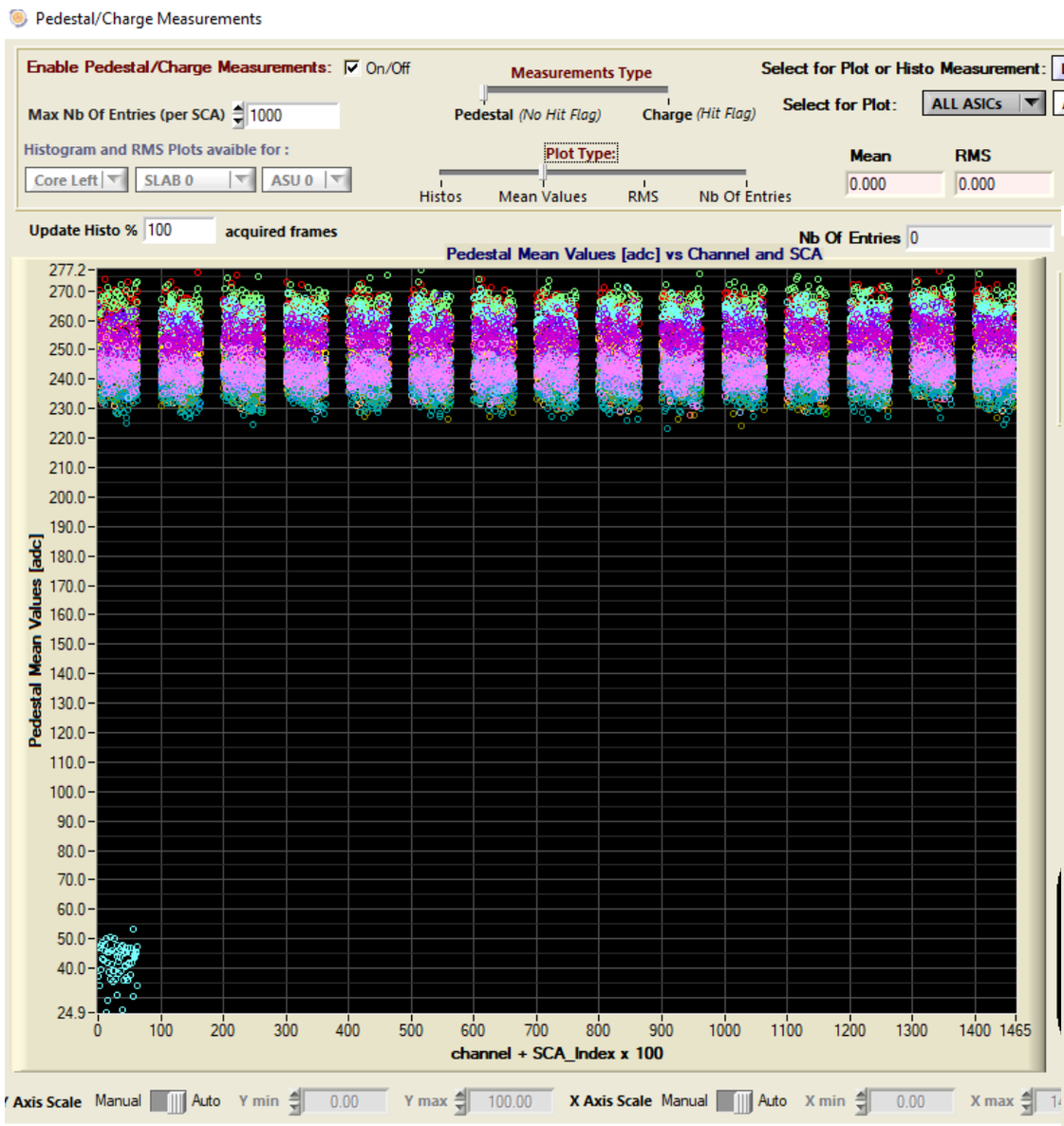
- PCBs received end of 2021 and cabled in January at IJCLab.
- Problem of missing thermal pads that made the cabling very difficult: only one board cabled for now.

➔ Minor modification to be reported on FEV 2.1

Preliminary measurements and comparison between naked FEV 2.0 (Skiroc 2A) and FEV 11 (Skiroc 2)

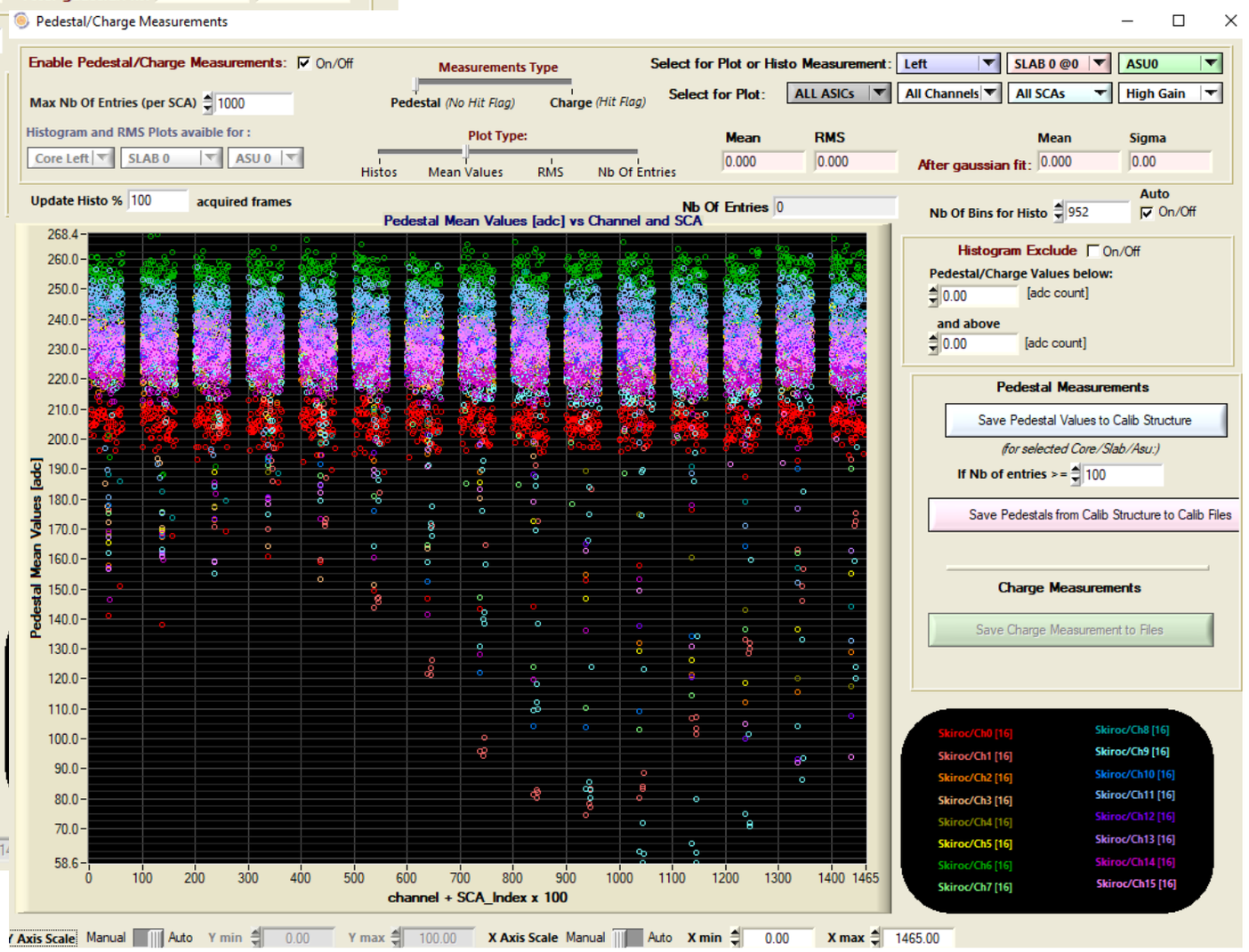
Pedestal Measurements : Mean Values

FEV 2.0



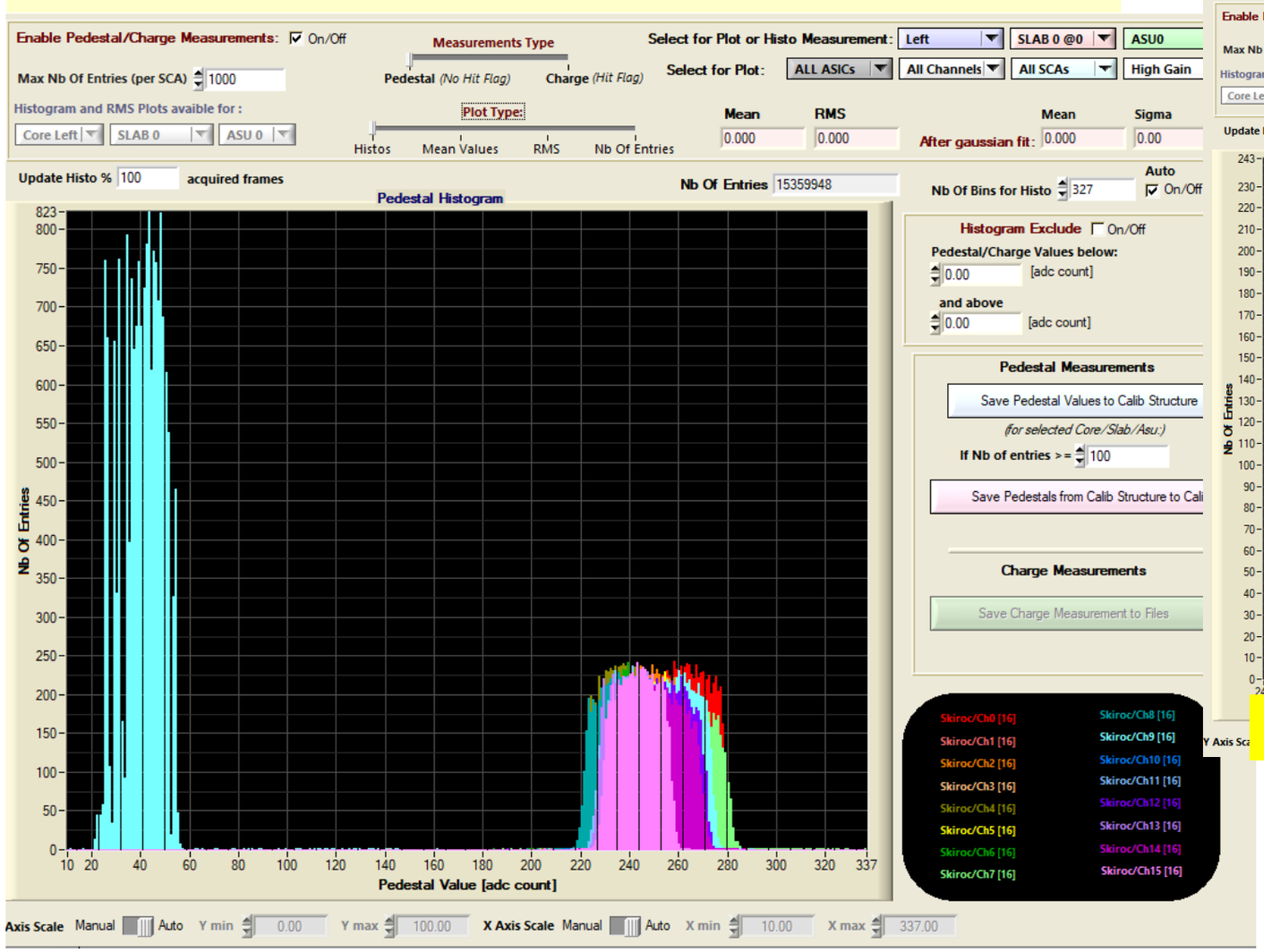
➔ One failing SCA of Skriroc 9

FEV 11

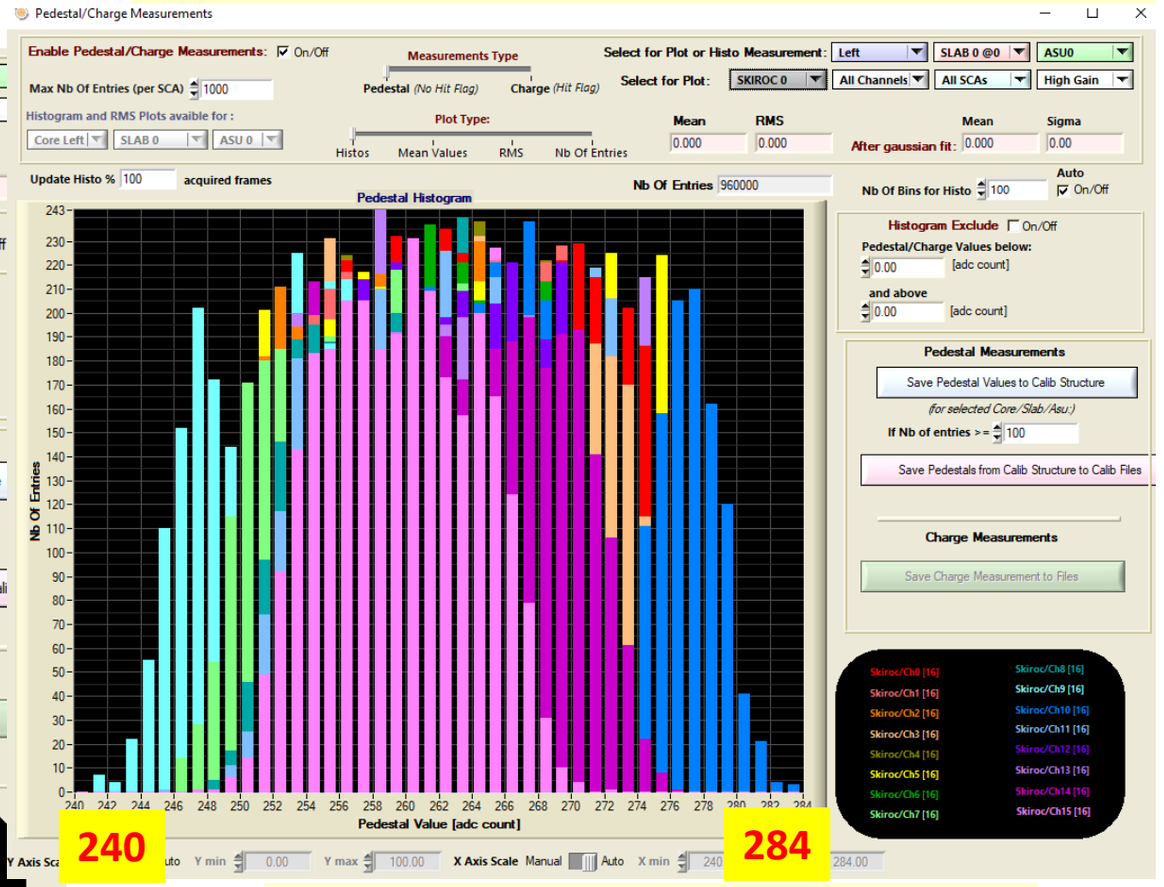


Pedestal Measurements : Histograms FEV 2.0

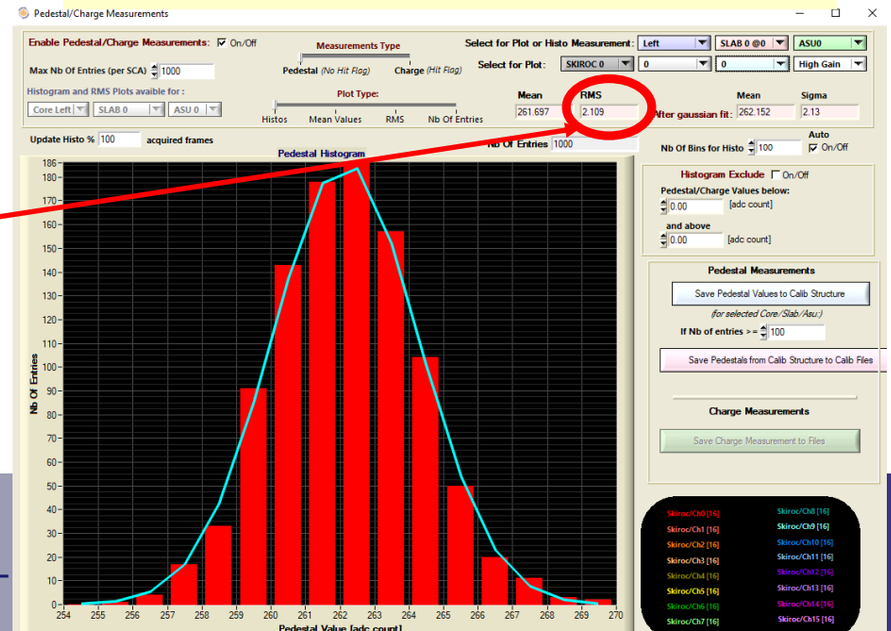
FEV 2.0: All Skirocs/All Channels/All SCAs



FEV 2.0: Skiroc 0 /All Channels/All SCAs



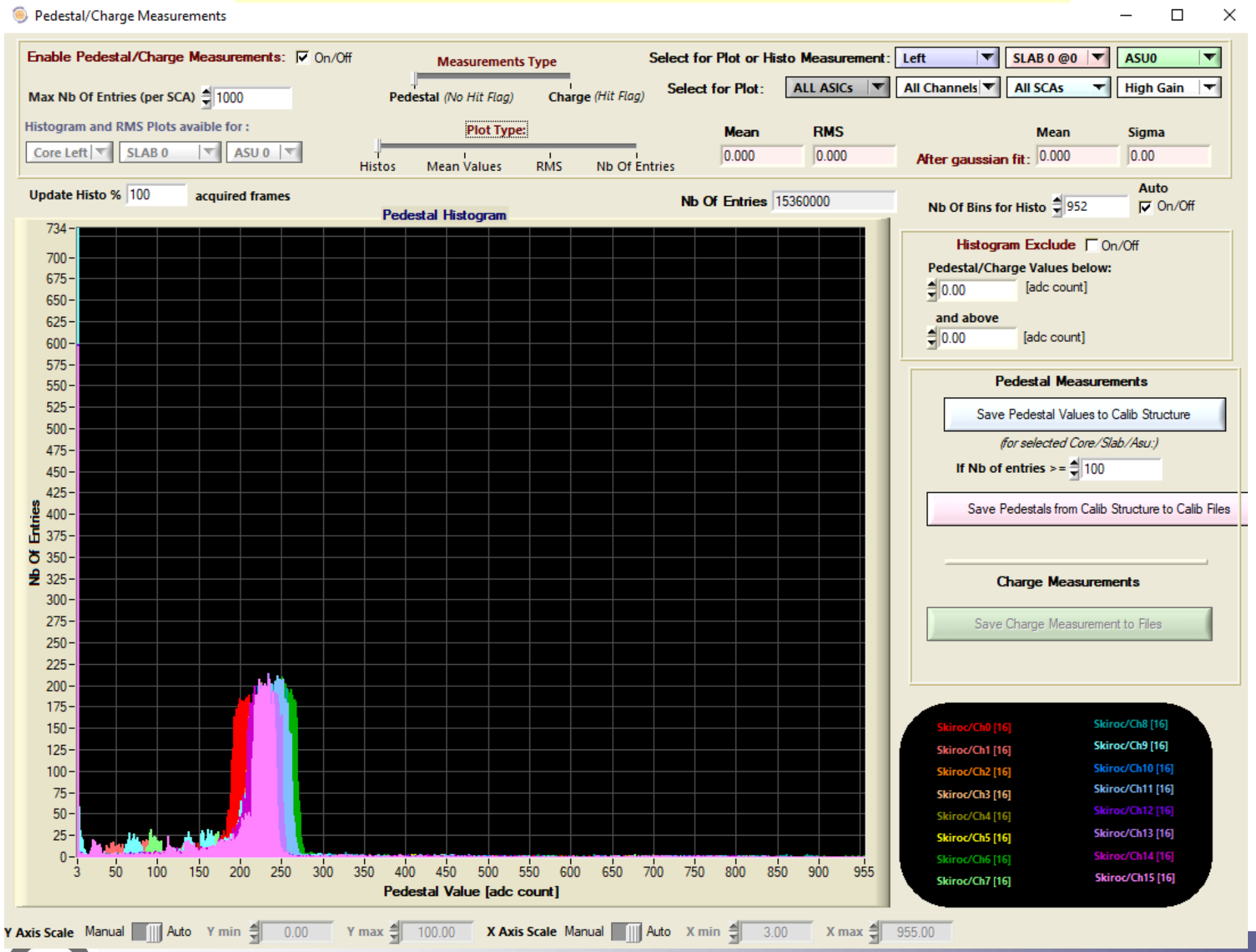
FEV 2.0: Skiroc 0 /CH 0/SCA 0



RMS : 2.1 adc count

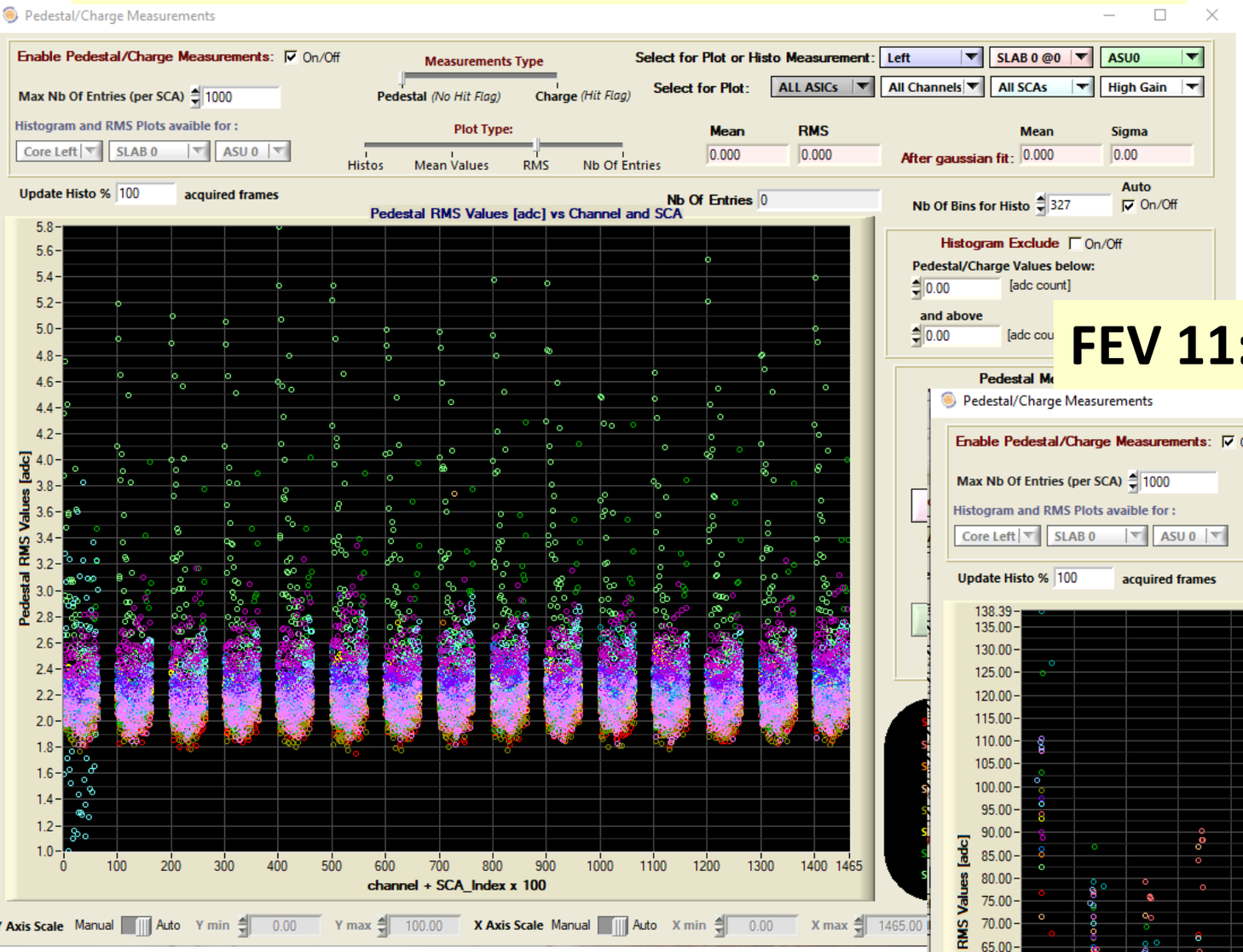
Pedestal Measurements
Histograms FEV 11

FEV 11: All Skirocs/All Channels/All SCAs

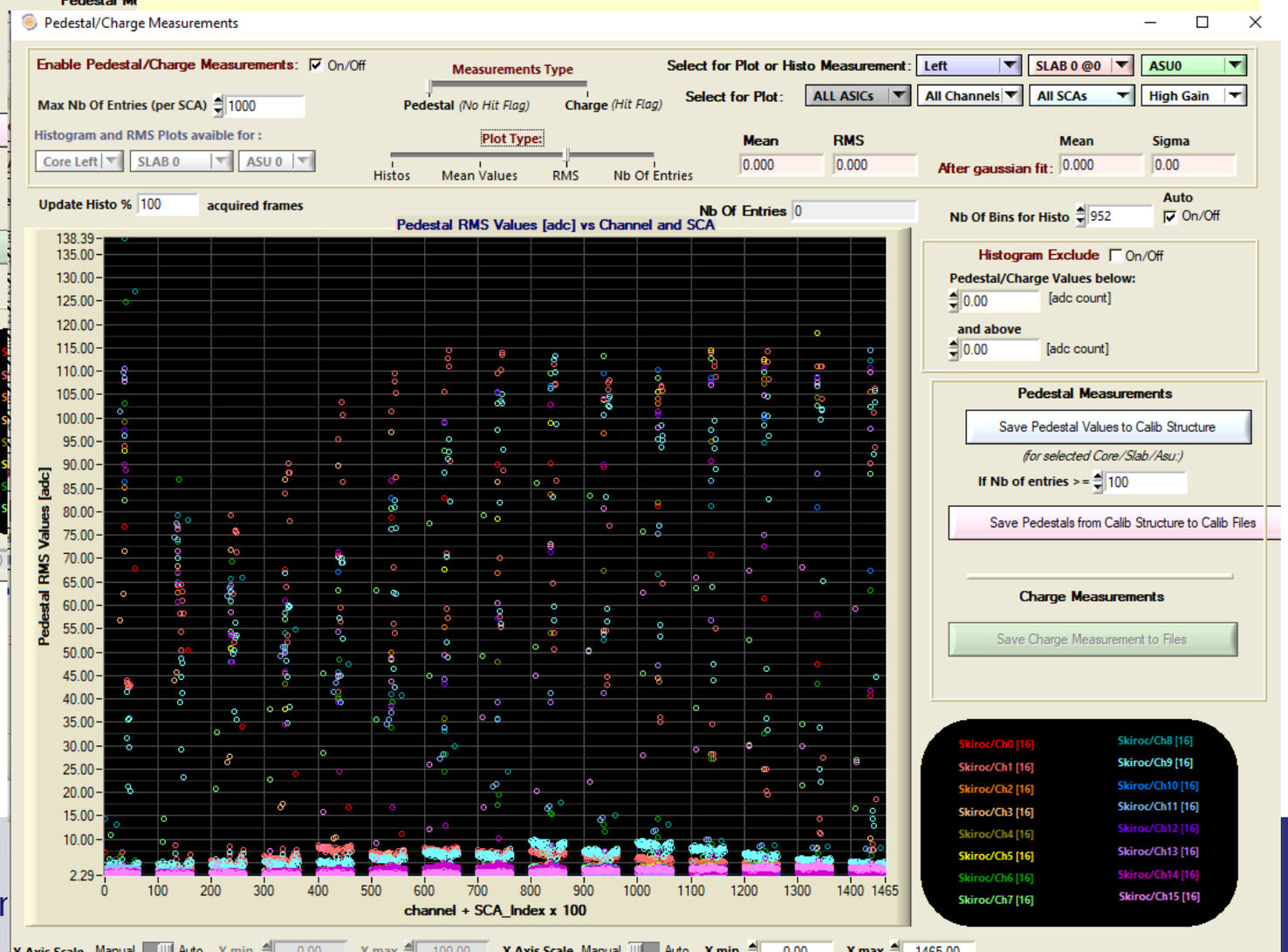


Pedestal Measurements : RMS Values (adc counts)

FEV 2.0: Mean RMS 2.2 adc count, max 5.8



FEV 11: min RMS 2.2 adc count, max 138!



Pedestal Measurements : FEV11

➔ Exclude « false » measurements

FEV 11: Mean RMS ~2/3 adc count , max value: 22

Zoom on RMS measurements for FEV 11, SKIROC 0

Pedestal/Charge Measurements

Enable Pedestal/Charge Measurements: On/Off

Max Nb Of Entries (per SCA) 1000

Histogram and RMS Plots avaible for : Core Left | SLAB 0 | ASU 0

Measurements Type: Pedestal (No Hit Flag) / Charge (Hit Flag)

Plot Type: Histos / Mean Values / RMS / Nb Of Entries

Select for Plot or Histo Measurement: Left | SLAB 0 @0 | ASU0

Select for Plot: SKIROC 0 | All Channels | All SCAs | High Gain

	Mean	RMS
	0.000	0.000

After gaussian fit: Mean 0.000, Sigma 0.00

Update Histo % 100 acquired frames

Nb Of Entries 0

Nb Of Bins for Histo 952 Auto On/Off

Pedestal RMS Values [adc] vs Channel and SCA

Channel 37 and ??

Pedestal RMS Values [adc]: 90.30, 85.00, 80.00, 75.00, 70.00, 65.00, 60.00, 55.00, 50.00, 45.00, 40.00, 35.00, 30.00, 25.00, 20.00, 15.00, 10.00, 5.00, 2.44

channel + SCA_Index x 100: 0, 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1465

Histogram Exclude On/Off

Pedestal/Charge Values below: 0.00 [adc count]

and above 0.00 [adc count]

Pedestal Measurements

Save Pedestal Values to Calib Structure

(for selected Core/Slab/Asu:)

If Nb of entries >= 100

Save Pedestals from Calib Structure to Calib Files

Charge Measurements

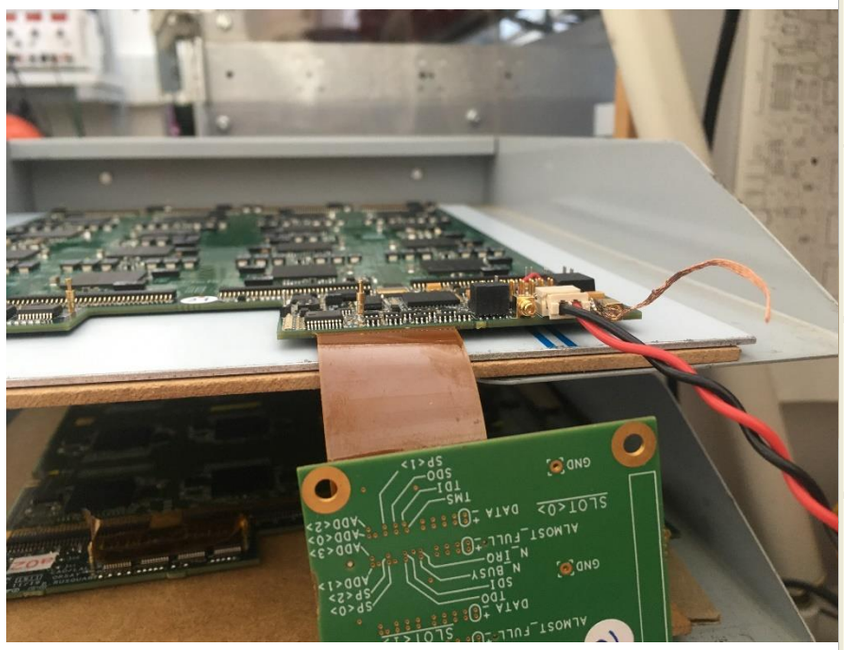
Save Charge Measurement to Files

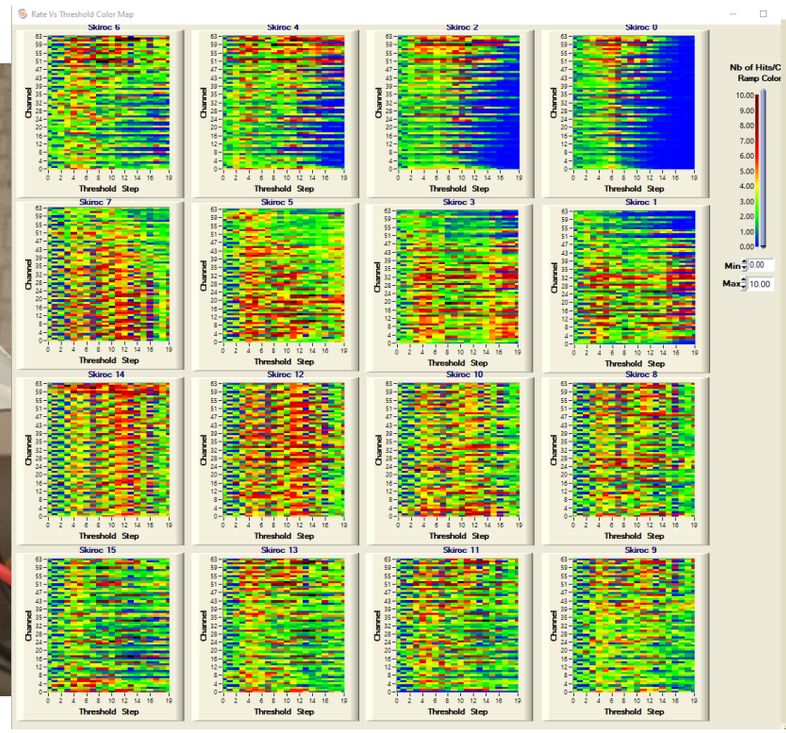
Skiroc/Ch0 [16] Skiroc/Ch1 [16] Skiroc/Ch2 [16] Skiroc/Ch3 [16] Skiroc/Ch4 [16] Skiroc/Ch5 [16] Skiroc/Ch6 [16] Skiroc/Ch7 [16]

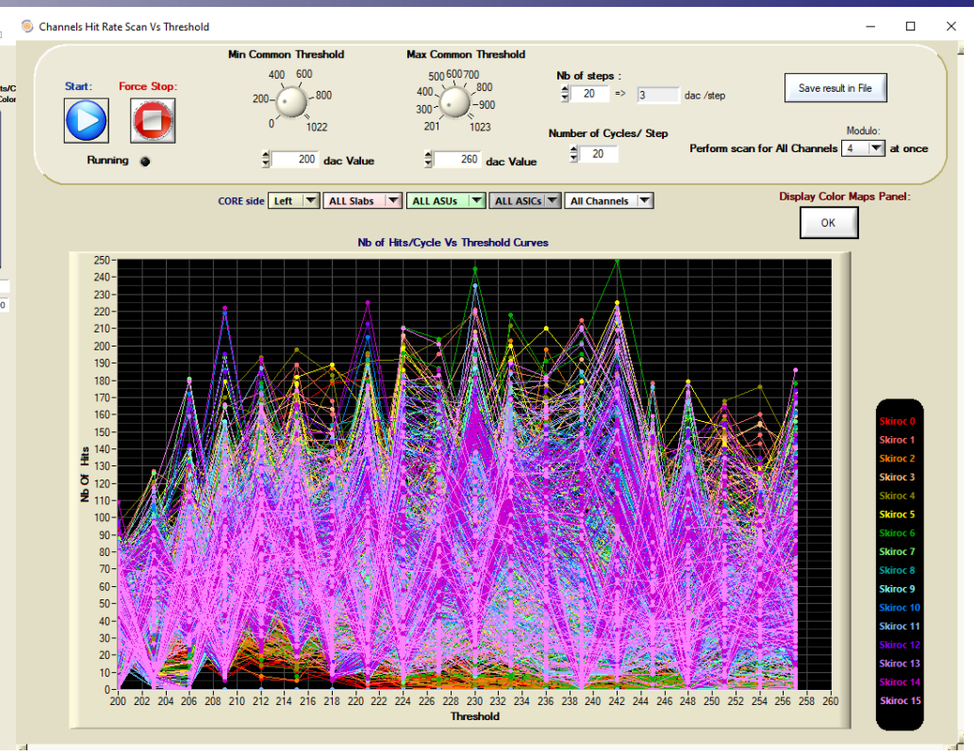
Skiroc/Ch8 [16] Skiroc/Ch9 [16] Skiroc/Ch10 [16] Skiroc/Ch11 [16] Skiroc/Ch12 [16] Skiroc/Ch13 [16] Skiroc/Ch14 [16] Skiroc/Ch15 [16]

Y Axis Scale Manual Auto Y min 0.00 Y max 100.00 X Axis Scale Manual Auto X min 0.00 X max 1465.00

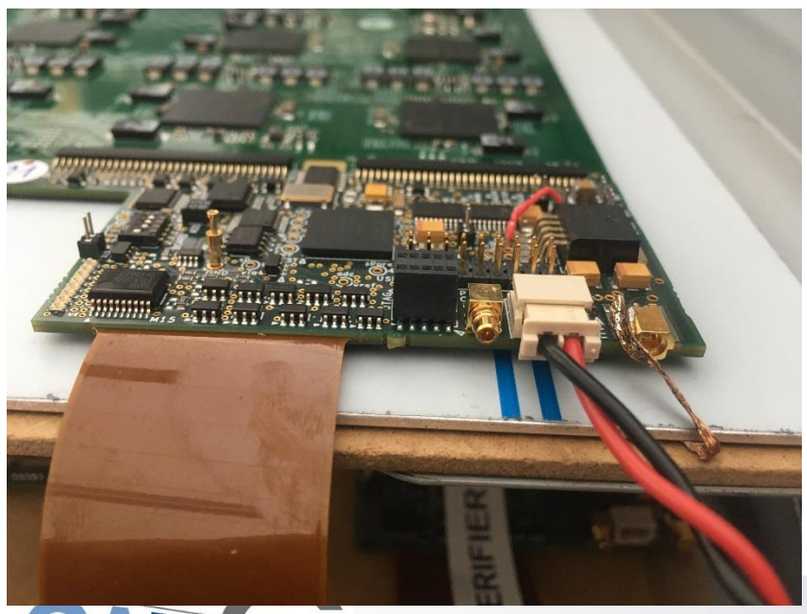
Threshold Scans and effect of shielding

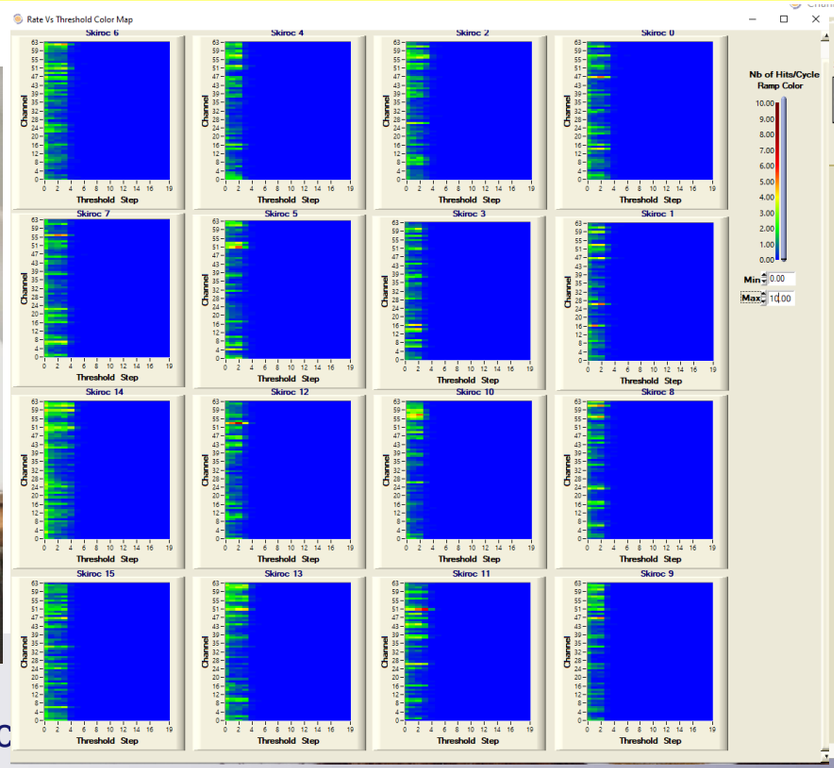


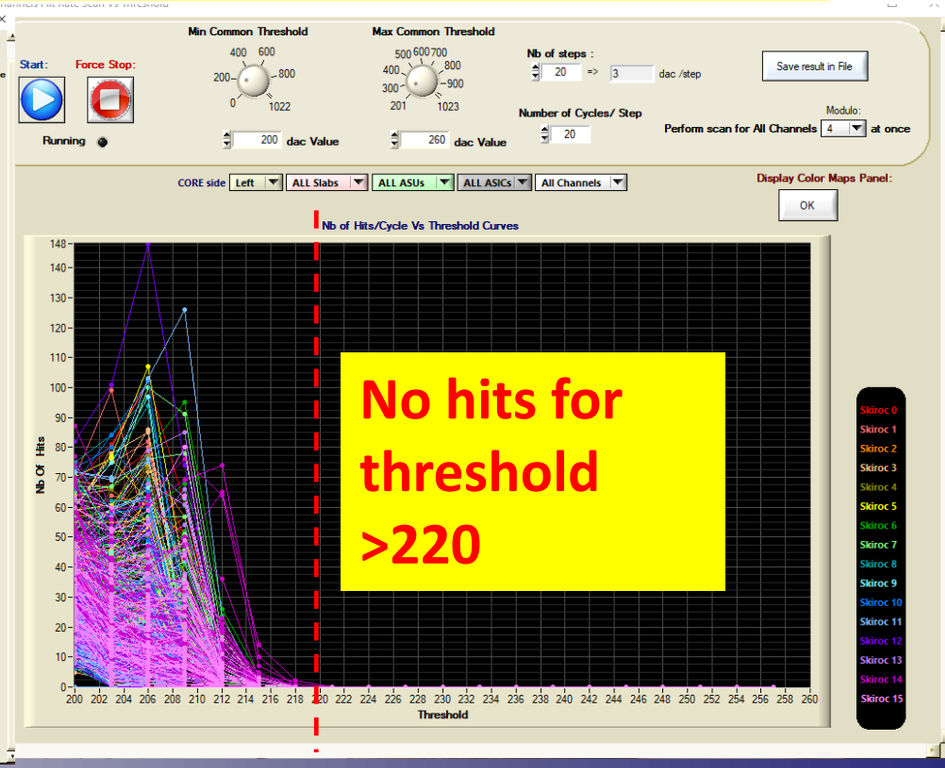




Threshold scan between **200** and **250** with 20 steps (**3 adc count/ step**)

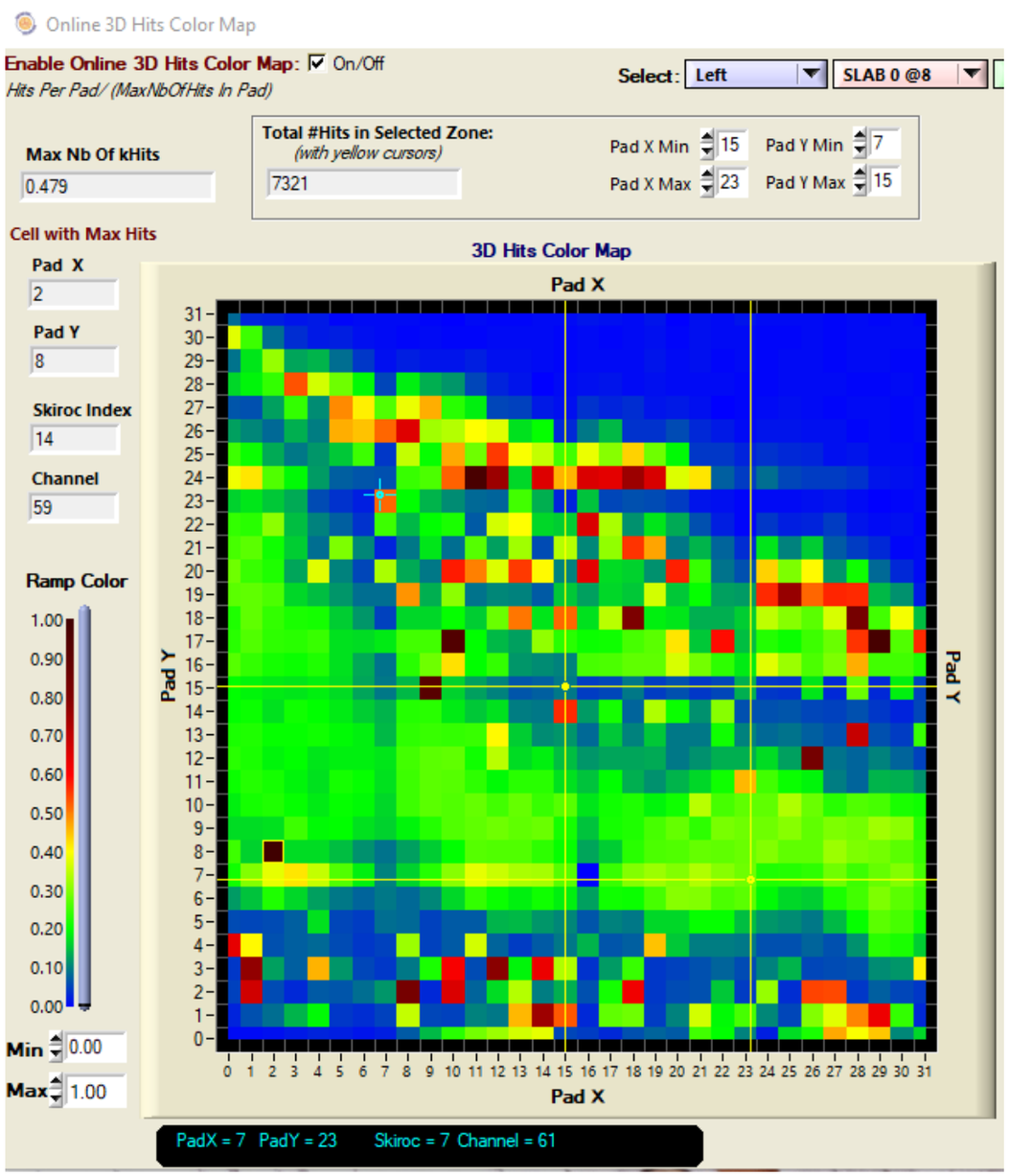




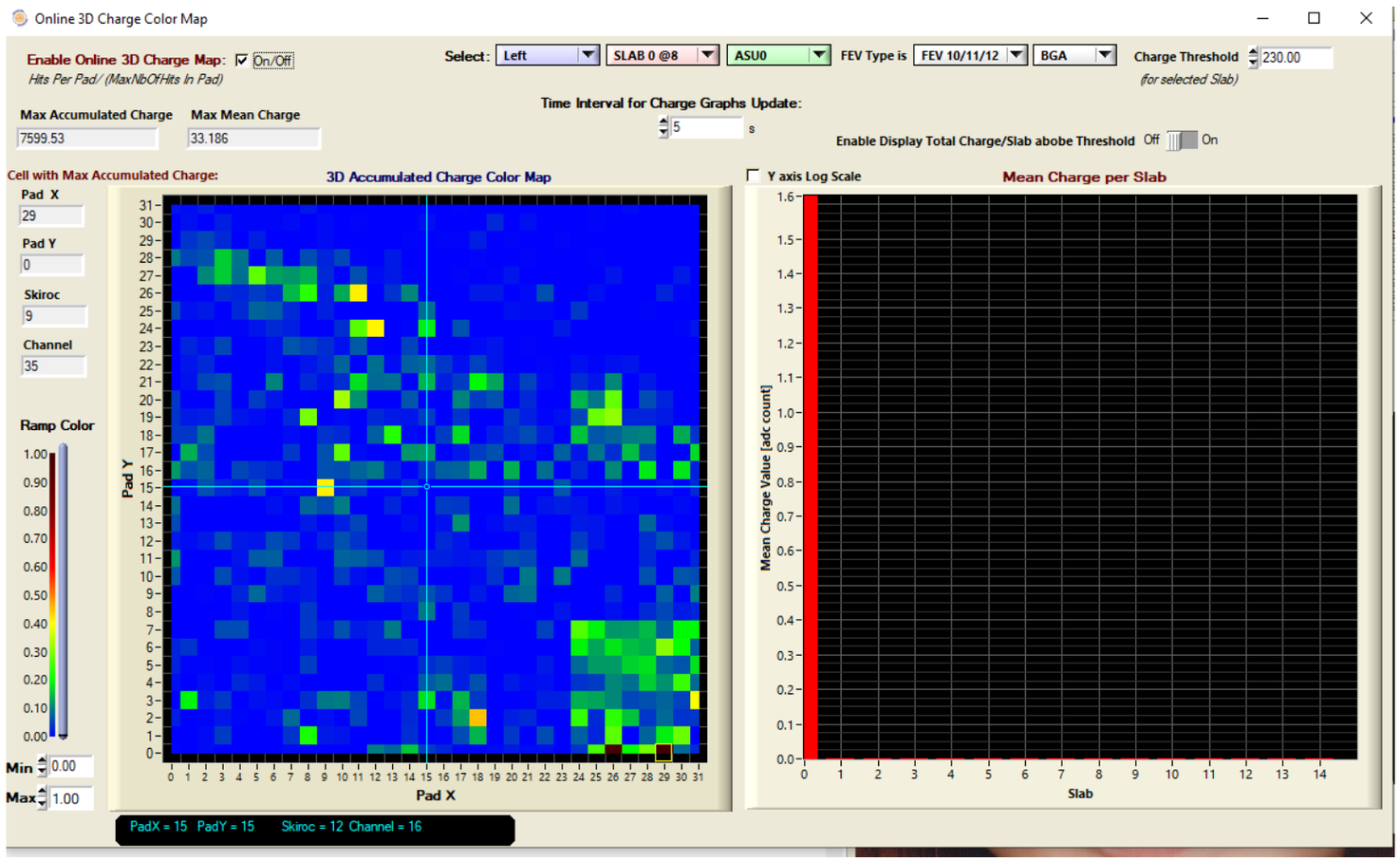


Hit map and Charge Map without shielding

Hit Color Map

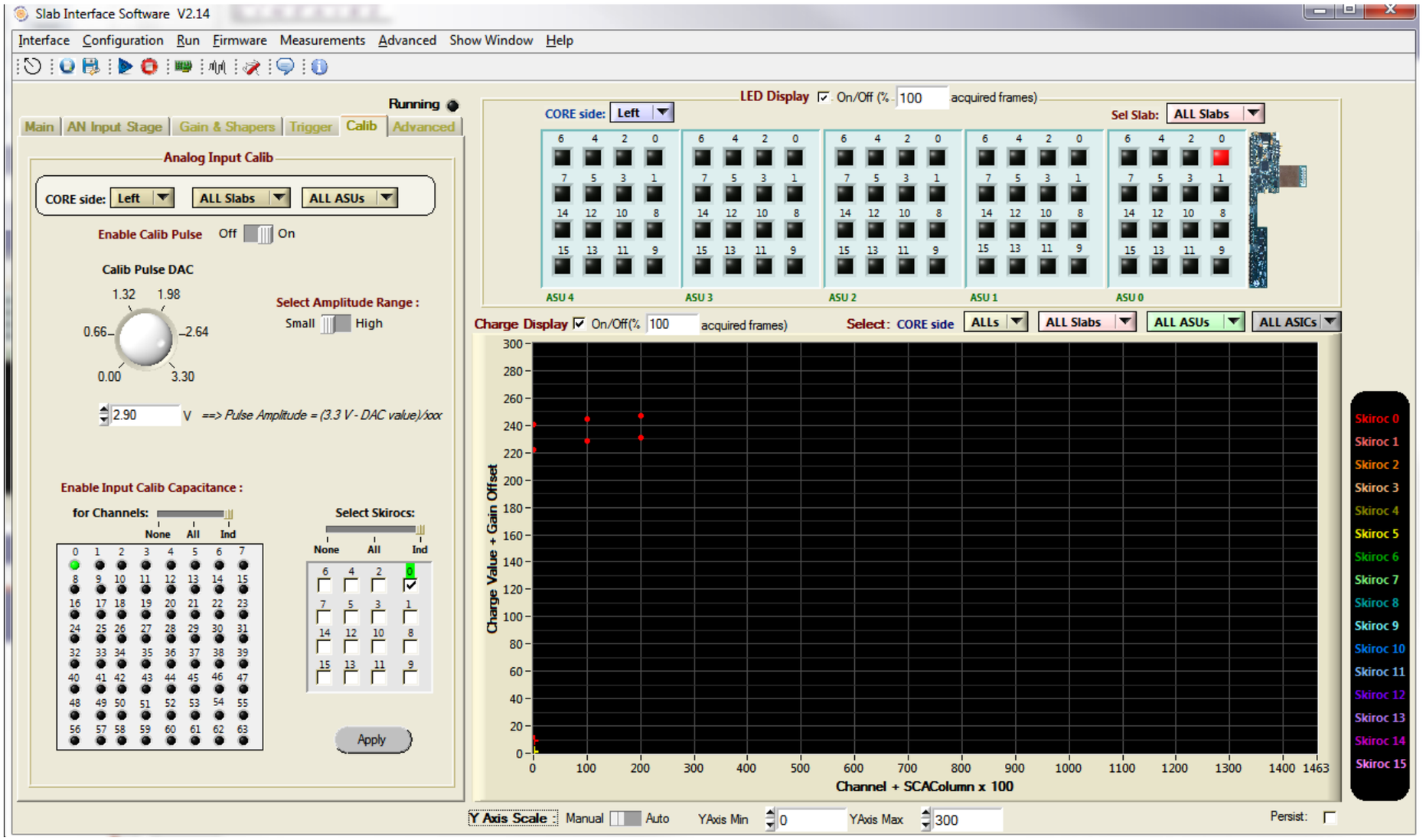


Charge Color Map



➔ Triggering Noise but no Charge

Charge Injection: very small signals

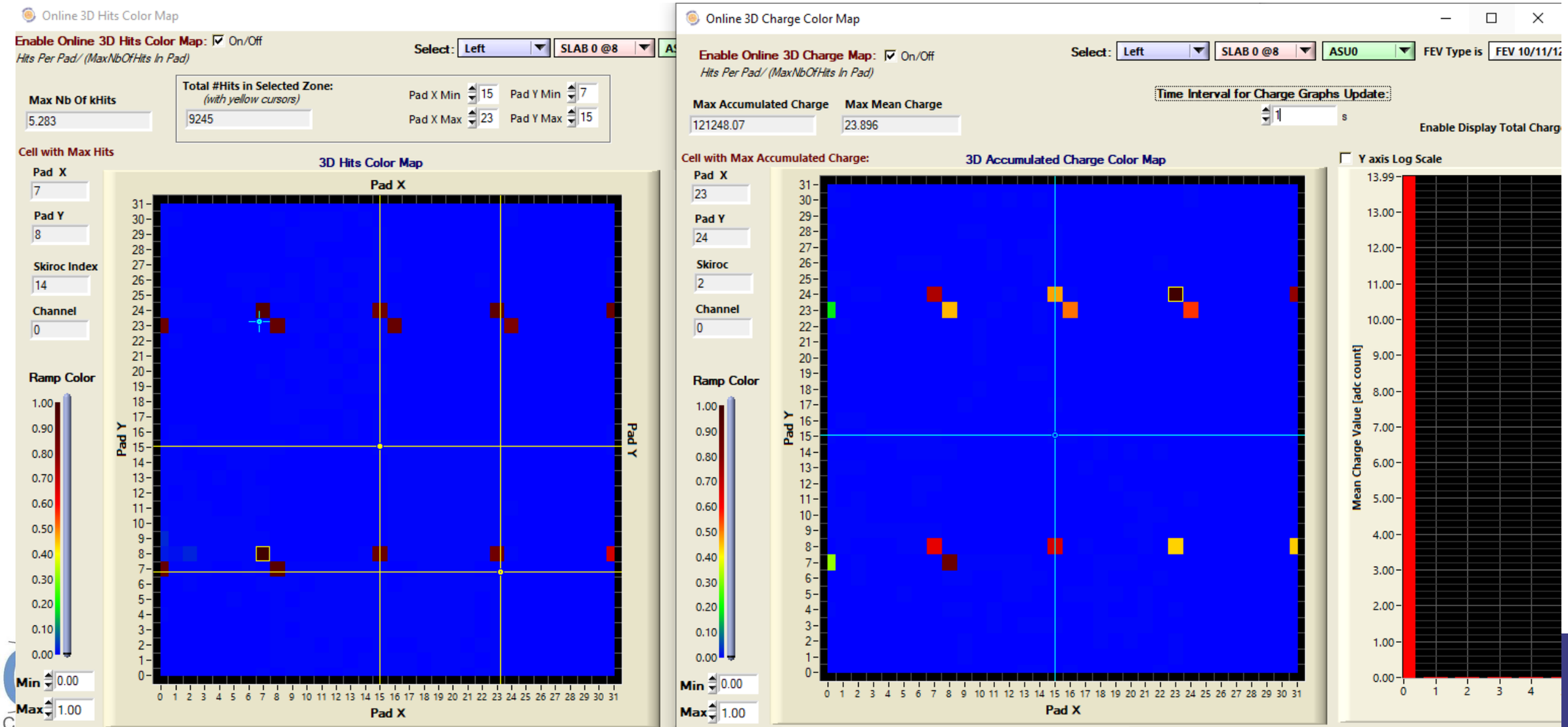


- **We look the minimum triggerable charge**

Hit and Charge 3D plots

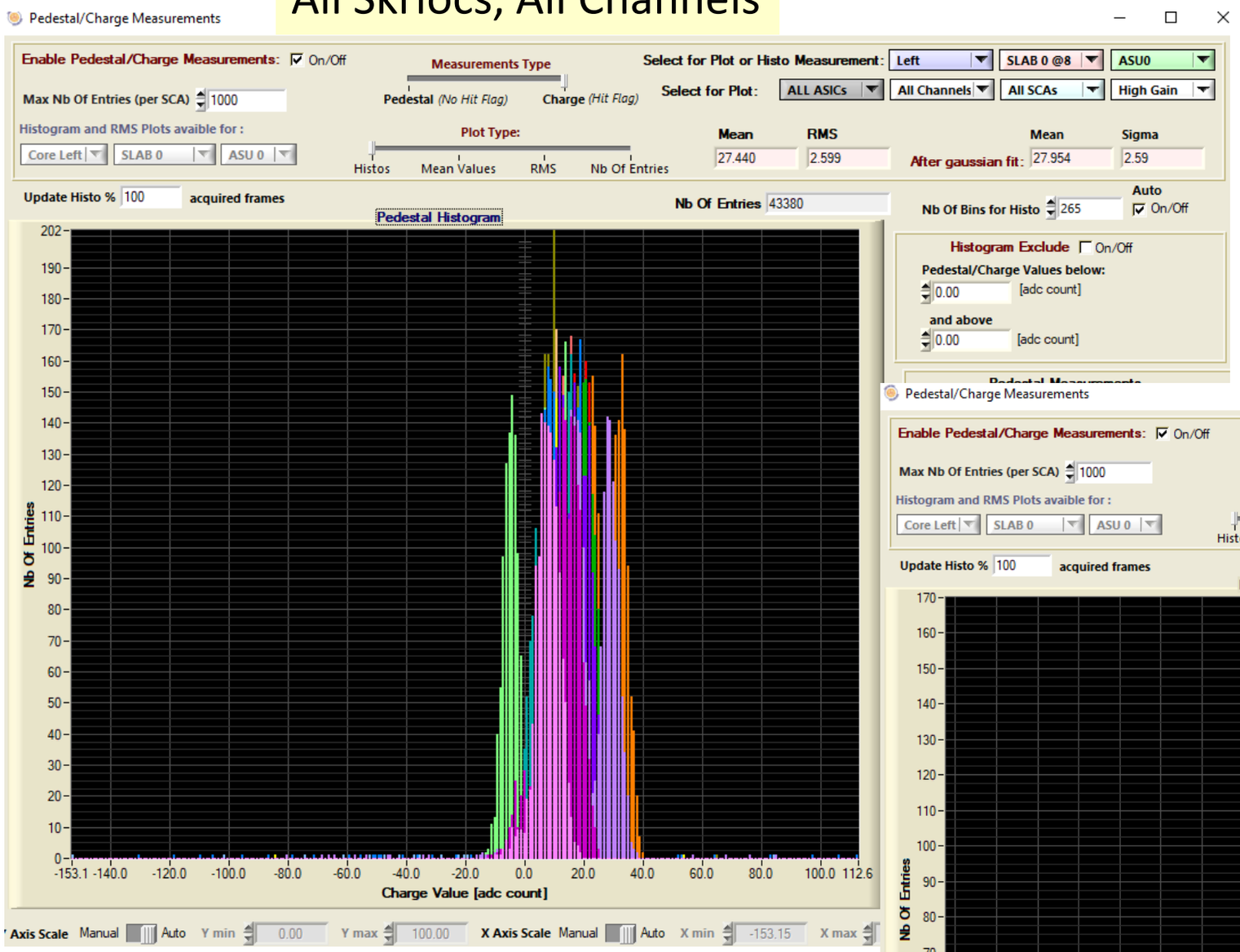
Settings :

- Pulse Calib set to 3.2 V (in the calib Panel ➔ pulse amplitude ~ few mV)
  ➔ small Mean value : ~23 adc count.
- Charge injected on **Channel 0 of all SKIROCs but ALL CHANNELS ON**
- Threshold set to : 224
- Channel Threshold : 15

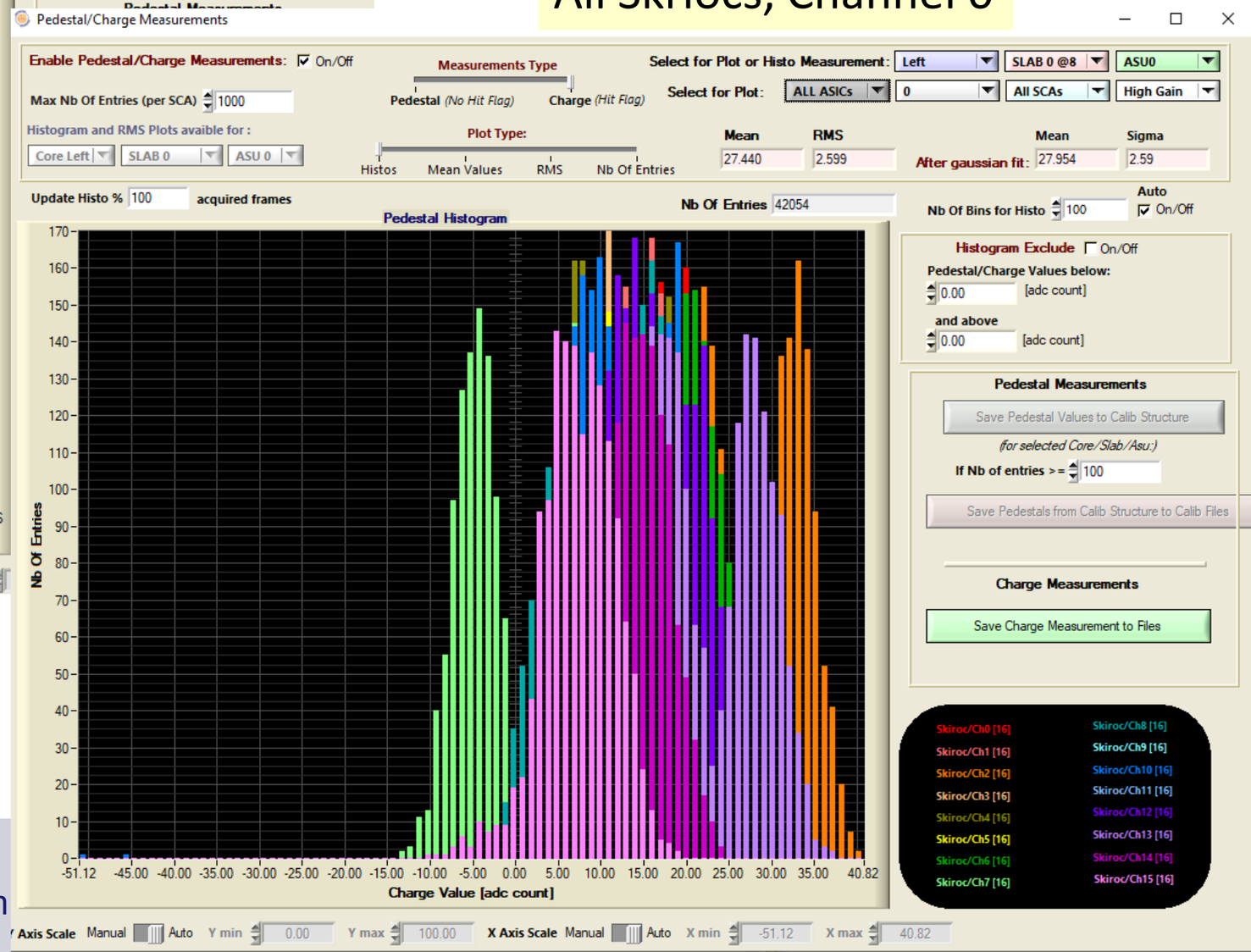


Charge Histograms with Pedestal correction

All Skriocs, All Channels



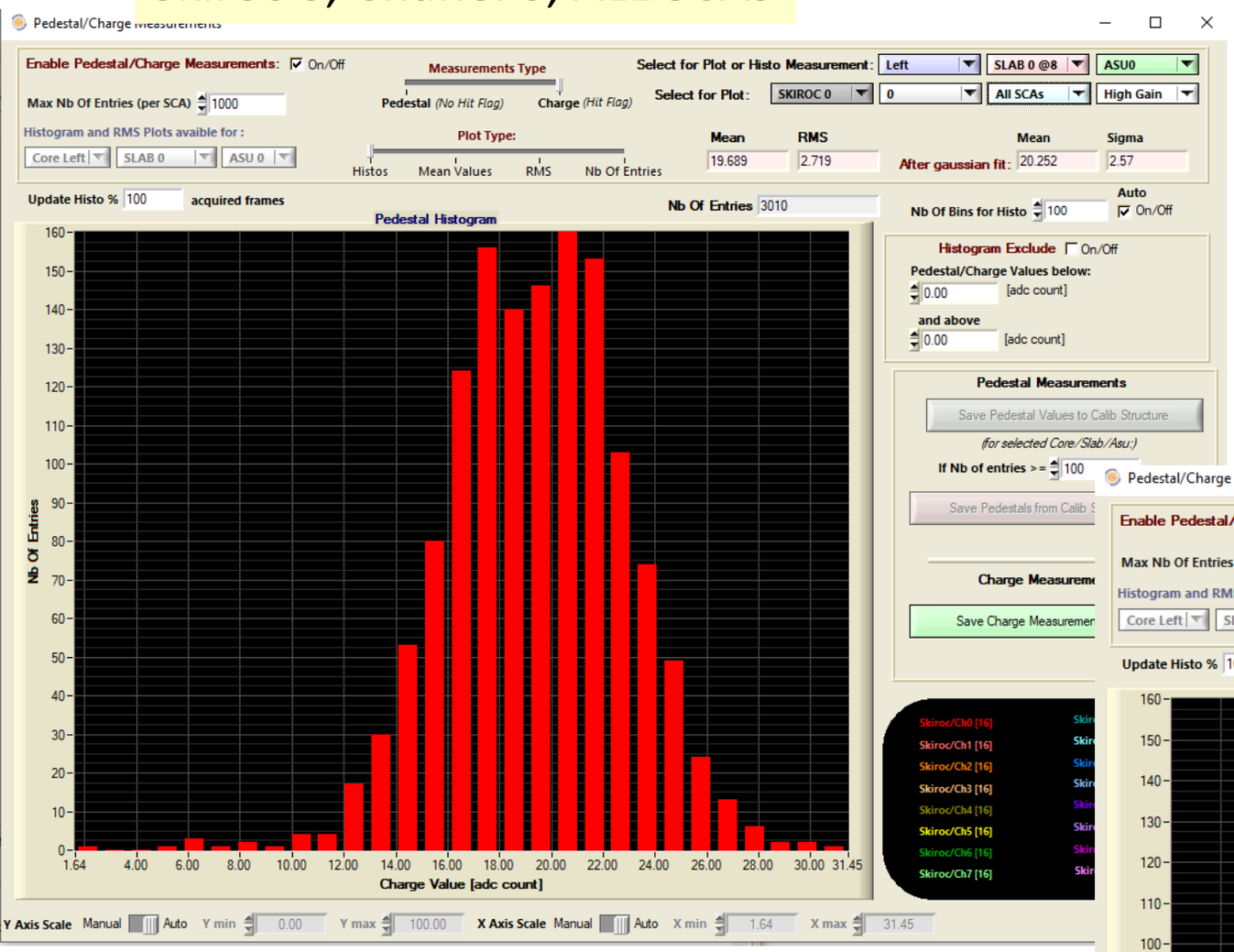
All Skriocs, Channel 0



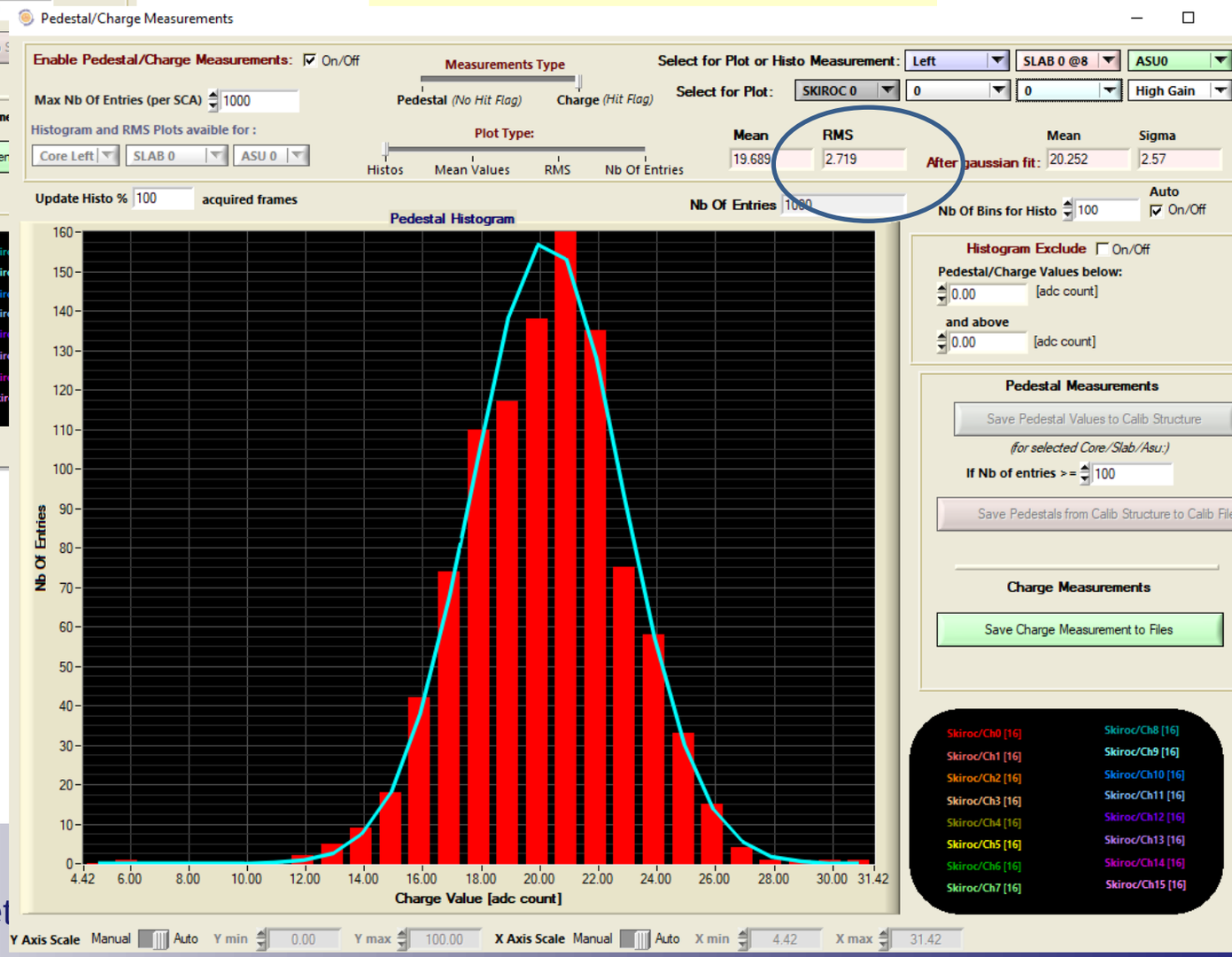
Can we use these type of measurements for a first level **Gain correction**??

Charge Measurement: Zoom on one Skiroc

Skiroc 0, Chanel 0, ALL SCAs



Skiroc 0, Chanel 0, SCA 0



Future plans and Conclusion

- **Successfull data taking** with **15-layer prototype** (Nov 21, March 22)
  - **Synchronized** beam with **AHCAL**
  - Interface with **EUDAQ**
  - Improvement of **Online monitoring tools**

- **Next plans for Current SiW Ecal prototype:**
  - Extend the prototype to **more than 15 layers (mid term)**
    ➔ using **existing boards**: two core Kaptons and one Core Module.
  - Improve **ground shielding**
  - Try to understand inhomegeneity of gain in most ASUs
  - Work on **Thresholds** and **Gain** adjustment using **charge injection**?
  - Add other automatic measurements in the software: **hold scan?**
  - Problem with **components shortage**

➔ **we can not currently produce any boards …**

- **Next test beam at CERN : JUNE 2022**
  - concentrate on good boards
  - 5 ? FEV13 + COBs and FEV11/12 Slabs
- **New Front End Board FEV 2.0**
  - **Power Pulsing**
  - Test a **long Slab**
  - **TDC** Measurements