Future ROCs for CALICE

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Valencia

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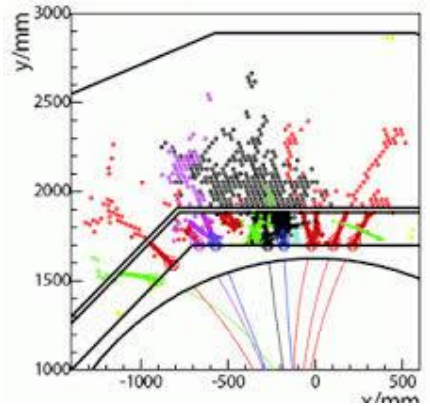
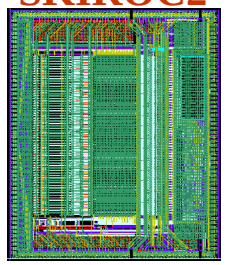
Organization for Micro-Electronics desiGn and Applications

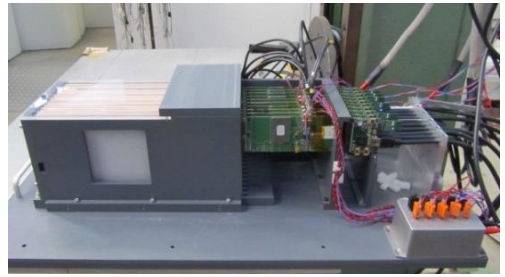
CALICE technological prototypes

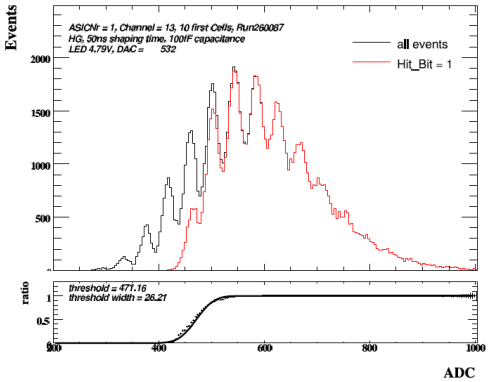
- R&D on imaging calorimetry
  - Particle Flow Algorithms [
  - Electronics crucial (low noise, low power, fully integrated)
  - Several innovative features (power pulsing, SiPM…)
  - Validation of technological prototypes
  - Common R/O features
  - Worldwide collaboration



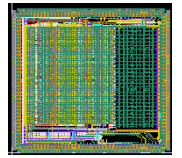
SKIROC2



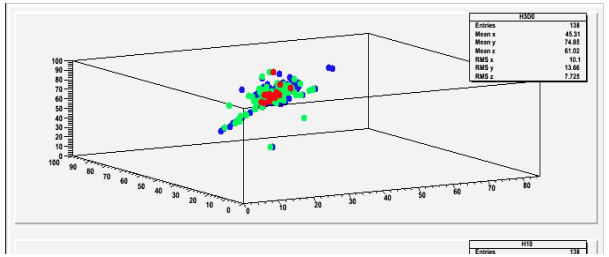




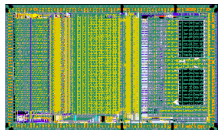
SPIROC2



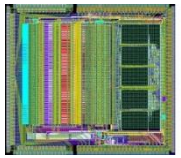
AIDA



HARDROC2

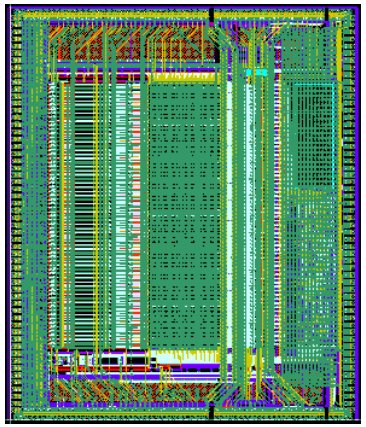


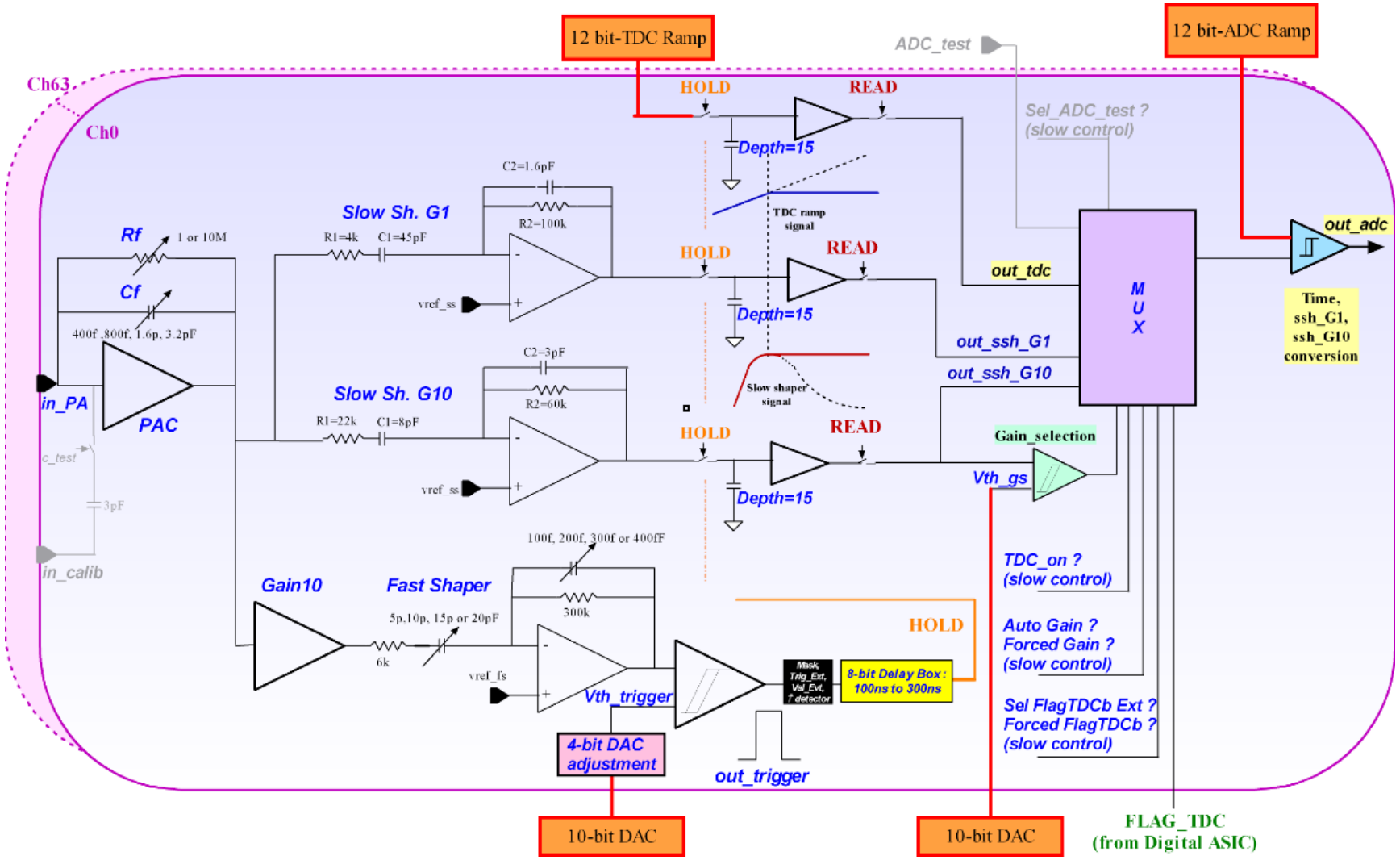
MICROROC



SKIROC2 readout ASIC

- 64-channel Silicon Kalorimeter Integrated Read-Out Chip
  - Autotrigger @ ½ MIP = 2 fC
  - Charge measurement 15 bits in two gains
  - 16-deep Analog memory
  - Low power 25µW/Ch with power pulsing
  - Embedded readout (see SPIROC)
  - SiGe 350 nm, produced in 2010





HGCROC overview

Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

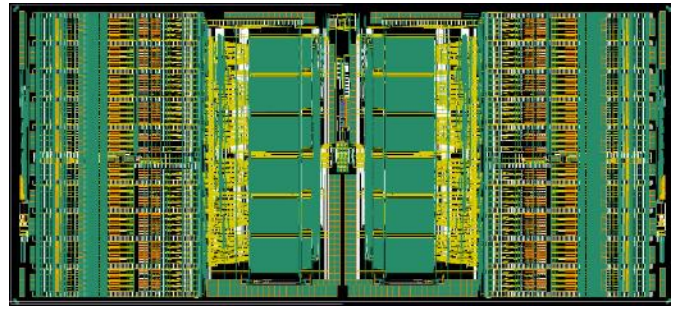
- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

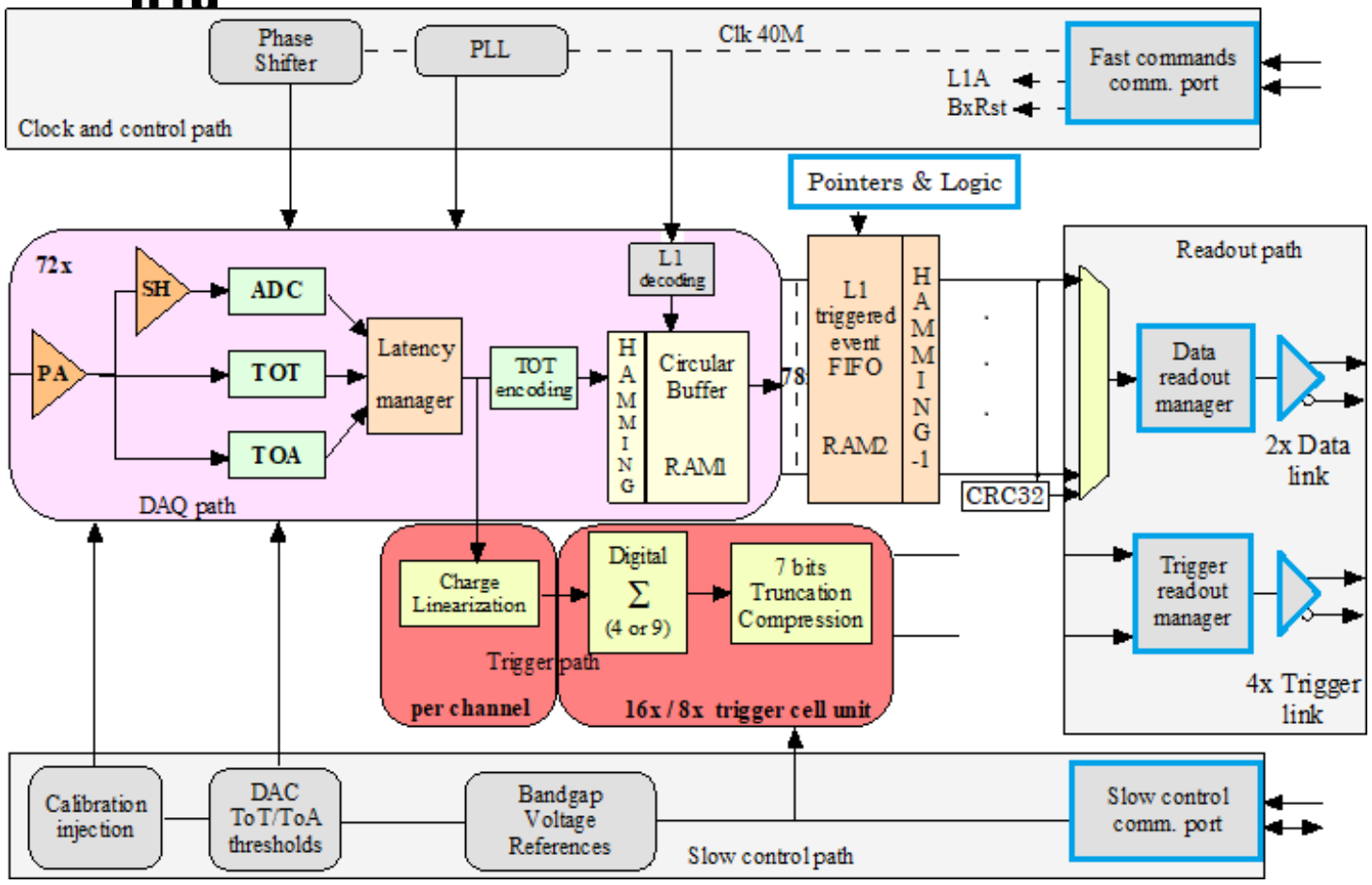
Control

- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks

- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

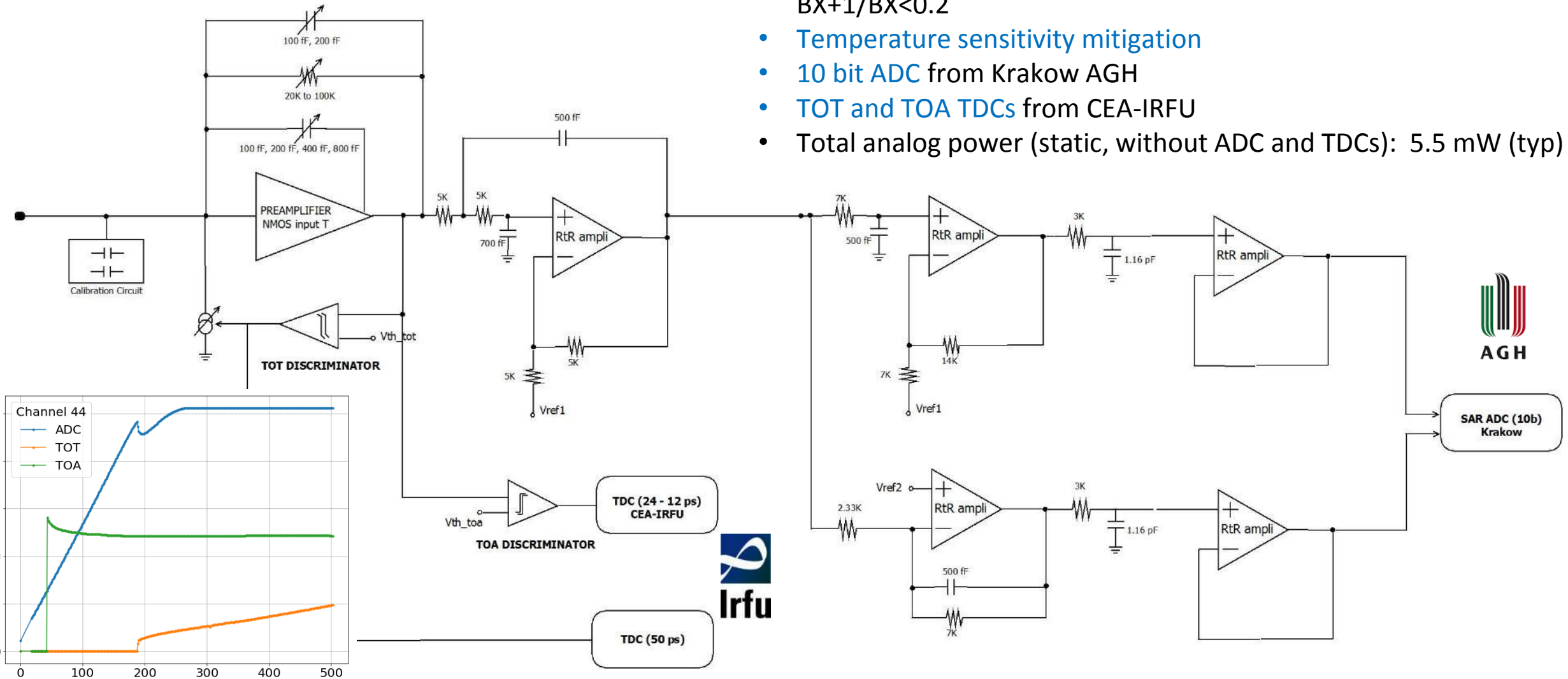




Analog Channel Overview: Silicon version

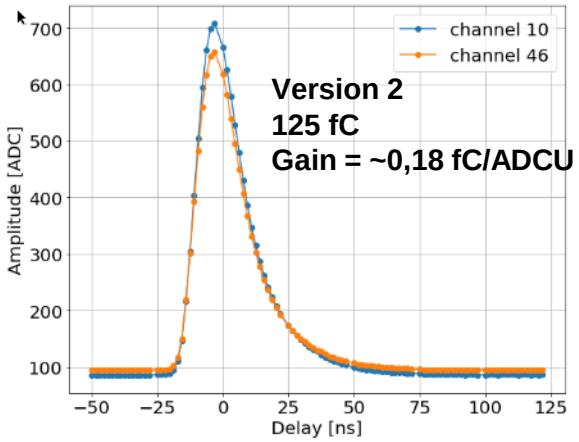
- Calibration pulser, 0.5pF and 8 pF calibration cap.
- Preamp : adjustable gains for 80, 160 and 320 fC ranges
- Tunable TOT threshold

- Compensation for the leakage current, 10 µA max. (not shown in the figure)
- Sallen Key shaper RC4, tp < 25 ns, tunable (~20%) with 2 bits, BX+1/BX<0.2
- Temperature sensitivity mitigation
- 10 bit ADC from Krakow AGH
- TOT and TOA TDCs from CEA-IRFU
- Total analog power (static, without ADC and TDCs): 5.5 mW (typ)

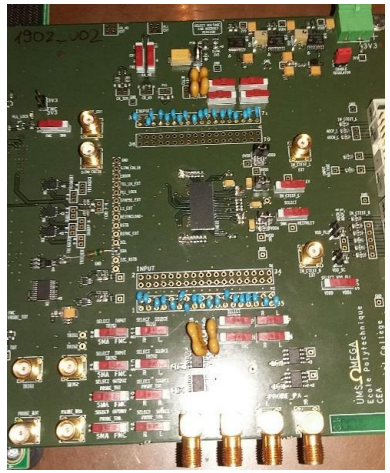


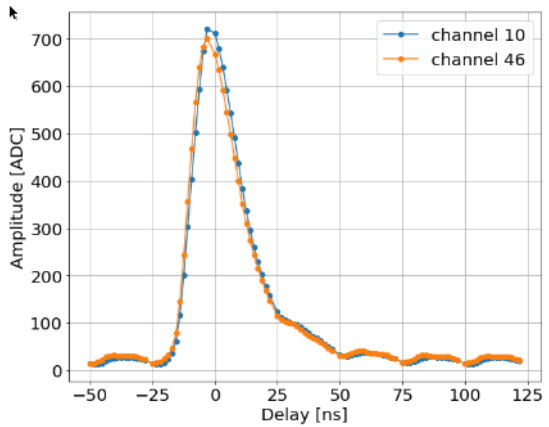
ROCv2 test boards - pulse scan reconstruction

Flip-Chip on mezzanine

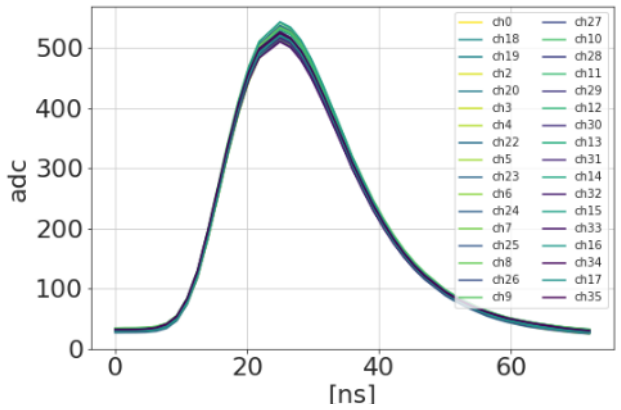


BGA board

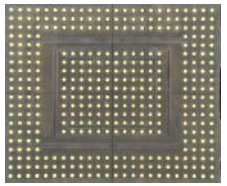


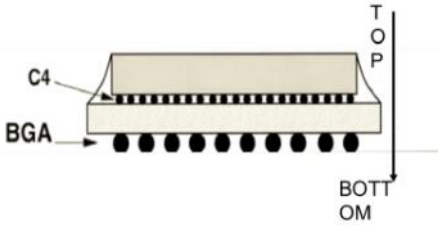


BGA on mezzanine



- Using phase shifter to move the sampling clock
- Separates effects from the BGA substrate and PCB
- Falling time (10-90 %): ~ 30 ns, < 20 % at BX+1
- Digital 40 MHz clock coupling on the analog signal on the BGA board (digital noise)





ROCv3: Charge measurements (ADC range)

- Injection and readout with the full readout chain enabled
- Internal injection with calibration DAC (low 1,5 fC offset)
- ADC noise ~0.3 fC resolution

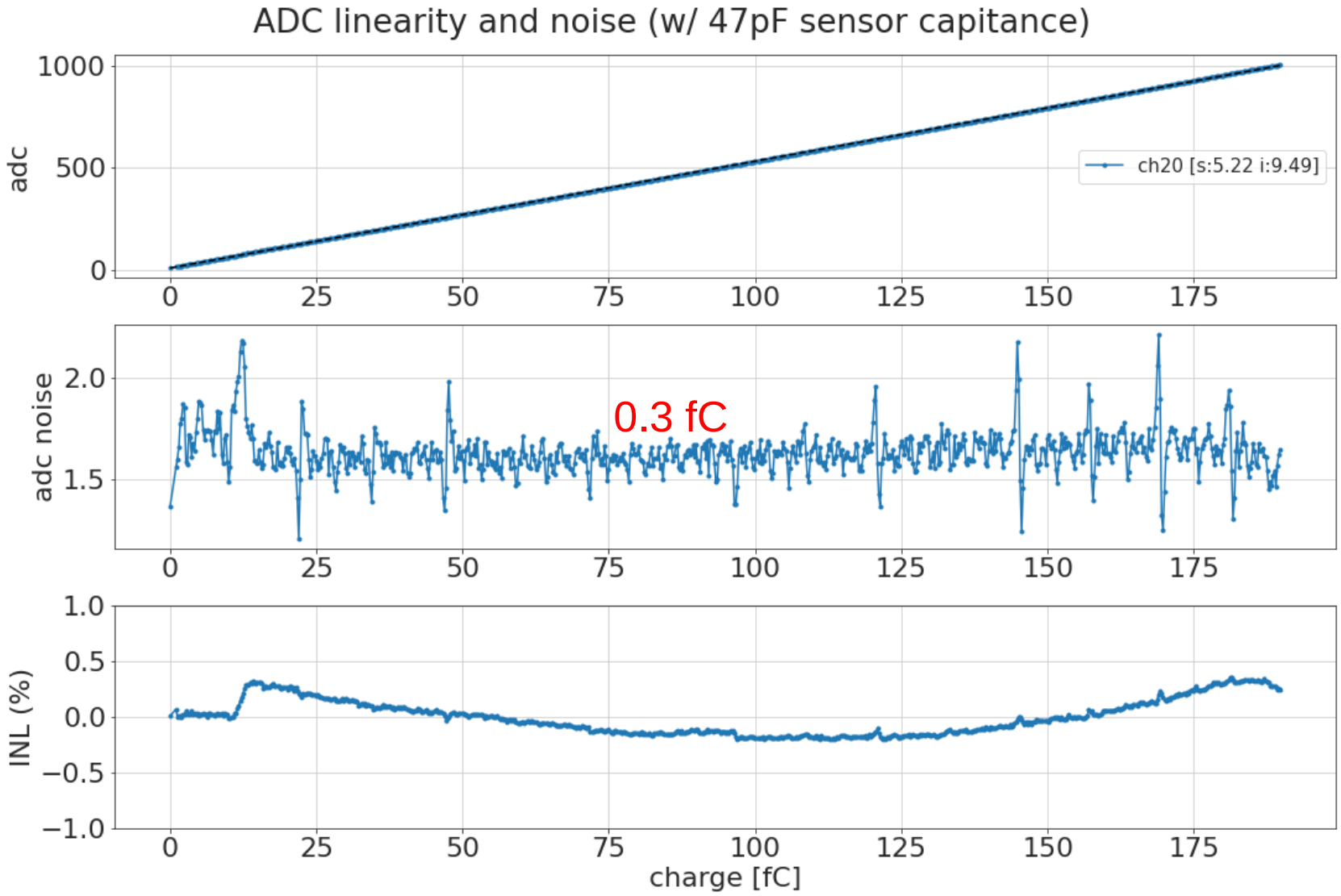
(1.6 ADCu)

- Good linearity within +/- 0.5%

1.6 fC (~1 MIP) linearity for the typical gain

➔ The results are comparable to ROCv2 in terms of noise and linearity

Preliminary results

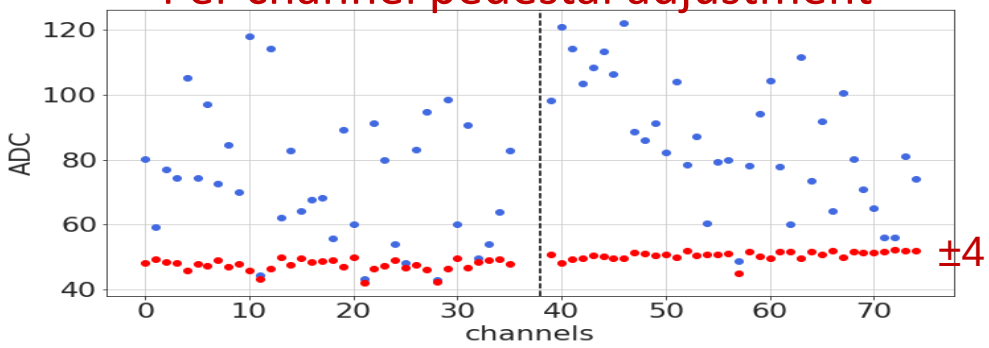


ROCv3: Noise and pedestal measurements

- Measured noise with 50 pF input cap = 0.3 fC (~ 2000 electrons) (0.7 nV / √Hz)
- Very low correlated noise contribution: max 0.15
- Comparable with HGCROC2 even if the digital activity was doubled

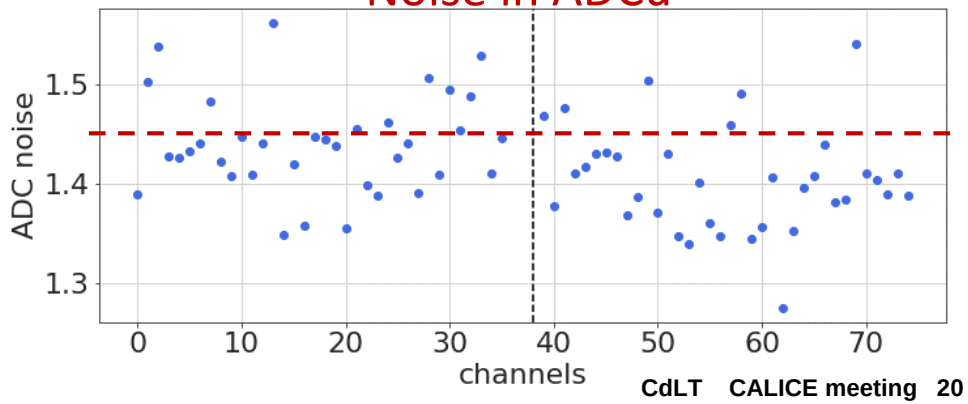
- ADC pedestal adjustment done manually with local 6b DAC

Per channel pedestal adjustment

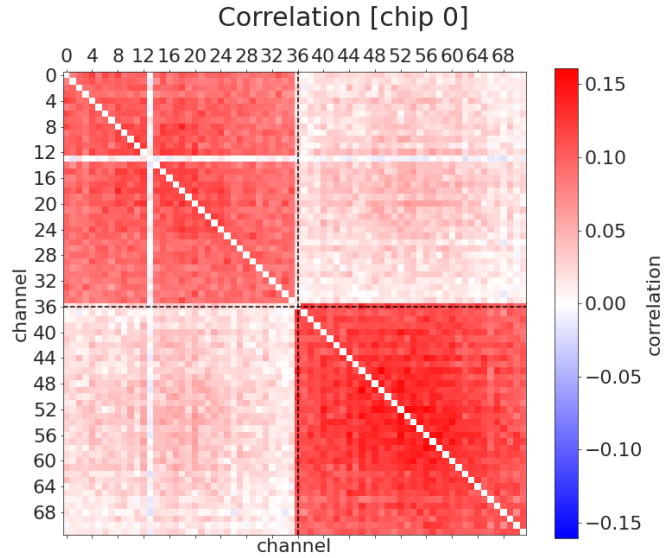


±4 ADCu

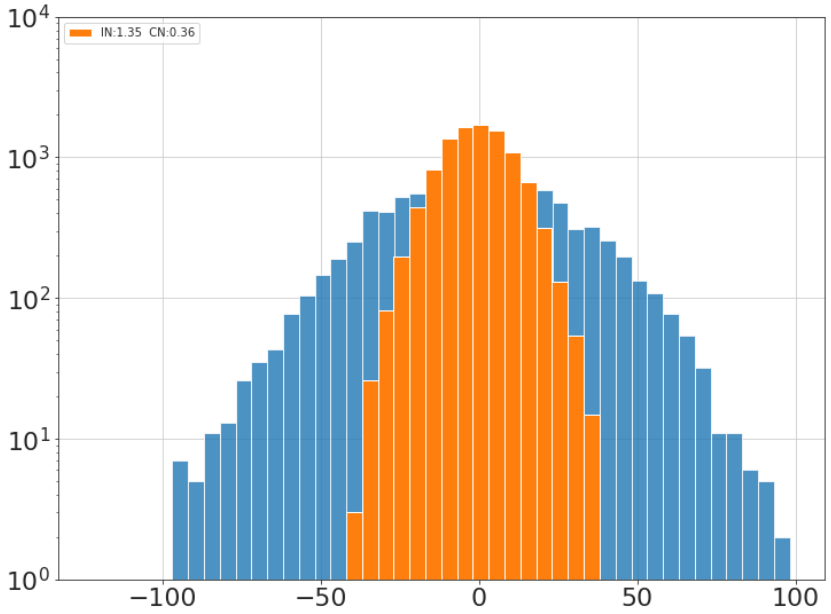
Noise in ADCu



~0.3 fC

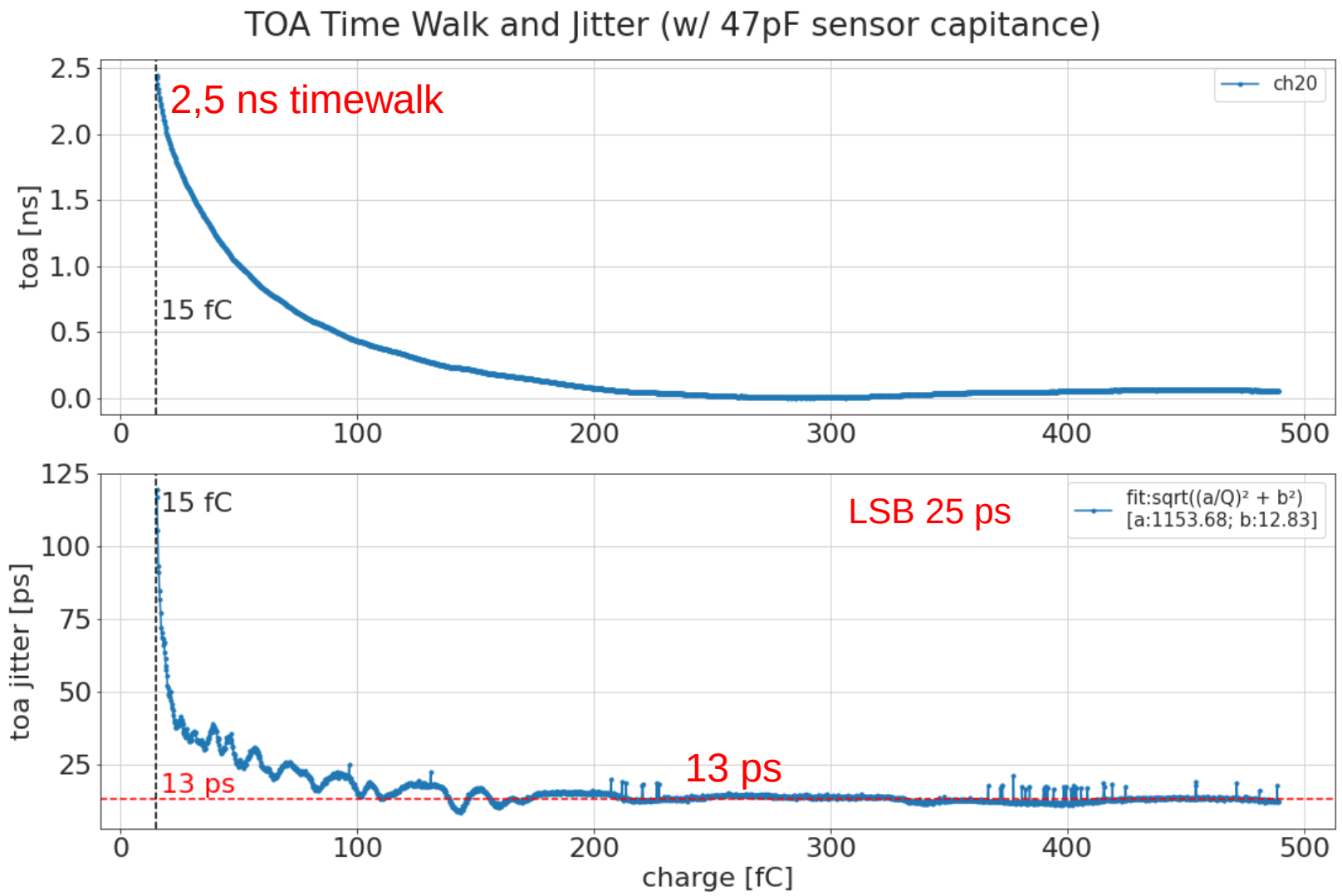


Full chip (72 channels)



ROCv3: Timing measurements (TOA)

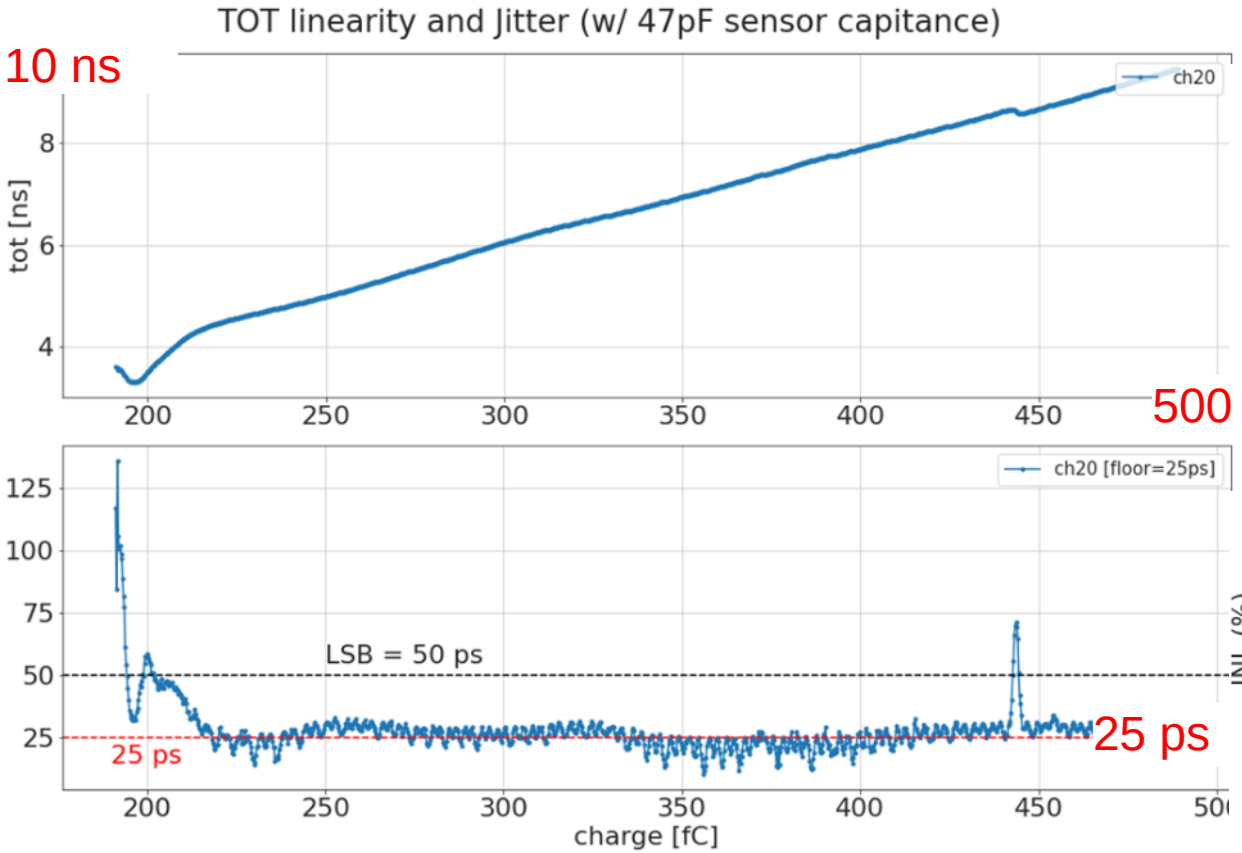
- The TDC has been improved to properly reconstruct the timing (also new layout) and to cope with outliers
- Minimum threshold set to 15 fC (20 fC for ROCv2)
- The measured jitter is about 13 ps (25 ps for ROCv2)
- Extremely promising results

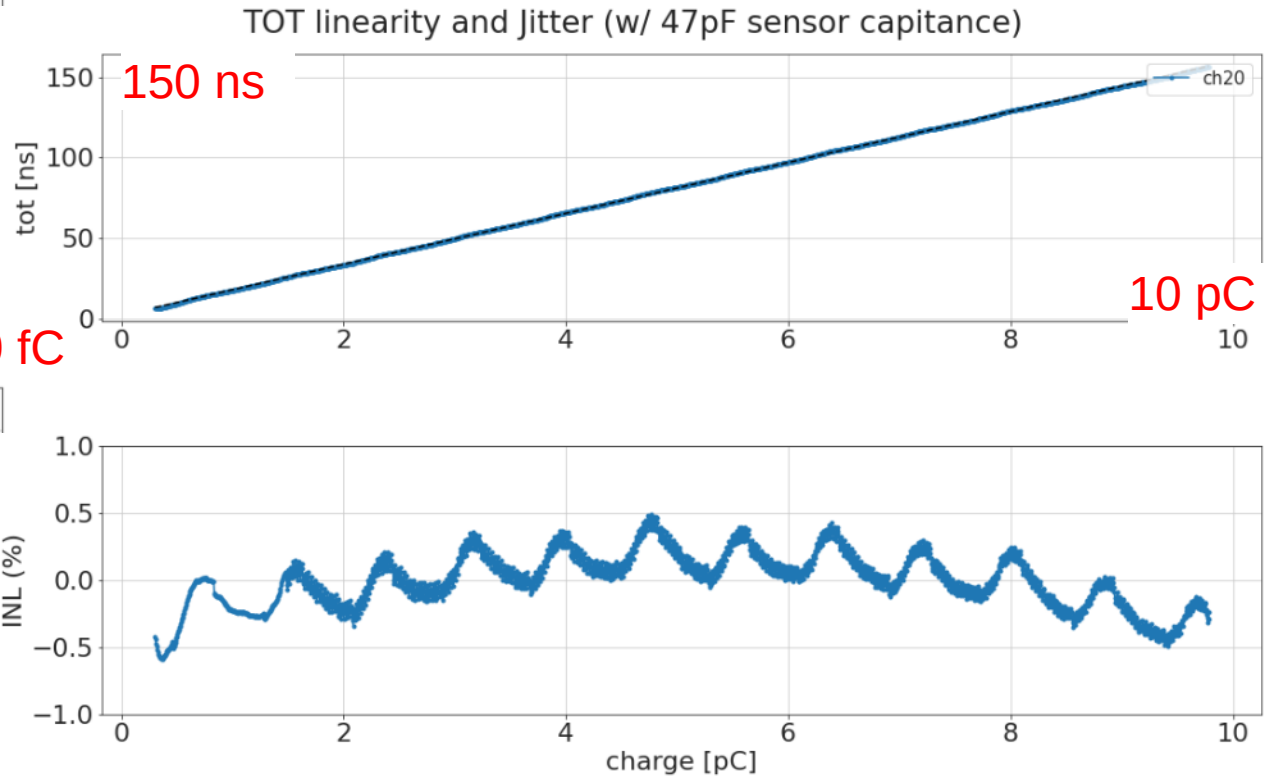


ROCv3: Time over Threshold measuremenst (TOT)

Charge measurement from TOT when preamplifier saturates (max 200 ns)

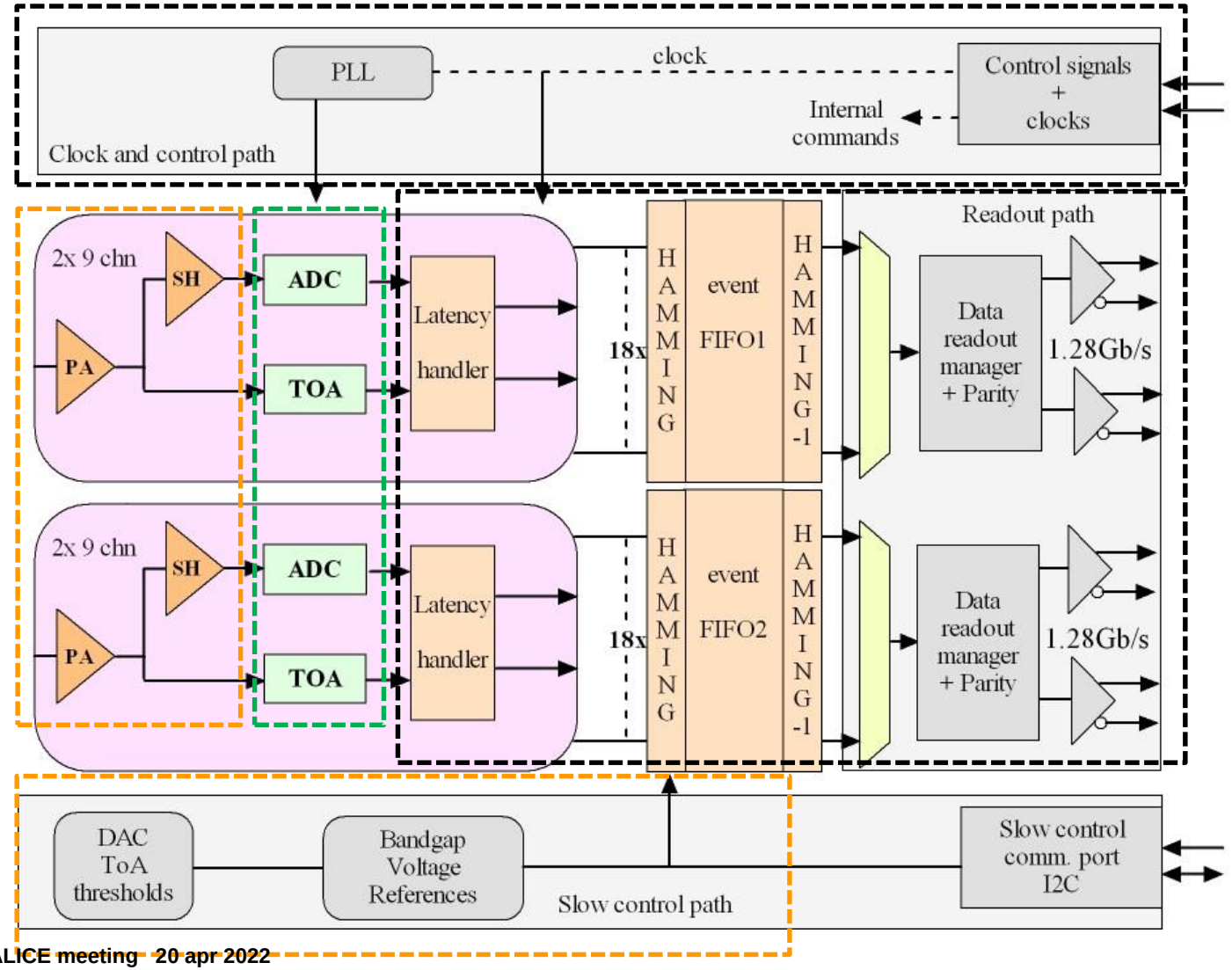
- 160 fC to 10 pC (for the typical preamplifier gain) with 12-bits TDC (LSB 50ps)
- Linearity < 1% linearity to be confirmed (2% in ROCv2)
- Resolution around 25 ps (50 ps in ROCv2)





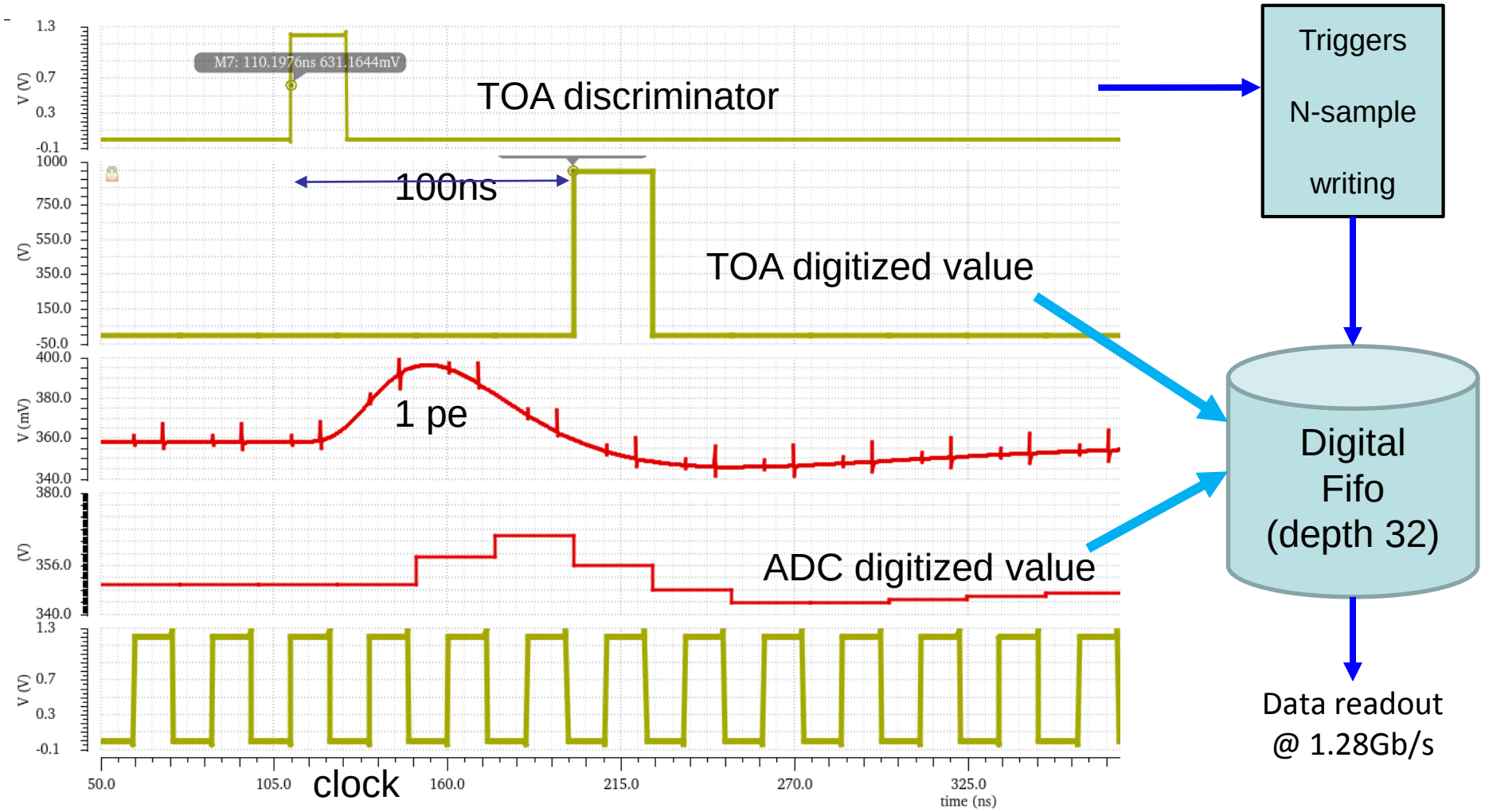
HKROC : adaptation to HyperKamioKande

- Main key points:
  - Based on the existing **HGCROC chip** for CMS-CERN (TSMC 130 nm)
  - Low power design ➔ 15 mW / channel
  - Charge measurement up to 2500 pC
  - Time measurement (25 ps)
  - 36 channels
  - 10bit 40MHz ADC from AGH Krakow
  - 25ps TDC from CEA Saclay



Full digitization chain simulation

- Full amplification and digitization chain simulated in analog mode



R&D for FCC

- Liquid argon with fine segmentation
  - ~300 ns shaping
  - 50-100 pF sensor capacitance
  - ~2 fC MIP
- cold electronics option LAr = 87K
  - Reduce feedthroughs « nightmare »
  - Multiplexing by ~100
  - Only digital data out
- Need low power Calorimeter SoC working at Lar
- Profit from AIDA Innova run end 2022 in TSMC130n

Modifications for CALICE

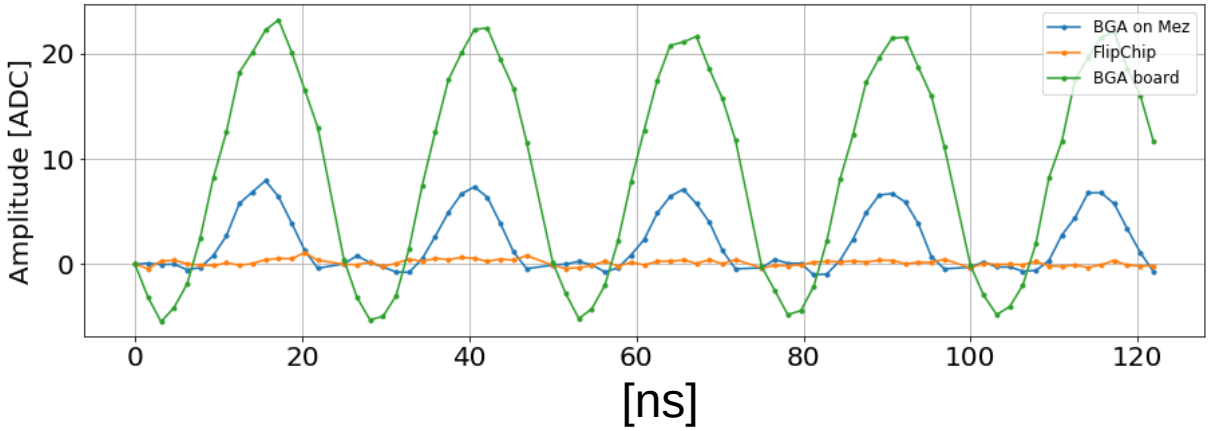
- Dynamic gain preamp or TOT ?
- 200 ns shaping, 10 MHz ADC, several samples on the waveform
- Timing capability ? Auto-trigger and zero suppression
- Target ~1 mW power/ch and possible power pulsing
- I²C slow control ? New readout protocol ?
- Include 2.5V LDO inside VFE ?
- Compatible with FCC LAr. SiPM/RPC tbd

	experiment	Sensor	capacitance	shaping	power	data	techno	Vdd	slow control
SKIROC2	CALICE	Si	30 pF	300 ns	5 mW/ch	5 MHz	SiGe 350n	3.3 V	SPI
HGCROC	CMS	Si	50 pF	20 ns	20 mW/ch	1.2 Gb/s	TSMC 130n	1.2 V	I²C
FCC	LAR	Lar	50-200 pF	200 ns	<1 mW	Gb/s	TSMC 130n	1.2 V	I²C
SKIROC3	CALICE	Si	50 pF	200 ns	<1 mW	Mb/S	TSMC 130n	1.2 V	?

backup

Digital noise

- A 40 MHz modulation is visible on the analog signals
  - Comes from digital current spikes on preamp ground node
    - 10 µV on ground give 1 ADC count
  - BGA worse than flip chip
  - BGA substrate optimised, improvements made by optimizing decoupling & the pcb ground impedance
  - Further improved by removing decoupling caps !
    - Reduces digital current spikes (inductance)



- This provides recommendations for the Hexaboard design
  - Very delicate design!