SiW-ECAL: Better event building

Lessons learned from TB2022-03

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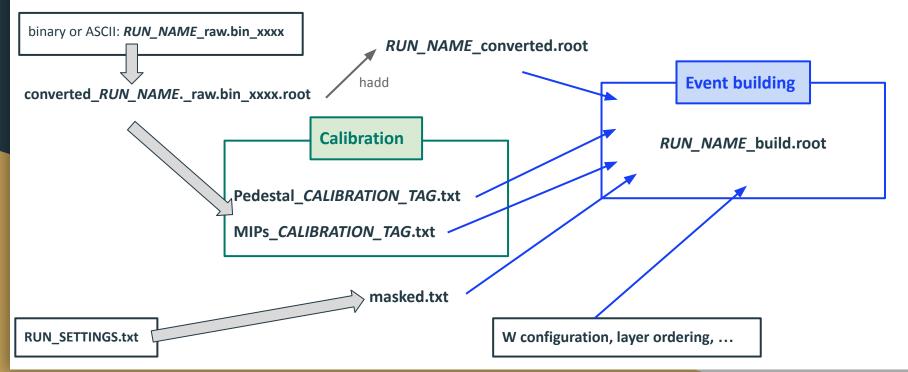


Overview

- Introduction: Event building
- Empty events
- Chip hits split

Event building

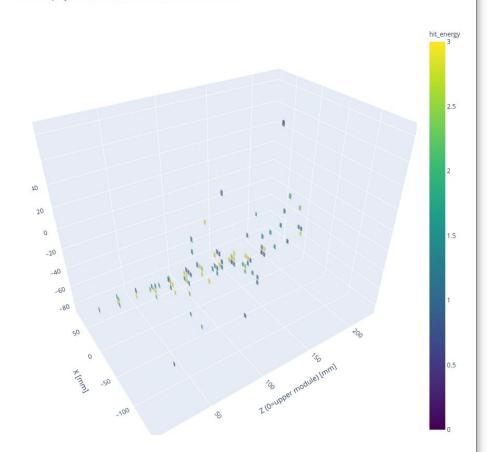
Event building pipeline

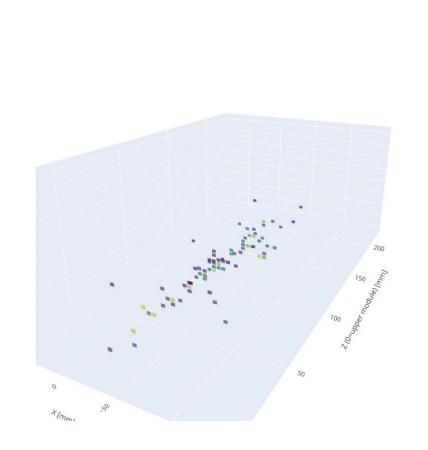


Comparing Simulation with data: build.root files

- simulation.lcio → sim_build.root written by Fabricio
- E.g. raw energy spread plots (see later)
- New monitoring scripts to create the build.root file while the run is ongoing
- Next slide: Event displays real data (left) & simulation @3GeV







hit_energy

0.8

0.6

0.4

0.2

<u>SiWECAL-TB-monitoring</u> for just-in-time event building

- steering file per SiW-ECAL setup
- Constant feedback

```
[INFO 09:28:32] Logging to file /afs/cern.ch/user/j/jokunath/public/
[DEBUG 09:09:32:39] Channel masks written to /afs/cern.ch/user/j/jokunat in mi
[INFO 09:00009:32:39] The run has finished. Monitoring will try to catch to get in the converted of the converted
```

```
max workers = 10
     output parent = data
     skip dirty dat = False
     # Only used if the raw data is in raw.bin XXXX format. -1 for no split
     binary split M = 50
     # Needs some extra python packages, and adds some extra time. For batch
     # finished runs, you might want to set this to `quality info`= False`.
     quality info = True
     [snapshot]
     after = 1, 10
     everv = 50
     # Setting this to True can save some disk space for long runs.
     delete previous = False
     # Any field in `default eventbuilding.cfg` can be overwritten here.
     # That is also where you can find explanations of their meaning.
     # (local) ./continuous event building/SiWECAL-TB-analysis/eventbuilding
     # (online) https://github.com/SiWECAL-TestBeam/SiWECAL-TB-analysis/tree
     [eventbuilding]
    min slabs hit = 6
    # Tungsten thickness in mm. A single number is interpreted as per layer
    asu versions = 13,13,COB,COB,11,11,11,12,12,12,12,11,11,10,11
    \max entries = -1
     no lg = False
     zero suppress = True
     merge within chip = True
     pedestals file =
                             example/dummy calibration/Pedestal dummy high
     mip calibration file =
                              example/dummy calibration/MIP dummy highgain.
     pedestals lg file =
                              example/dummy calibration/Pedestal dummy lowga
     mip calibration lq file = example/dummy calibration/MIP dummy lowgain.t
                              continuous event building/SiWECAL-TB-analysis/
35 mapping file cob =
                             continuous event building/SiWECAL-TB-analysis/
```

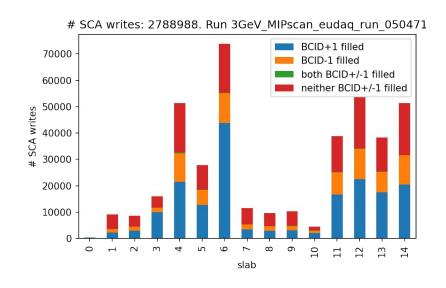
monitoring.cfg

[monitoring]

Empty SCA frames

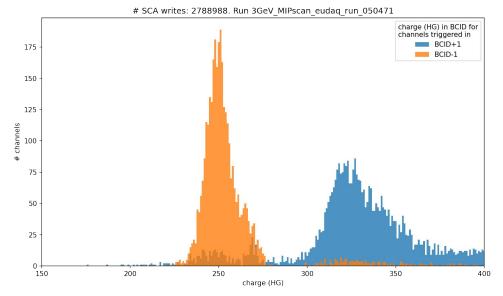
SCAs without hits (and their neighbours)

- BCID empty, BCID+1 filled
 - o (analog) delay cells
- BCID empty BCID-1 filled
 - o digital connection issue
 - well & long known, Stéphane can explain it better (2016 CALICE meeting)
- both BCID+/-1 filled
 - most of the times probably just a retriggering train
 - o sometimes not
- neither BCID+/-1 filled
 - 0 ???
 - I found that other chips tend to have SCA readouts on this BCID
- Effect much smaller for Skiroc2a (vs Skiroc2)



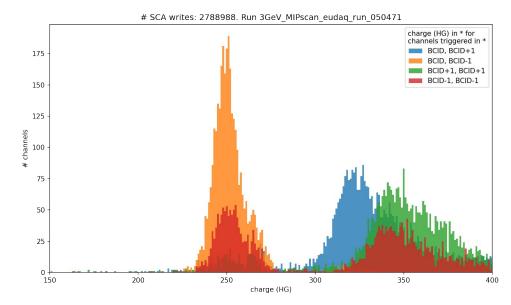
Charges in the empty events

- The following plots on layer 7 only.
- Charges from triggered channels before/after an empty event



Charges in the empty events

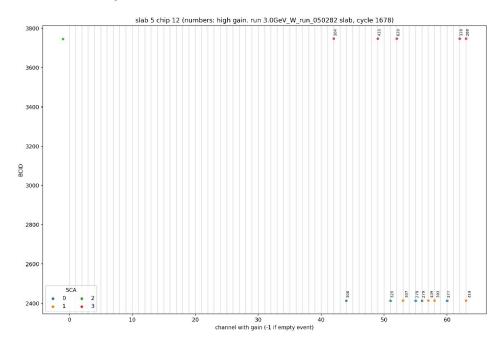
- The following plots on layer 7 only.
- Charges from triggered channels
 before/after an empty event
- The charge histograms from empty SCA frames look less good
- Especially triggered SCA with hits better than empty triggered SCA before it

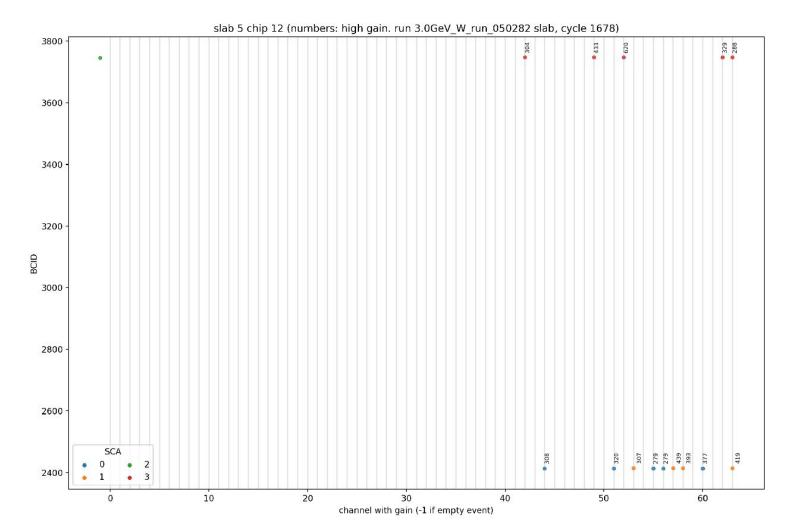


Chip hits split

Chip hits split over multiple BCIDs/SCAs

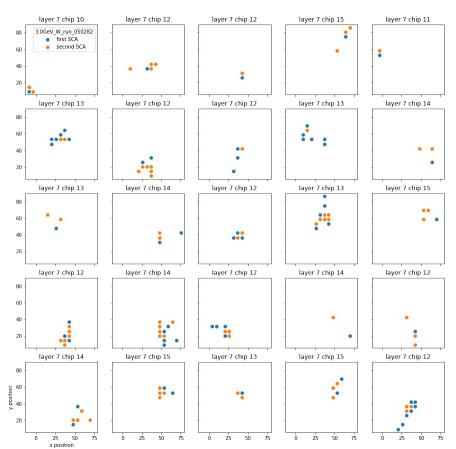
- Triggers on different channels in consecutive BCIDs
- If more than 2 SCAs in a row, probably retiggering effects
- Due to Delay box?





Chip split in x-y

 No obvious pattern for first/second SCA of the splitted event in x vs y

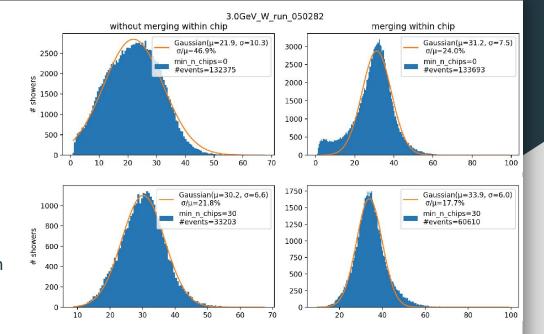


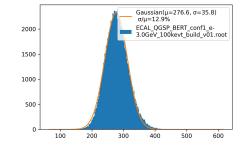
Energy spread

- Left: before within chip merging
- Clearly, the merging is necessary
- Some chips not great: require
 min_n_chips for improvements
- Lowest: Comparison with Simulation
 @Fabricio (here: before any digitisation, masking, ...)

Caveats

- At these low energies, counting hit channels should be better than sampling-fraction weighted energy sum
- Prelimary MIP & Pedestal calibrations
- No correction for masked cells here





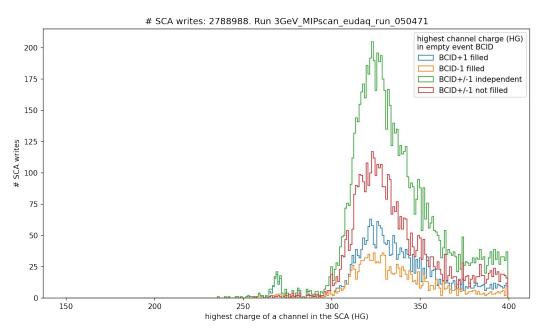
Summary

- 1. **Empty SCAs**: (most of the time, at least for event building): just take the BCID-neighbouring, non-empty SCA
- 2. **Hits splitting** on same chip: if exactly 2 consecutive SCAs: take the union of triggered channels
- 3. New **JIT-build-monitoring** tools
- 4. **SIM-vs-data** comparison tools in place

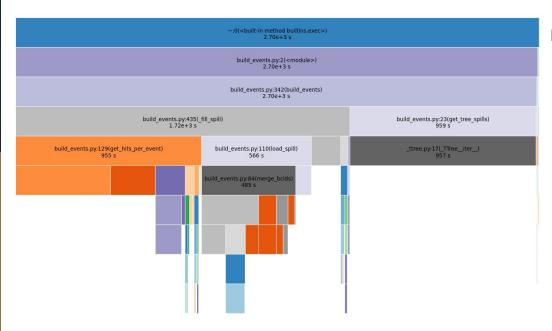
Backup

Highest charge per readout

- Here, plotted only highest charge per SCA
- All histograms look rather similar



Is this fast enough?



Profiling shows:

- No obvious bottlenecks left
- > ⅓ of time spend in get_tree_spills (loading data to memory?)
 - I do not think this can be sped up
 - Even pure ROOT/C++ should not be faster here
- Upfront cost usually < 8s
 - Loading imports
 - Loading & improving calibration
 - Writing calibration histograms
- merge_bcids could potentially be faster
 - o But why bother?

Why buildfiles

event spill bcid prev_bcid next_bcid nhit_slab nhit_chip nhit_chan nhit_len sum_hg sum_energy

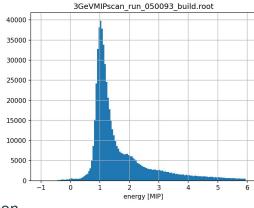
Event level information

- Useful for selection
- e.g. "nhit_slab > 10"



hit arrays

- Know which hits belong together
- hit_energy: calibration applied. ==1 for average MIP deposit



```
[1]: import awkward as ak
import matplotlib.pyplot as plt
%matplotlib widget
import numpy as np
import uproot

file = "3GeVMIPscan_run_050093_build.root"
    ar = uproot.open(file)["ecal"].arrays(filter_name="hit_*")
    n_slabs = uproot.open(file)["ecal"]["nhit_slab"].array()

[2]: hits = ar[n_slabs > 10]
    hits = hits[hits.hit_isHit == 1]
    energy = ak.flatten(hits.hit_energy).to_numpy()
    fig, ax = plt.subplots()
    ax.hist(energy, bins=np.arange(-1, 6, 0.05))
    ax.set_xlabel("energy [MIP]")
    ax.set_title(file)
    ax.grid()
```

