CALICE SiW ECAL – Way to 15 layer stack

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On behalf of the SiW ECAL Groups in CALICE:

CALICE Meeting IFIC Valencia – April 2022

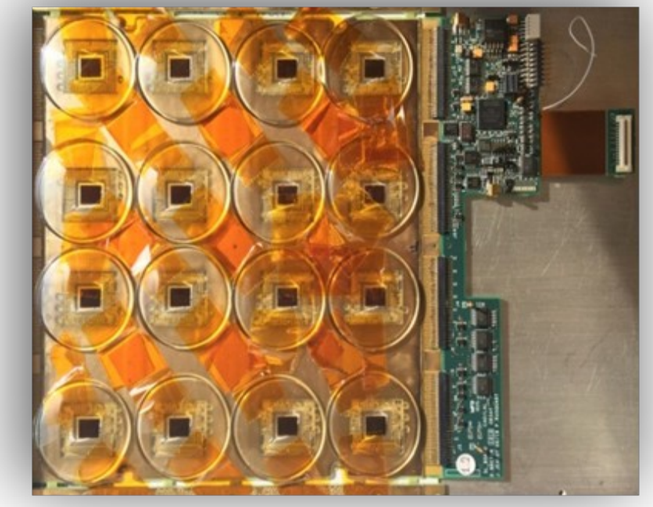
Prologue – “The FEV Zoo”

- In recent years the SiW ECAL has developed and used several PCB variants
  - To make sure that you don't get lost, here comes an introduction

FEV10-12

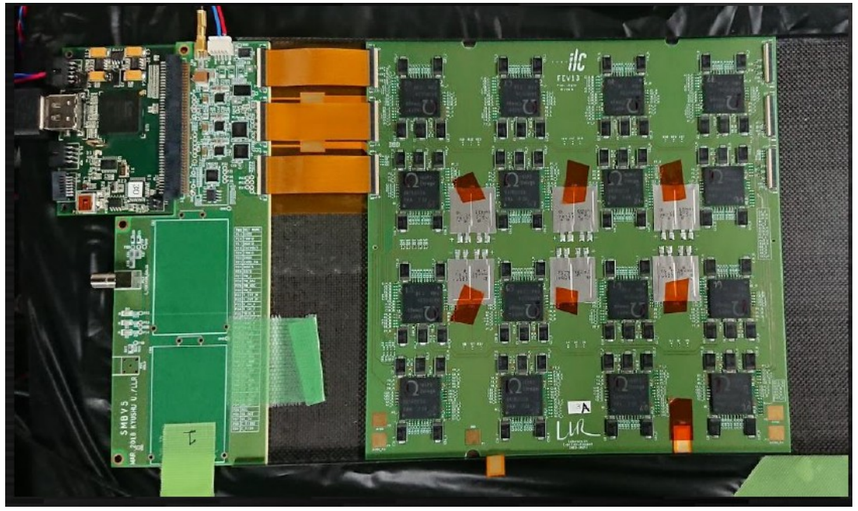
- ASICs in BGA Package
- Incremental modifications
  From v10 -> v12
- Main “Working horses” since 2014

FEV_COB



- ASICs wirebonded in cavities
  - COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

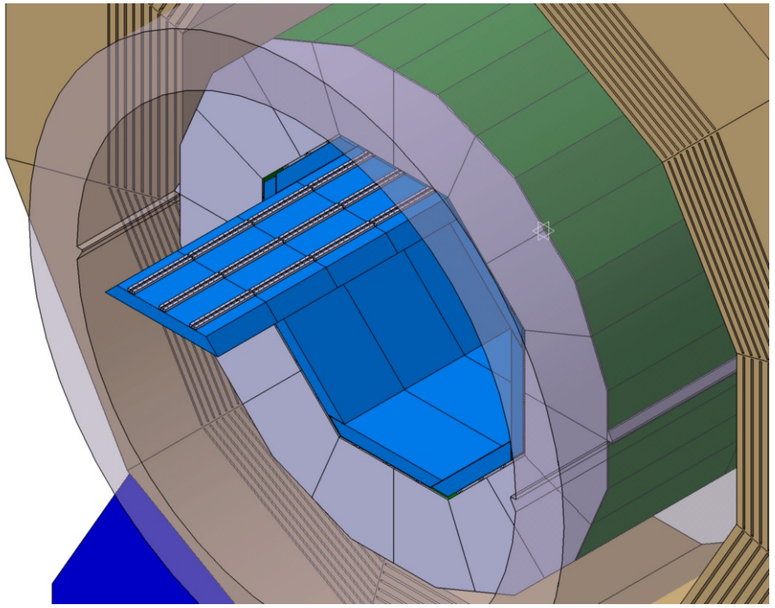
FEV13



- Also based on BGA packaging
- Different routing than FEV10-12
- Different external connectivity

Silicon Tungsten electromagnetic calorimeter

- Optimized for Particle Flow: Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

- $O(10^8)$ cells
- “No space”
=> Large integration effort

Basic Requirements:

- Extreme high granularity
- Compact and hermetic
- (inside magnetic coil)

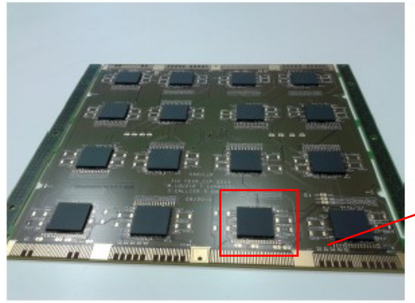
Basic Choices:

- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, Φ=96mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design
  - Allows for pixelisationRobust technology
  - Excellent signal/noise ratio: 10 as design value

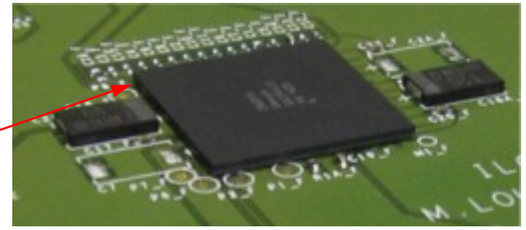
- All future e+e- collider projects feature at least one detector concept with this technology
  - Decision for CMS HGCAL based on CALICE/ILD prototypes

SiW Ecal – Elements of (long) layer

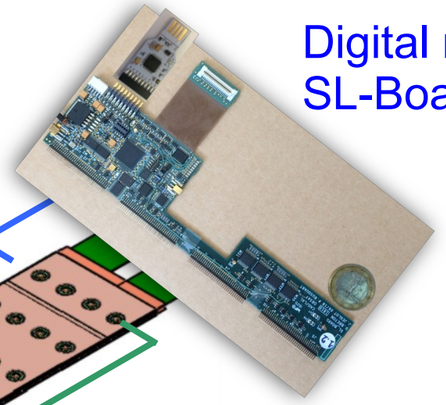
ASIC+PCB+SiWafer
=ASU
Size 18x18 cm²
(IJCLab, Kyushu, OMEGA, LLR, SKKU)



ASIC SKIROC2(a)
(OMEGA)
Wire Bonded or
In BGA package
(IJCLab, Kyushu, LLR)

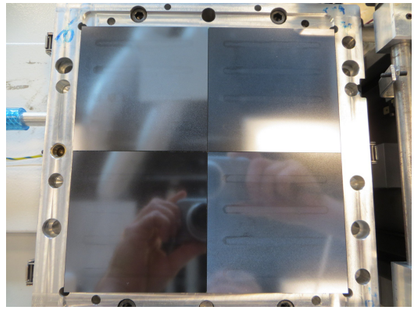


Interconnection
(IJCLab)



Digital readout
SL-Board (IJCLab)

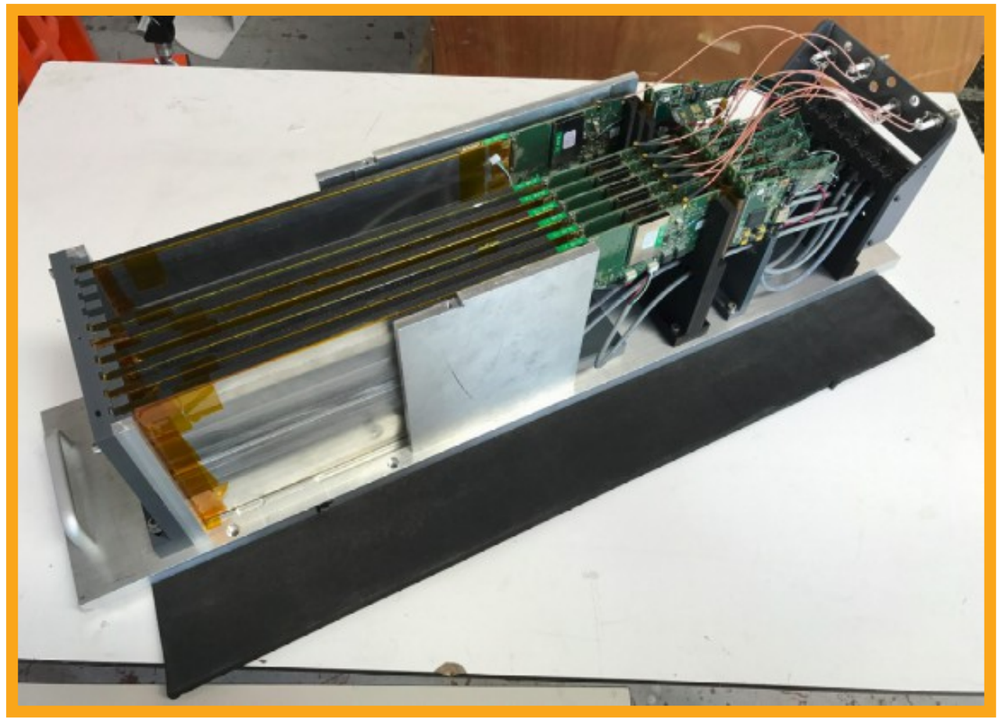
SiWafers glued onto PCB
Pixel size
5.5x5.5 mm²
(LPNHE)



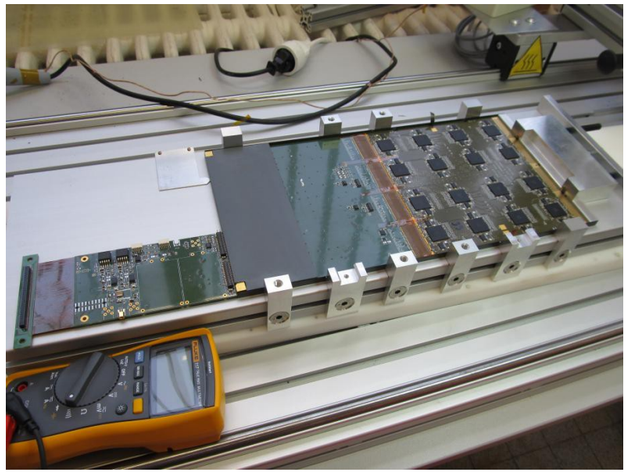
Note that an additional hub for hardware Development is being set up at IFIC/Valencia

- The beam test set up will consist of a **stack of short layers** consisting of one ASU and a readout card each

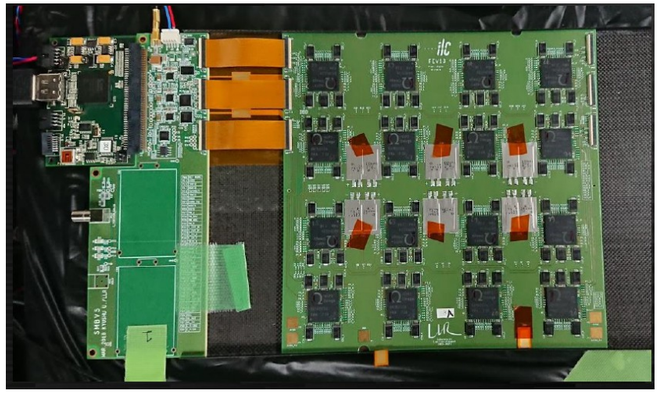
Prototypes until ~2018



- Total ~15 layers constructed
  - Max of ten tested within one stack
- 1024 channels per layer
- Assembly chains in France and Japan
- Beam tests at DESY and CERN since 2016



PCB FEV10-12
with long adapter card
Wafer thickness
325 µm

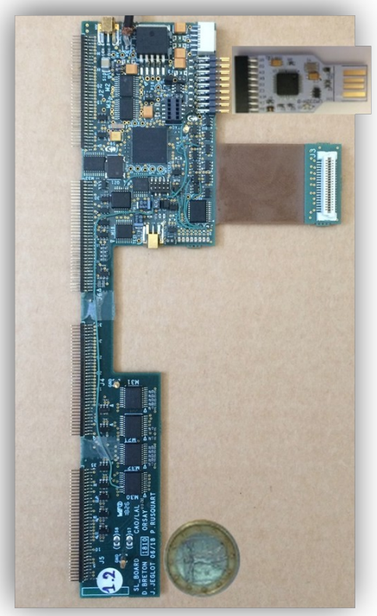


PCB FEV13
with small(er) adapter card
Wafer thickness
650 µm

R&D for thin PCB see backup

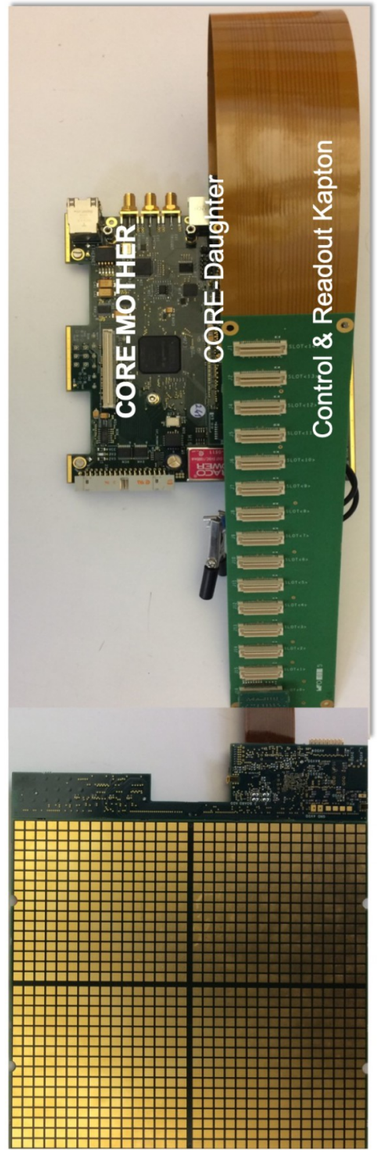
Compact readout

Current detector interface card (SL Board) and zoom into interface region



SL Board

Complete readout system

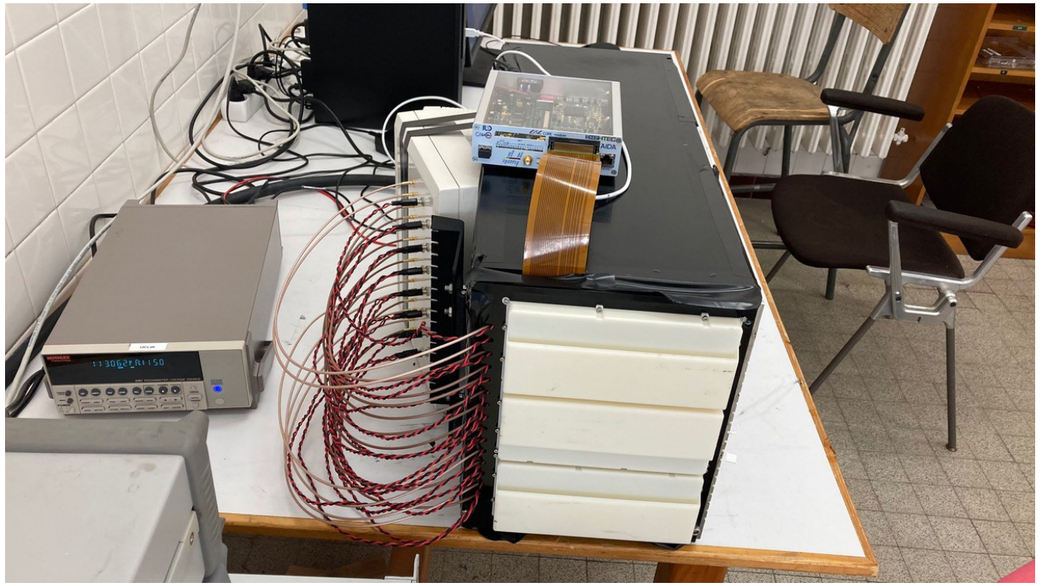


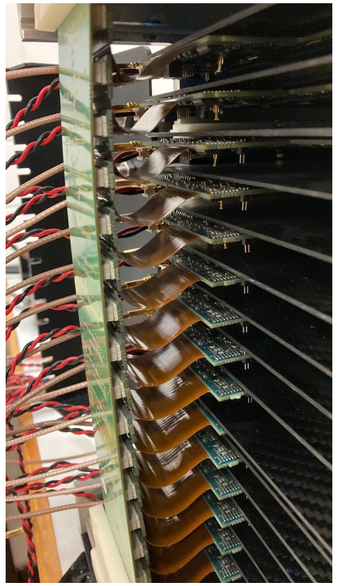
- “Dead space free” granular calorimeters put tight demands on compactness
  - Current developments in for SiW ECAL meet these requirements
- System allows to read column of 15 layers <-> to be expected in ILD
  - Important that full readout system goes through scrutiny in beam tests

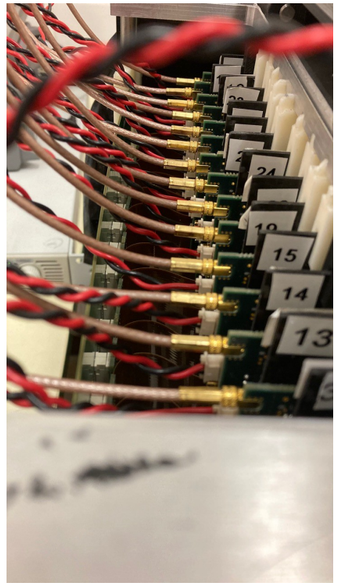
- Note that 11 layers equipped previously with long adapter card have been disassembled and equipped with SL Board

15 layer stack Stack

- Mechanical housing by IJCLab
- First operation in Summer 2020 with 4 damaged slabs
- Two new slabs produced and two slabs repaired over Winter/Spring 2020/21
- Re-start on 2nd of June with 15 “full” layers by Yuichi (PhD), Robin (intern), IJCLab engineers and technicians and Adrian during visit to IJCLab
  - Reminder: 15 layers correspond to 15360 cells







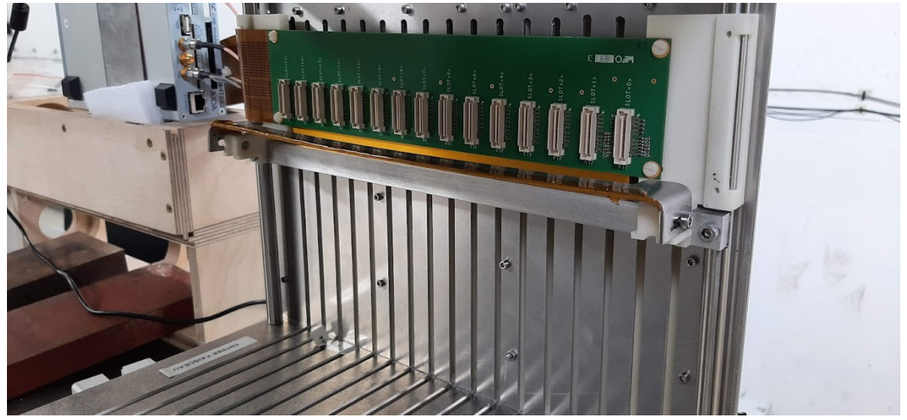
- Since 2/6/21: Commissioning

- Since 18/6/21: Data taking with cosmics and systematic characterisation

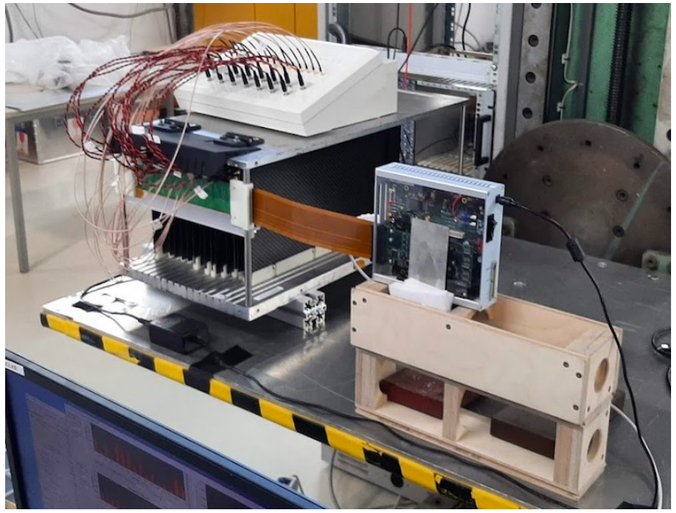
Operation modes

- Mechanical
  - Stack can be operated in “MIP Mode” and in “Tungsten mode”
  - Rails with thicknesses of 2.8mm and 4.2 mm
  - Detector is small and handy enough to switch between modes during a beam test
  - Switch will take around 1/2 day
  - For commissioning we operate in “MIP Mode”
- Electrical
  - Currently we operate in continous mode (i.e. not power pulsed)
  - A priori possible but ASUs not optimised for pp-mode
  - Left for FEV2.x (>= 2022)

Interior view on mechaniccal strucutre with CORE Kapton

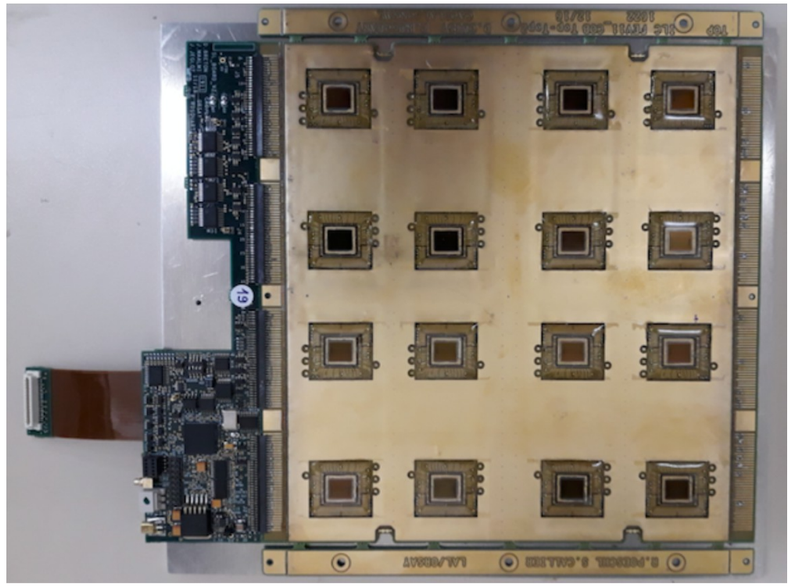


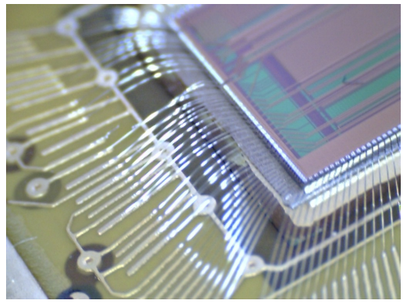
Equipped stack at DESY before closing



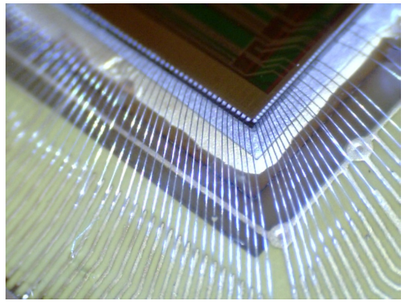
ASUs based on COBs

- Two COBs in beam test
  - Replaced two layers of stack in March beam test





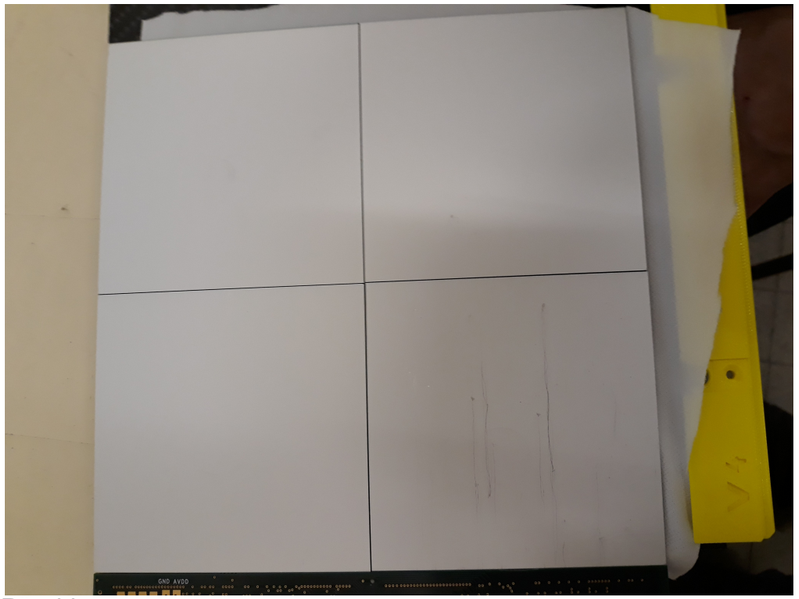
Before application of epoxy



After application of epoxy

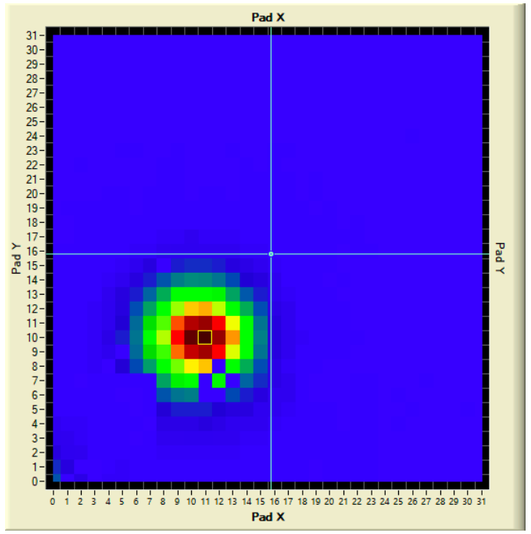
- Three COBs encapsulated at IJCLab
  - Excellent pioneering work!
  - Two used for beam test
  - The third one has 15/16 chips operational (may need a further look)
- A fourth one encapsulated at IFIC/Valencia
  - Ready for usage

Gluing wafers onto COBs

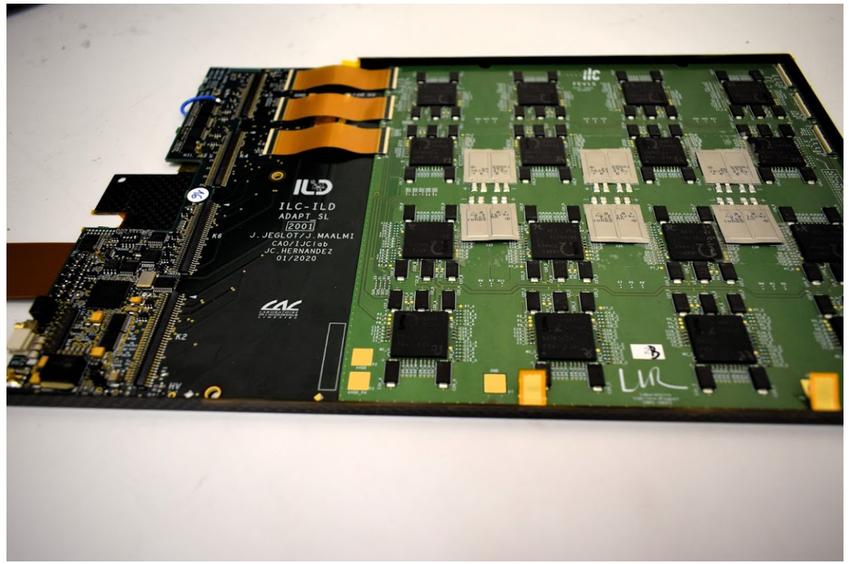


- Wafer gluing at LPNHE
- Since a decade it was a concern whether wafers could be glued on flat COBs
- Gluing of one wafer already in 2019
- Gluing of four wafers onto two boards during winter 2020
- This step together with the beam test in March 2022 concludes the first R&D cycle on the COBs

Beam spot in COB



Adaptation of FEV13



FEV13 connected via interface card to SL-Board

- Interface card for allows for integration of FEV13 in stack
  - Successful technical tests in Autumn 2020
  - In total 7 FEV13 equipped with wafers are available in F and JP
  - Two FEV13 used for beam test in March 2022

Testbeam readiness review – 7/10/21

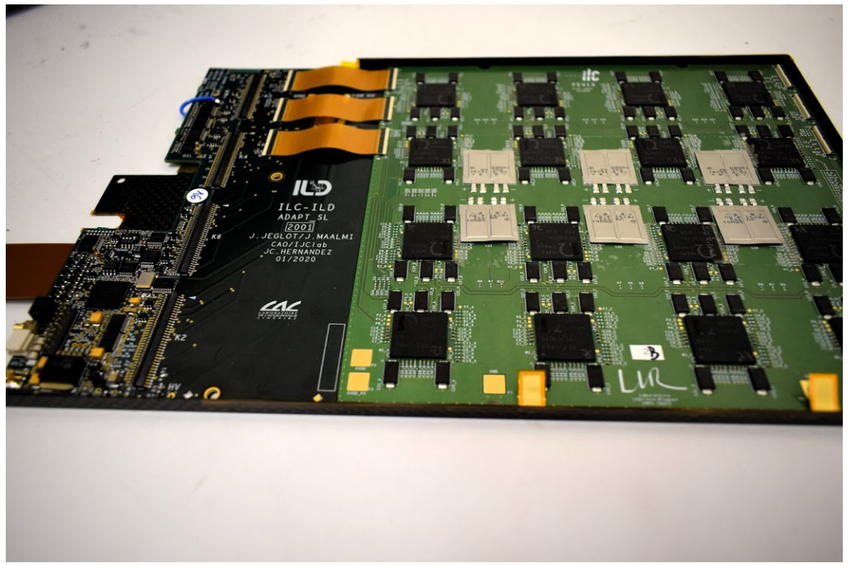
- Review organised by CALICE TB before November 2021 beam test
- Reviewers: Mary Cruz (CIEMAT), Jiri (FZU) and Shen (UHEI)

Summary and outlook

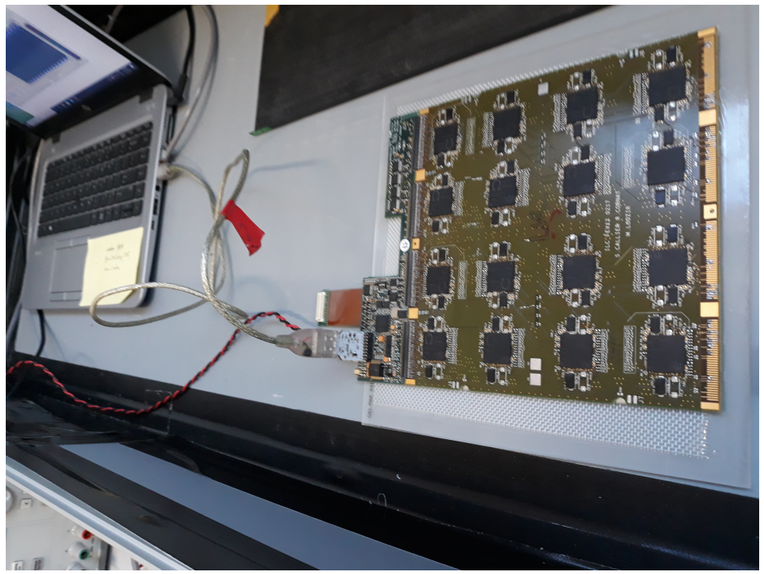
- Since 2017 - Compilation of stack with 15 layers to allow for consistent system tests of SiW ECAL
  - Lots of development work
  - Compact readout
  - Encapusaltion techniques for COB
- Regular running of stack with 15360 readout cells since beginning of June 2021
  - Stack is a combination of freshly produced layers and layers recycled from 2015/16 production
  - Easy integration of new layers
  - FEV13, COBs
  - New compact DAQ allows for smooth running and data taking (see talk by Jihane)
- Two beam tests in November 2021 and March 2022
  - Enormous learning curve
  - Experience shows (again) that only system tests in beam allow to get a complete picture on the atatus of the R&D
  - Stay tuned for further talks today and on Friday

Backup

Interface to FEV13 and Deployment of hardware



FEV13 connected via interface card to SL-Board



New FEV12 on single slab test bench

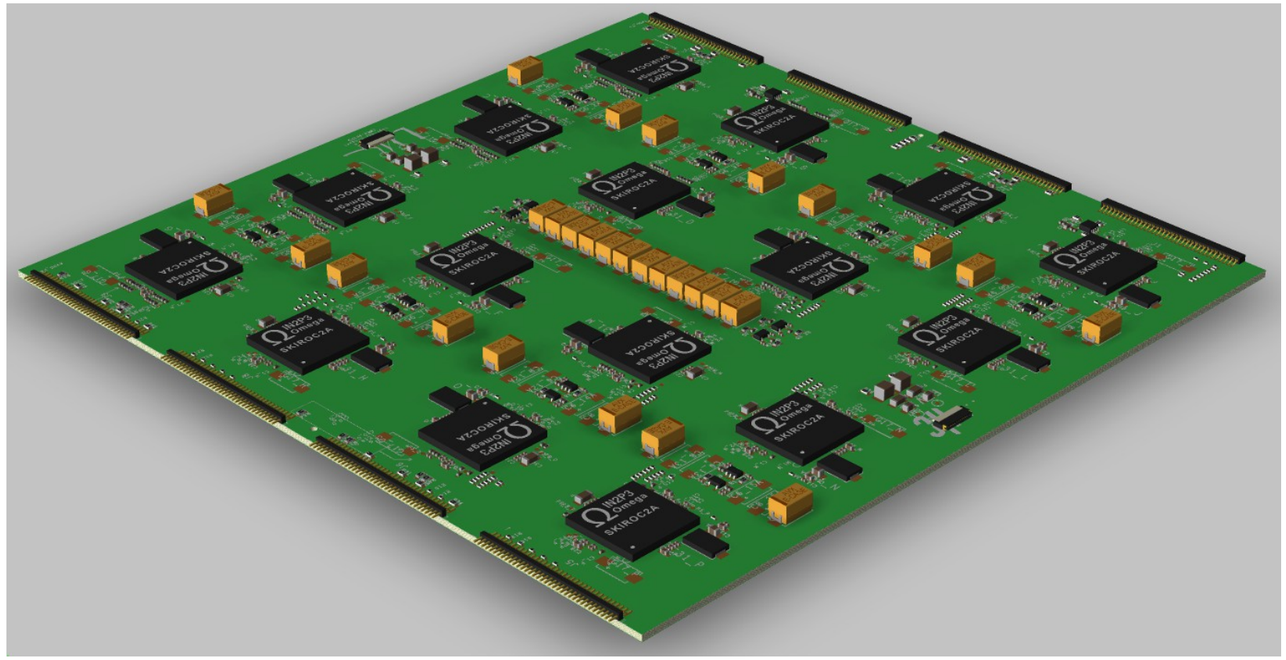
- Interface card for allows for integration of FEV13 in stack
  - Successful technical tests in Autumn 2020
  - In total 7 FEV13 equipped with wafers are available in F and JP
- Started to deploy Hardware/software for digital readout (i.e. SL-Board and User Interface) to other Ecal groups
  - First “client” LLR
  - IFIC will follow during visit of Adrian end of May/June, as soon as travel will be possible
  - In preparation of deployment to Japan is planned

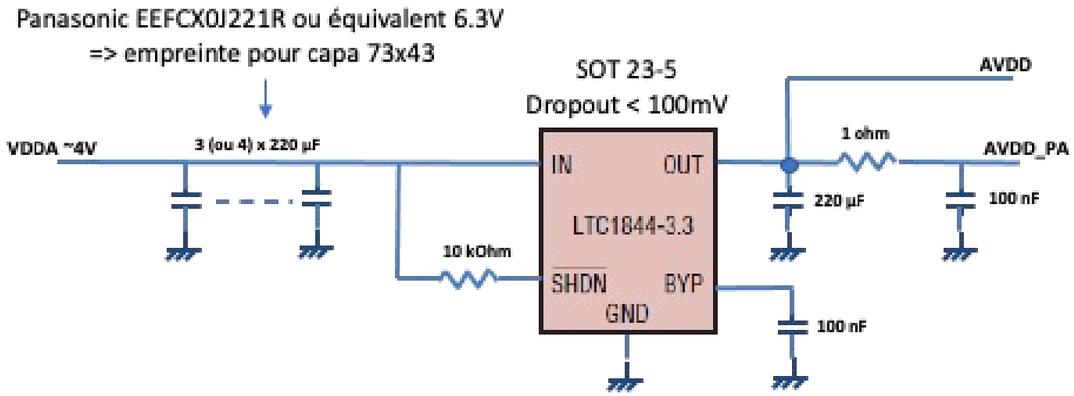
15 Slabs setup 02/06/21

coreKapton slot	Layer position	Slab ID	ASU type	wafer	front end (slboard ID)	Glissiere neded for the W	*W in front (mm)*	*X0*	*X0 (acc)*	Comments/Issues
14	0	31	FEV12	500						
13	1	30	FEV12	500						
12	2	13	FEV11	320	10	2.1mm	*2.1*	*0.6*	*0.6*	
11	3	14	FEV11	320	5	2.1mm	*2.1*	*0.6*	*1.2*	
10	4	15	FEV10	320	1	2.1mm	*2.1*	*0.6*	*1.8*	
9	5	19	FEV11	320	13	2.1mm	*2.1*	*0.6*	*2.4*	
8	6	20	FEV11	320	11	2.1mm	*2.1*	*0.6*	*3*	
7	7	24	FEV12	500	7	2.1mm	*2.1*	*0.6*	*3.6*	Stable AVDD ??
6	8	21	FEV11	320	14	2.1mm	*2.1*	*0.6*	*4.2*	
5	9	25	FEV12	500	3	2.1mm	*2.1*	*0.6*	*4.8*	problems communicating the ID of the SLboard ?? (SOLVED)
4	10	22	FEV11	320	4	4.2mm	*2.1*	*0.6*	*5.4*	
3	11	23	FEV10	320	6	4.2mm	*4.2*	*1.2*	*6.6*	
2	12	16	FEV11	320	9	2.1mm	*2.1*	*0.6*	*7.2*	
1	13	17	FEV11	320	2	4.2mm	*4.2*	*1.2*	*8.4*	problems communicating the ID of the SLboard ?? (SOLVED) Stable consumption ?? --> SOLVED shorcut in DVDD (capacitance in skiroc 14)
0	14	18	FEV11	320	0	whatever (no W will be added)	*4.2*	*1.2*	*9.6*	

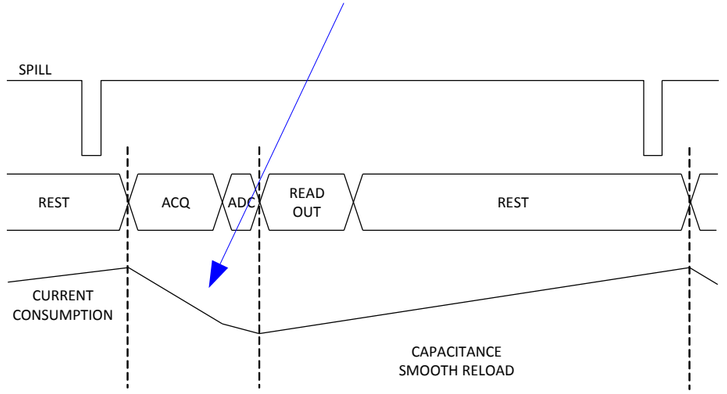
New FEV2.0 et al.

Status after regular discussions between engineers of LLR, IJCLab, LPNHE and OMEGA





With 600 µF, we ensure 100mA during 3ms with a voltage drop of 0.5V (ΔV = I.t/C).



- New board for next step of technical realisation of power pulsed Ecal layers
  - Capacitances and LDO close to ASICs
- Last month progress in design
  - Stacking of PCB
  - Choice of components
- Another important feature is that HV will be transported via connectors (i.e. On top of board
  - Wafer supply from bottom of board via plies (copper/kapton)
  - These plies are a delicate piece
  - Risk of shortcuts and wafer damage (the design of the kapton that goes below the board requires another design round)
- Expect production either shortly before or shortly after the summer break (not in a hurry, carefulness comes before speed)
- The setup will be completed by a “Termination card” that will allow for flexible chaining of cards (i.e. No soldering of terminations)
- and for flexible adding of decoupling capacitances (to study noise behaviour of COBs)