Test Beam DESY@2022/03

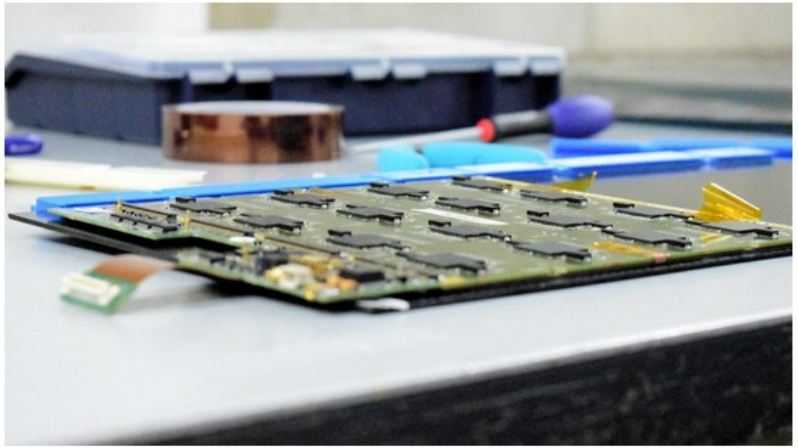
Adrián Irles*
on behalf the SiW-ECAL team

*AITANA group at IFIC – CSIC/UV

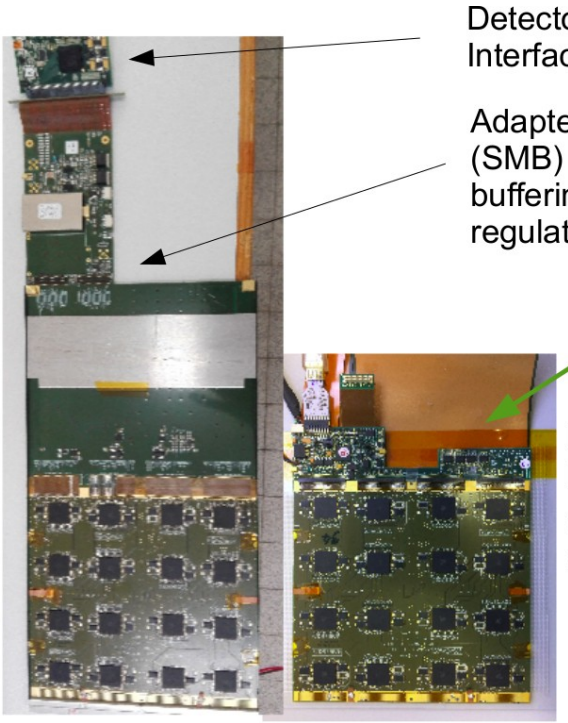
Outline

- Testing 15 stack with 15k readout cells
- New ultra compact DAQ able to cope with the complexity of having 15k readout cells
  - See J. Maalmi's talk
- Commissioning of the setup
  - See R. Poeschl's talk
- This talk (some selected results from the SiW-ECAL pre-CALICE meeting)
  - Technical tests (hold-scan, different gains…)
  - A brief overview of the layer performance (single cell performance)
  - First showers

Test Beam DESY 2021-22



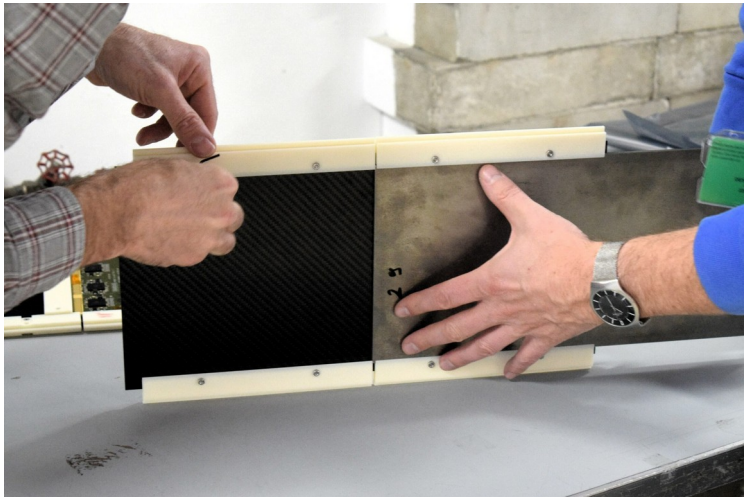
Test Beam setup

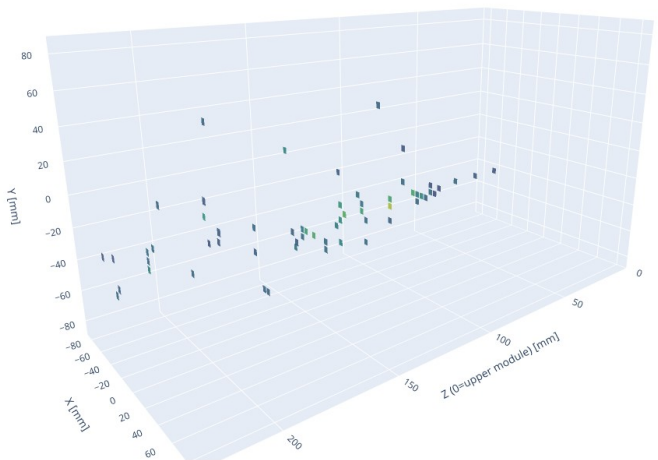


- **4 layers are "resurrected"**
  - Not operative before for different reasons
- **9 more layers have been "rebuild" → to adapt them to the new ultracompact DAQ**
- **4 new layers**
  - 2 of them with sensors glued in two separated batches (one sensor for test, the other 3 one year later)

Test Beam

- **DESY offers non-spilled beams of 1-6GeV (e-, e+)**
- **15 layers with 1024 readout cells each**
  - More than any LHC calorimeter
  - But it fits in a suitcase
- **4 weeks in total**
- ~3 weeks of commissioning and “training”
  - Mechanical structure (adding or removing the tungsten plates)
  - New and continuously improving DAQ and online monitoring tools
  - New semi-online monitoring tools
  - Hold values, gain optimization, Threshold optimization, single cell calibration, etc





Run summary

- Work in progress
- Runs with and without tungsten
- Pedestal Runs
- Holdscan runs (TB2021)
- Different gains
- Threshold optimization
- etc

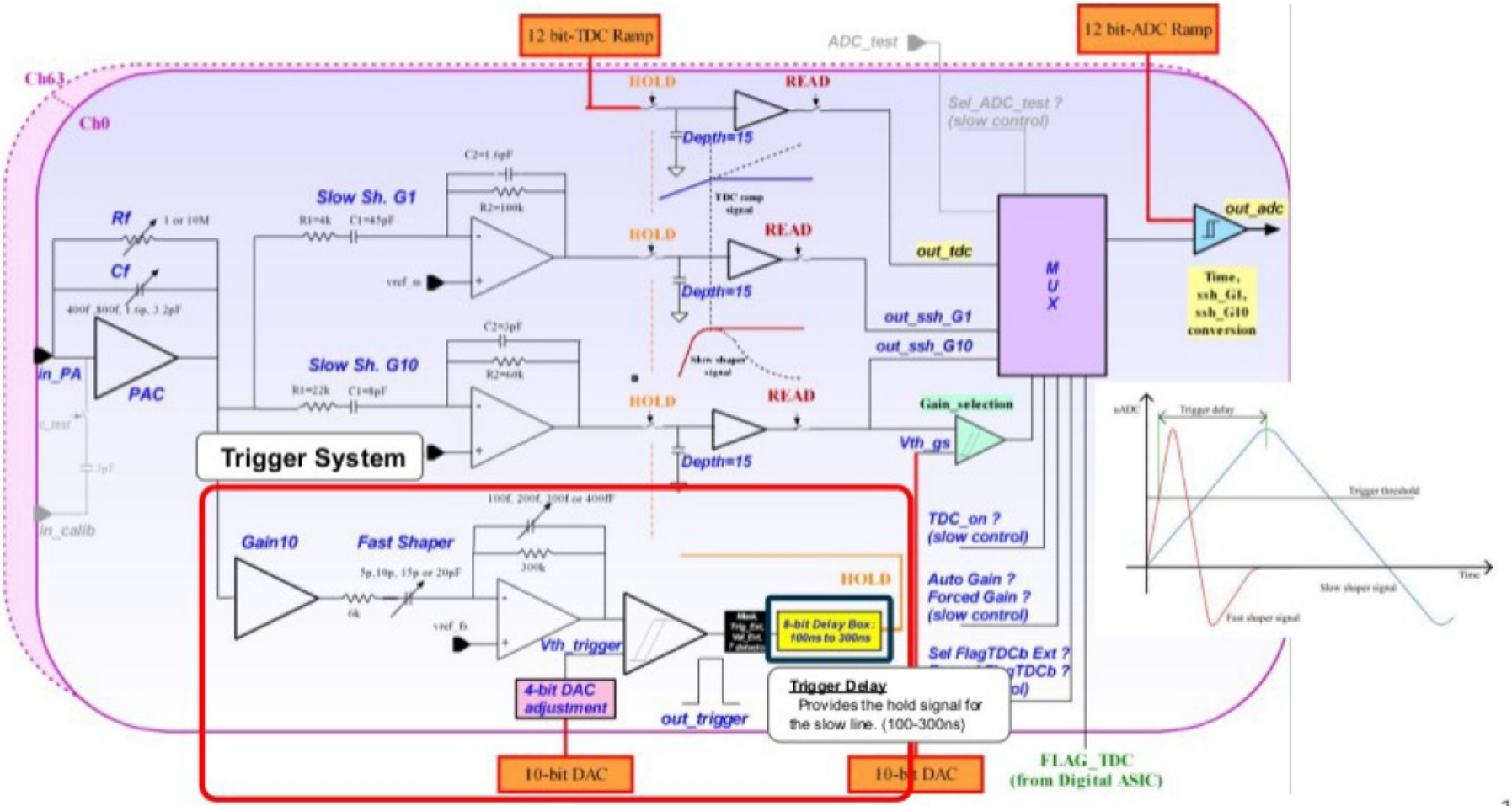
run#	type	pos x	pos y	window, delay (ms)	Beam rate/hz	Slab 0 rate/Hz	Stat Offline	stat slab 0 kHits	length / mins	start time	Rem
050270	3.0 GeV	-130.1	+26.9	1, 10	20 Hz	250	31000	7.788	5	17:05	Cycle ~ 70/s; 10Mbits/s Frames = ??
050271	3.0 GeV	-130.1	+26.9	1, 4	20 Hz	350	38470	10.953	5	17:11	Cycle ~ 125/s; 14Mbits/s 37903 cycles, 55398 frames
050272	3.0 GeV	-130.1	+26.9	1, 2	20 Hz	400	44620	12.560	5	17:16	Cycle ~ 180/s; 16Mbits/s 57579 cycles, 57912 frames
050273	3.0 GeV	-130.1	+26.9	1, 19	20 Hz	175	3024	3.560	5	17:25	Cycle ~ 40/s; 7Mbits/s 12402 cycles, 23206 frames
050274	3.0 GeV	-130.1	+26.9	2, 2	20 Hz	500	19350	10.572	5	17:33	Cycle ~ 120/s; 20Mbits/s 37903 cycles, 55398 frames but saturations everywhere ! (see plots)
050275	3.0 GeV	-130.1	+26.9	4, 2	20 Hz	600	56190	8.494	5	17:39	Cycle ~ 80/s; 24 Mbits/s 61707 cycles, 22320 frames but saturations everywhere (flat distrib)
050276	3.0 GeV	-130.1	+26.9	2, 2	12 Hz	350	65800	6.798*0.7	5	18:19	Cycle ~100 /s; 15 Mbits/s 36446 cycles, 67533 frames tres peu de saturation (max in slab 6 ~ 250/(14*750) = 2%
050277	3.0 GeV	-130.1	+26.9	1, 2	12 Hz	300		9.363*0.5	5	18:19	Cycle ~200 /s; 12 Mbits/s 58634 cycles, 72657 frames

Beam position

- 3.0GeV_W_Pos-130+27_run_050278
- COB mapping was now fixed for chip 15.

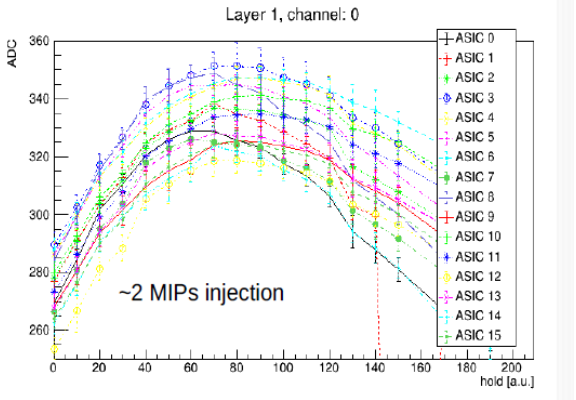
run#	type	pos x	pos y	Window, delay	Beam rate/hz	Slab 0 rate/Hz	stat slab 0 kHits	length / mins	start time	Rem
	3.0 GeV	-89.9	+26.9	2,2	20 Hz					lower right corner = slab 2, pad (16,8)
run_050278	3.0 GeV	-130.1	+26.9	2,2	12 Hz	400		72	19:26	lower left corner = slab 2, pad (8,8)
run_050279	3.0 GeV	-35.0	+112.5	2,2	12 Hz	(slab2) 600			21:30	Upper right corner
	3.0 GeV	-130.1	+112.5	2,2	20 Hz					Upper left corner

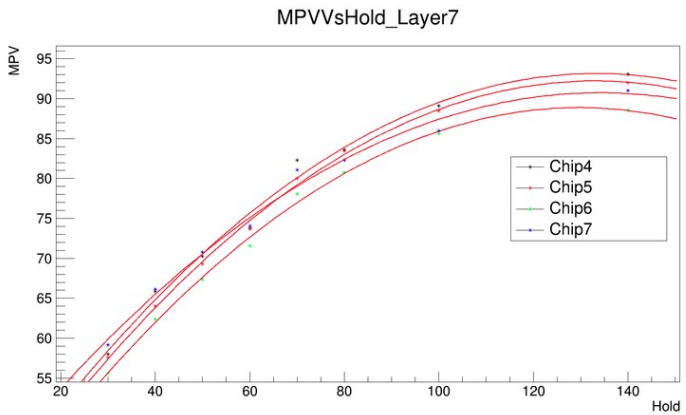
hold-scans

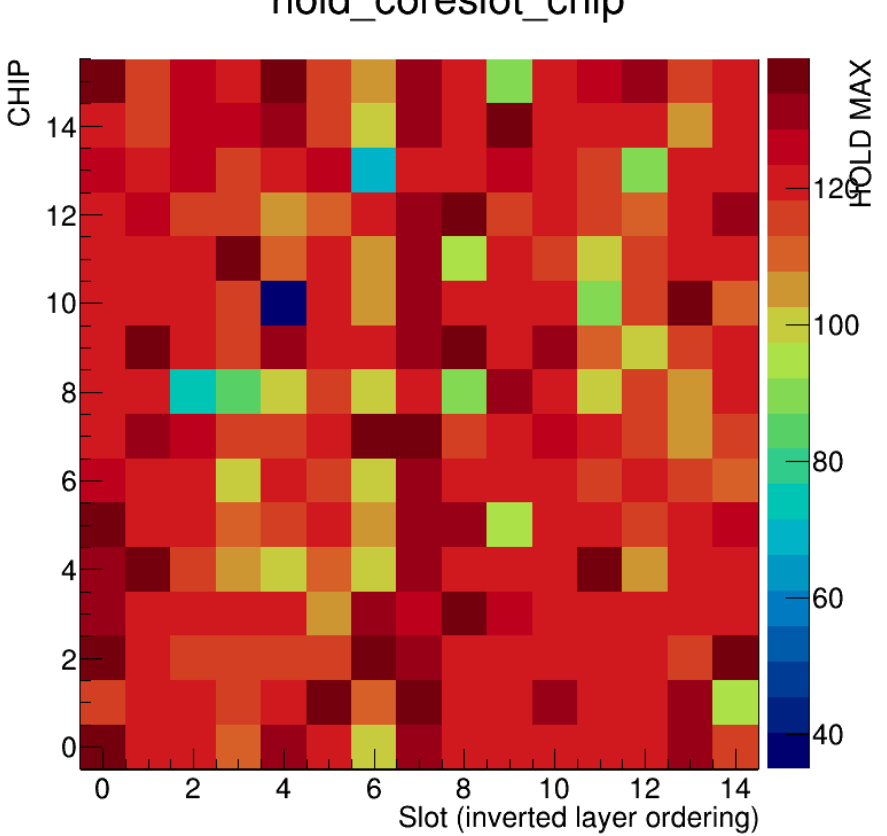

12 bit-TDC Ramp
ADC_test
12 bit-ADC Ramp
Ch63
Ch0
HOLD
READ
Depth=15
Sel_ADC_test ?
(slow control)
Slow Sh. G1
Rf
Cf
in_PA
PAC
in_calib
TDC ramp signal
out_tdc
out_adc
MUX
Time, ssh_G1, ssh_G10 conversion
out_ssh_G1
out_ssh_G10
Slow Sh. G10
Slow shaper signal
Gain_selection
Vth_gs
Trigger System
Gain10
Fast Shaper
Vth_trigger
TDC_on ?
(slow control)
Auto Gain ?
Forced Gain ?
(slow control)
8-bit Delay Box: 100ns to 300ns
Sel FlagTDCb Ext ?
4-bit DAC adjustment
out_trigger
Trigger Delay
Provides the hold signal for the slow line. (100-300ns)
10-bit DAC
10-bit DAC
FLAG_TDC
(from Digital ASIC)
sADC
Trigger delay
Trigger threshold
Time
Slow shaper signal
Fast shaper signal

hold-scans

- Done at the lab with pulses… quite different results compared with beam







Single cell calibration

- Two set of gains used:
  - LowElectrons Gains (or DESY gains) = 1.2pF for 320um wafers and 0.8pF for 500 and 650um wafers
  - ILCElectrons (or CERN gain) = 6pF
- For the DESY gain,
  - Pedestal and mip calibrations are estimated for the high and low branches
- For the CERN gain
  - only the high gain branch

layer position	SLABs before 01/04/2022	Slabs from 01/04/2022 ownards
0	34 fev13 650um	20 (fev11)
1	35 fev13 650um	21 (fev11)
2	33 cob 500um	34 fev13 650um
3	29 cob 500um	35 fev13 650um
4	19 (fev11) 320um	19 (fev11) 320um
5	20 (fev11) 320um	33 cob 500um
6	21 (fev11) 320um	29 cob 500um
7	30 fev12 500um	30 fev12 500um
8	31 fev12 500um	31 fev12 500um
9	24 fev12 500um	24 fev12 500um
10	25 fev12 500um	25 fev12 500um
11	22 (fev11) 320um	22 (fev11) 320um
12	18 (fev11) 320um	18 (fev11) 320um
13	23 (fev10) 320um	23 (fev11) 320um
14	17 (fev11) 320um	17 (fev11) 320um

Single cell calibration

- Two set of gains used:
  - **LowElectrons Gains (or DESY gains) = 1.2pF for 320um wafers and 0.8pF for 500 and 650um wafers**
  - ILCElectrons (or CERN gain) = 6pF
- For the DESY gain,
  - Pedestal and mip calibrations are estimated for the high and low branches
- For the CERN gain
  - only the high gain branch

layer position	SLABs before 01/04/2022	Slabs from 01/04/2022 ownards
0	34 fev13 650um	20 (fev11)
1	35 fev13 650um	21 (fev11)
2	33 cob 500um	34 fev13 650um
3	29 cob 500um	35 fev13 650um
4	19 (fev11) 320um	19 (fev11) 320um
5	20 (fev11) 320um	33 cob 500um
6	21 (fev11) 320um	29 cob 500um
7	30 fev12 500um	30 fev12 500um
8	31 fev12 500um	31 fev12 500um
9	24 fev12 500um	24 fev12 500um
10	25 fev12 500um	25 fev12 500um
11	22 (fev11) 320um	22 (fev11) 320um
12	18 (fev11) 320um	18 (fev11) 320um
13	23 (fev10) 320um	23 (fev11) 320um
14	17 (fev11) 320um	17 (fev11) 320um

covariance matrix method

https://arxiv.org/pdf/1401.7095.pdf

Coherent noise source identification in multi channel analysis

T. Frisson*[1] and R. Poeschl[1]

[1]Laboratoire de L'accélerateur Linéaire (LAL), CNRS/IN2P3, Orsay, France

May 4, 2021

- "The goal is to identify and characterize dissociable noise sources in a multi channel systems. This method cannot separated noise sources which affect exactly the same set of channels. In this case, the noises sources are processed as a single source. We consider a system with N channels. "
- "Each channel **k** is affected by an incoherent noise source **I_k** and Nc coherent noise sources (**C1_k, C2_k,... CN_k**). We assume that all noise source distributions are Gaussian and independant."

covariance matrix method

$$\sigma_i^2 = \sigma_{I_i}^2 + \sum_{j=1}^{N_c} \sigma_{C_i^j}^2 \tag{1}$$

The covariance matrix element from the two channels i and k is expressed by:

$$cov(i,k) = \delta_{ik}\sigma_{I_i}\sigma_{I_k} + \sum_{j=1}^{N_c} \sigma_{C_i^j}\sigma_{C_k^j} \tag{2}$$

where:

$$\delta_{ik} = \begin{cases} 1 & \text{if } i = k \\ 0 & \text{if } i \neq k \end{cases} \tag{3}$$

The covariance matrix element can also be determined from the data:

$$cov_{Data}(i,k) = \frac{\sum_{n=1}^{N_{event}} (A_i(n) - \mu_{A_i})(A_k(n) - \mu_{A_k})}{N_{event}} \tag{4}$$

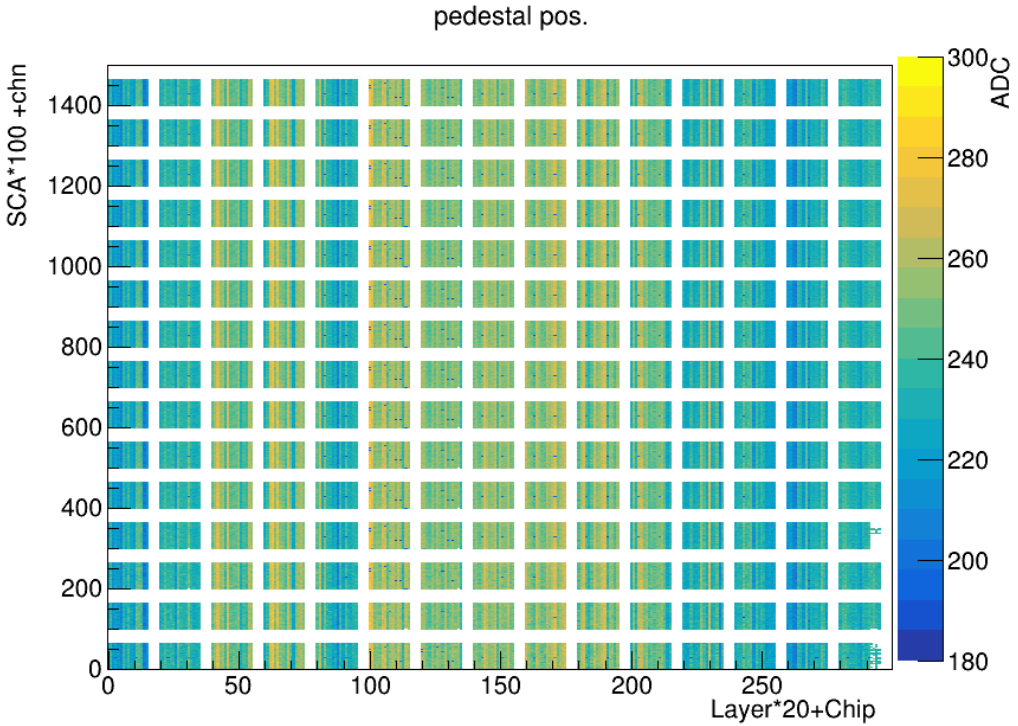
Measured amplitud if no hit

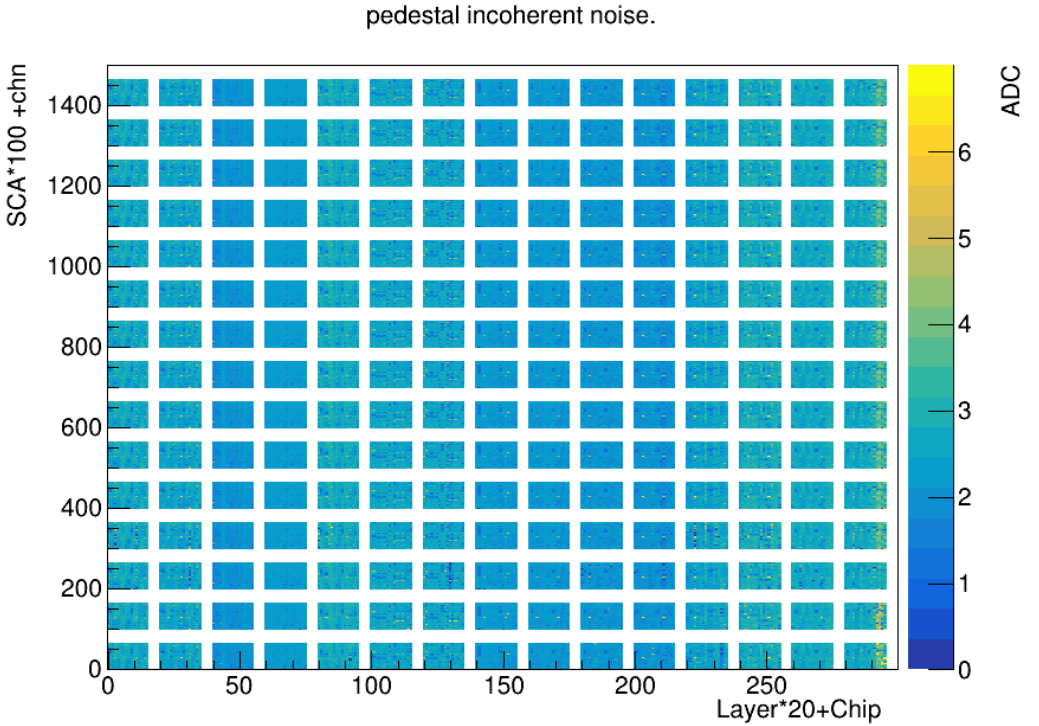
Pedestal position → calculated as simple histogram Mean

covariance matrix method

- The average pedestal is calculated on the fly
  - No gaussian fit is performed
- Following same recipe than in the CALICE note, we get the convergence with 2 coherent noises

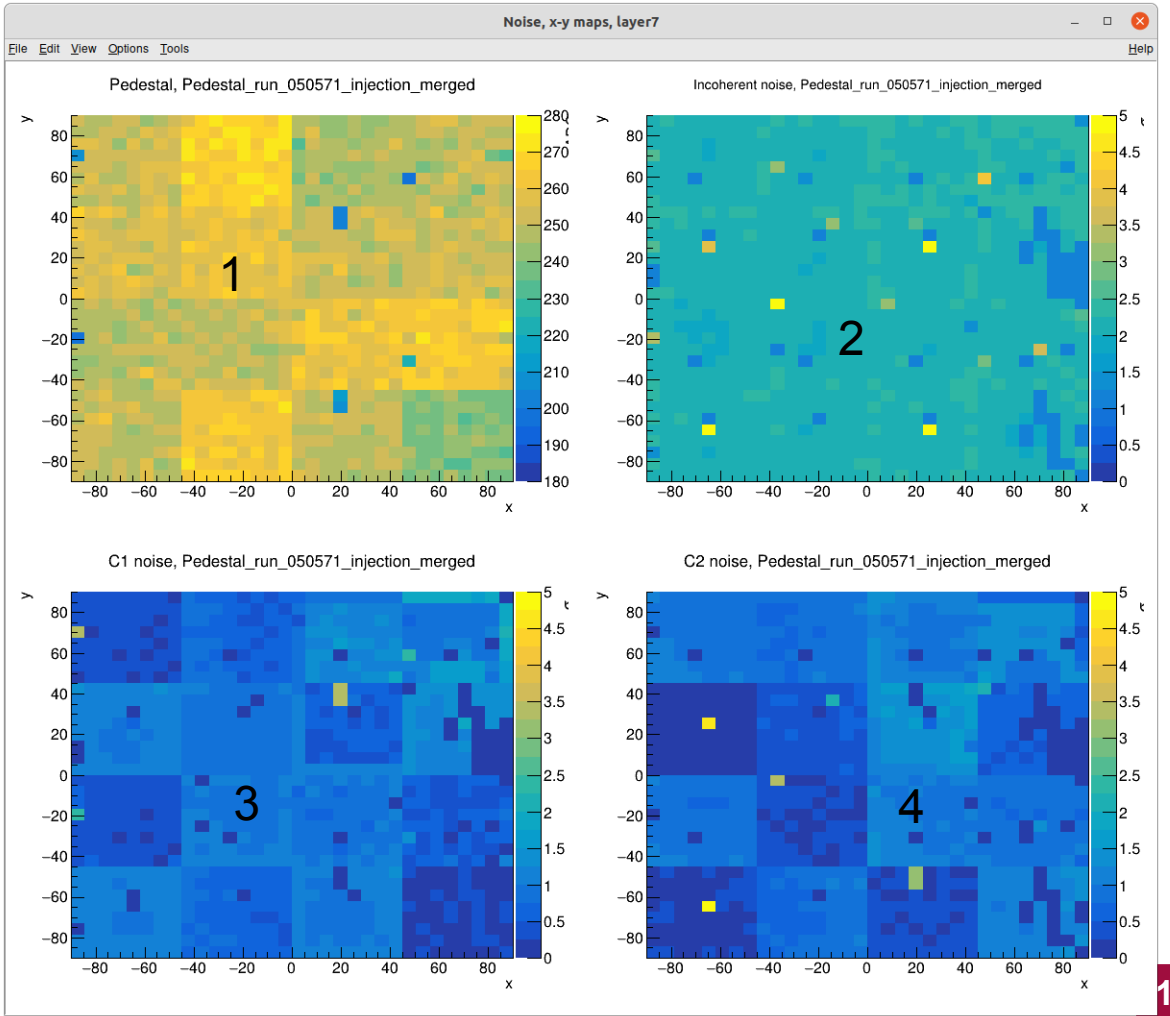
Pedestal position and incoherent noise



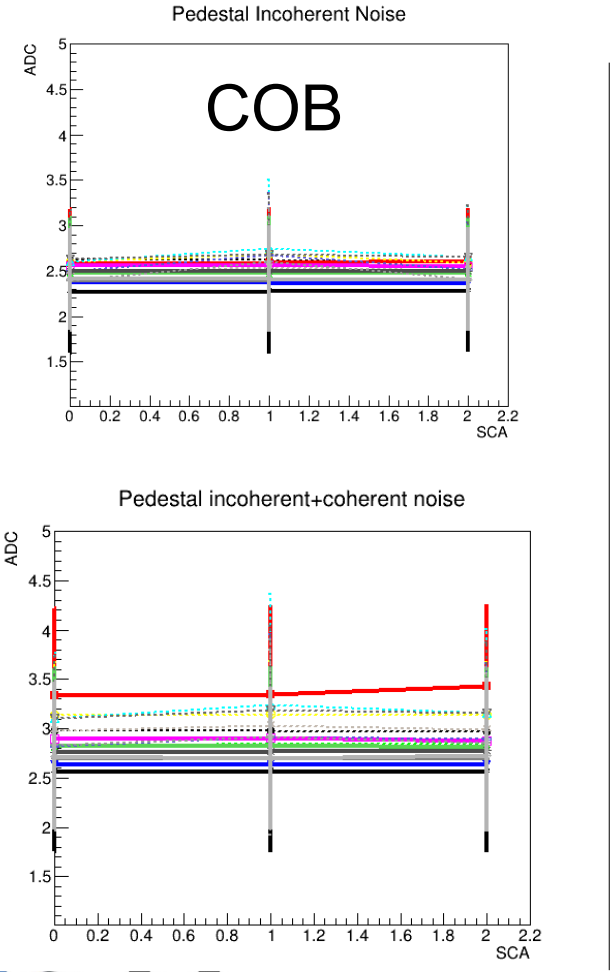


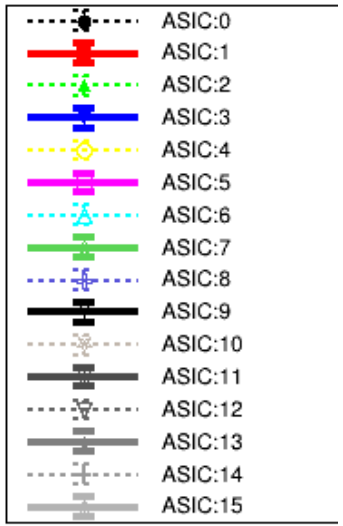
Layer 7, slab30 FEV12 sk2a, 500um (reference slab)

- 1) Pedestal map
  - Few channels are off
  - These are usually seen as noise sources (FEV10/11/22)
- 2) Incoherent noise map
  - The masked channels (37 plus more) have lower widths
  - Some near 37 channels have large noise contributions
- 3) coherent noise map (c1)
- 4) coherent noise map (c2)

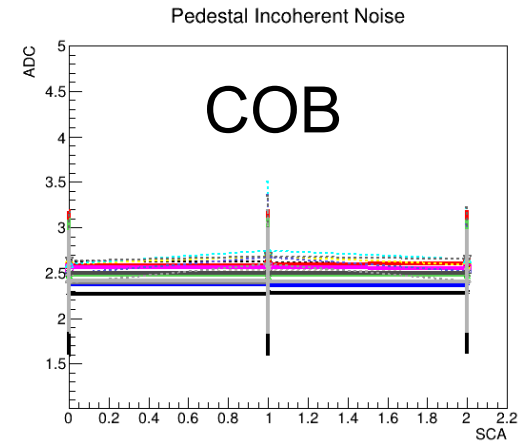


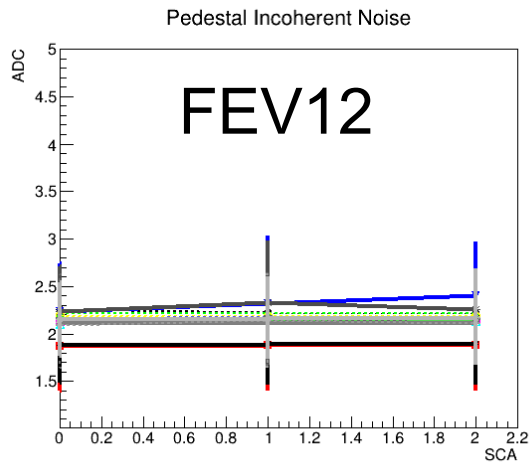
COB vs BGA

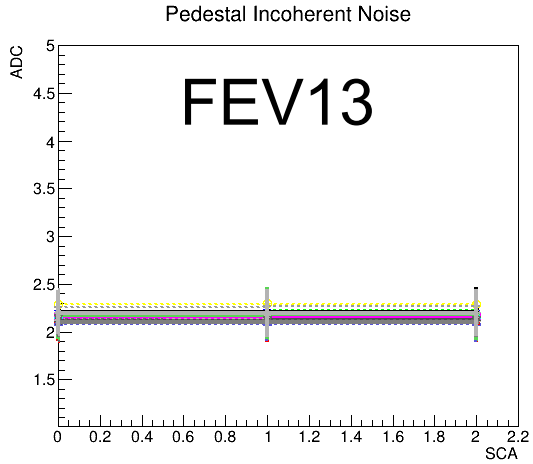

Pedestal Incoherent Noise
COB
ADC
SCA
Pedestal incoherent+coherent noise
ADC
SCA

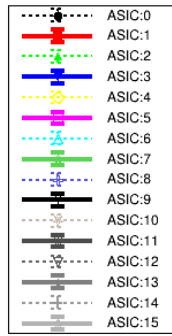

ASIC:0
ASIC:1
ASIC:2
ASIC:3
ASIC:4
ASIC:5
ASIC:6
ASIC:7
ASIC:8
ASIC:9
ASIC:10
ASIC:11
ASIC:12
ASIC:13
ASIC:14
ASIC:15

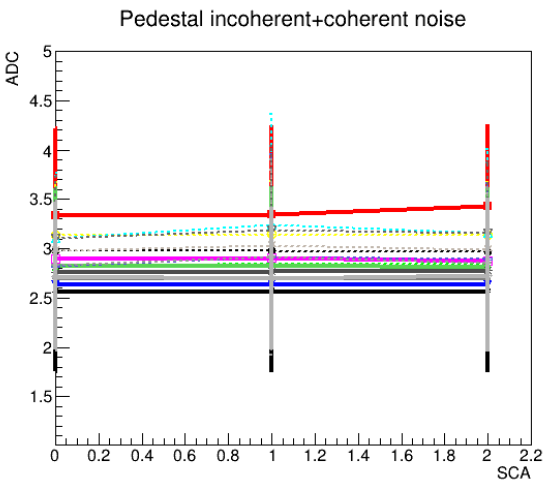
COB vs BGA

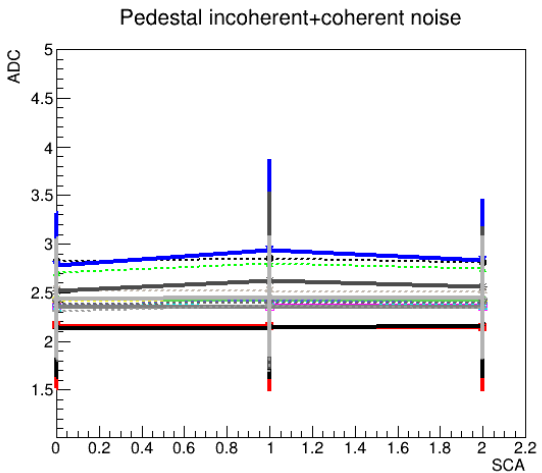

Pedestal Incoherent Noise
COB
ADC
SCA

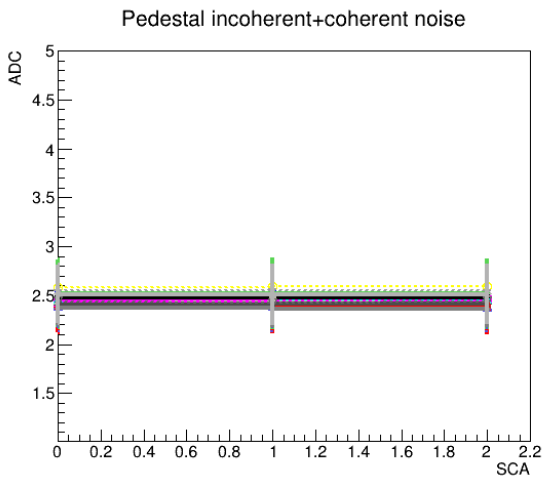

Pedestal Incoherent Noise
FEV12
ADC
SCA


Pedestal Incoherent Noise
FEV13
ADC
SCA


ASIC:0
ASIC:1
ASIC:2
ASIC:3
ASIC:4
ASIC:5
ASIC:6
ASIC:7
ASIC:8
ASIC:9
ASIC:10
ASIC:11
ASIC:12
ASIC:13
ASIC:14
ASIC:15

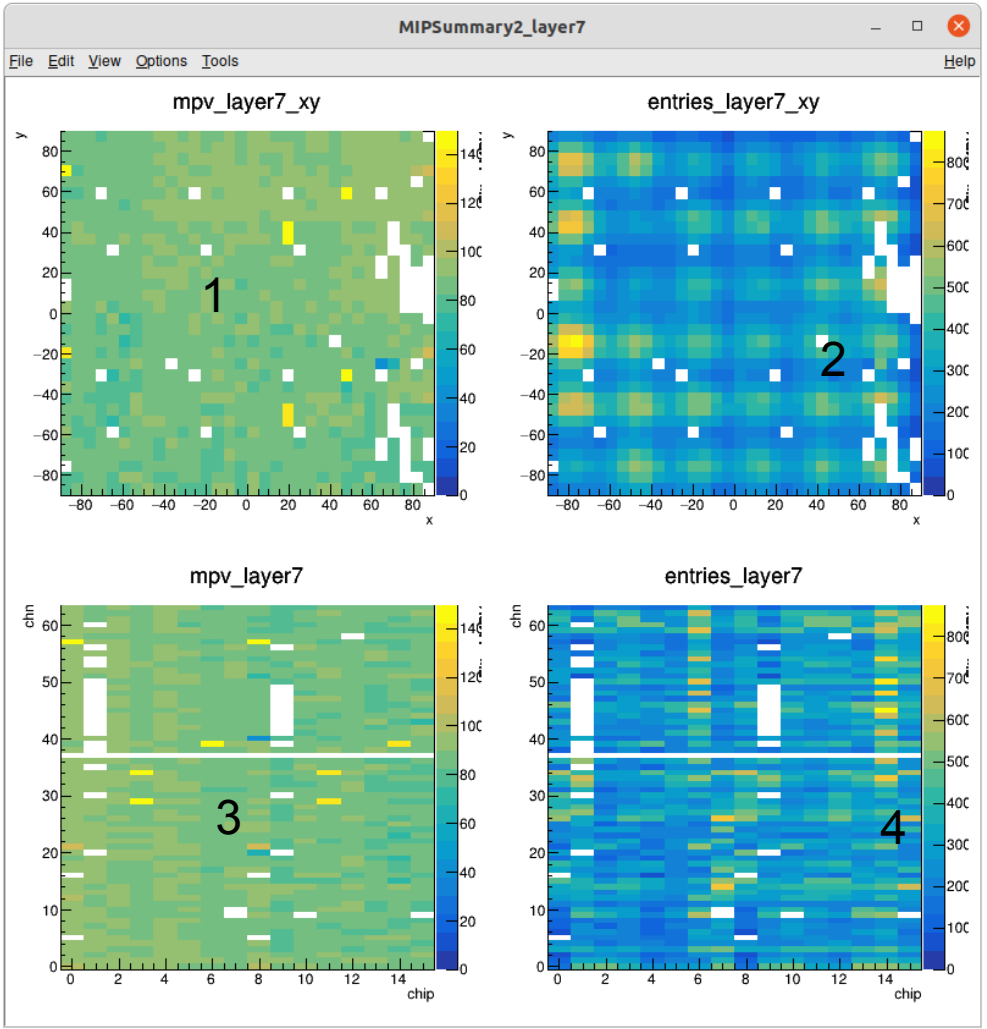

Pedestal incoherent+coherent noise
ADC
SCA


Pedestal incoherent+coherent noise
ADC
SCA


Pedestal incoherent+coherent noise
ADC
SCA

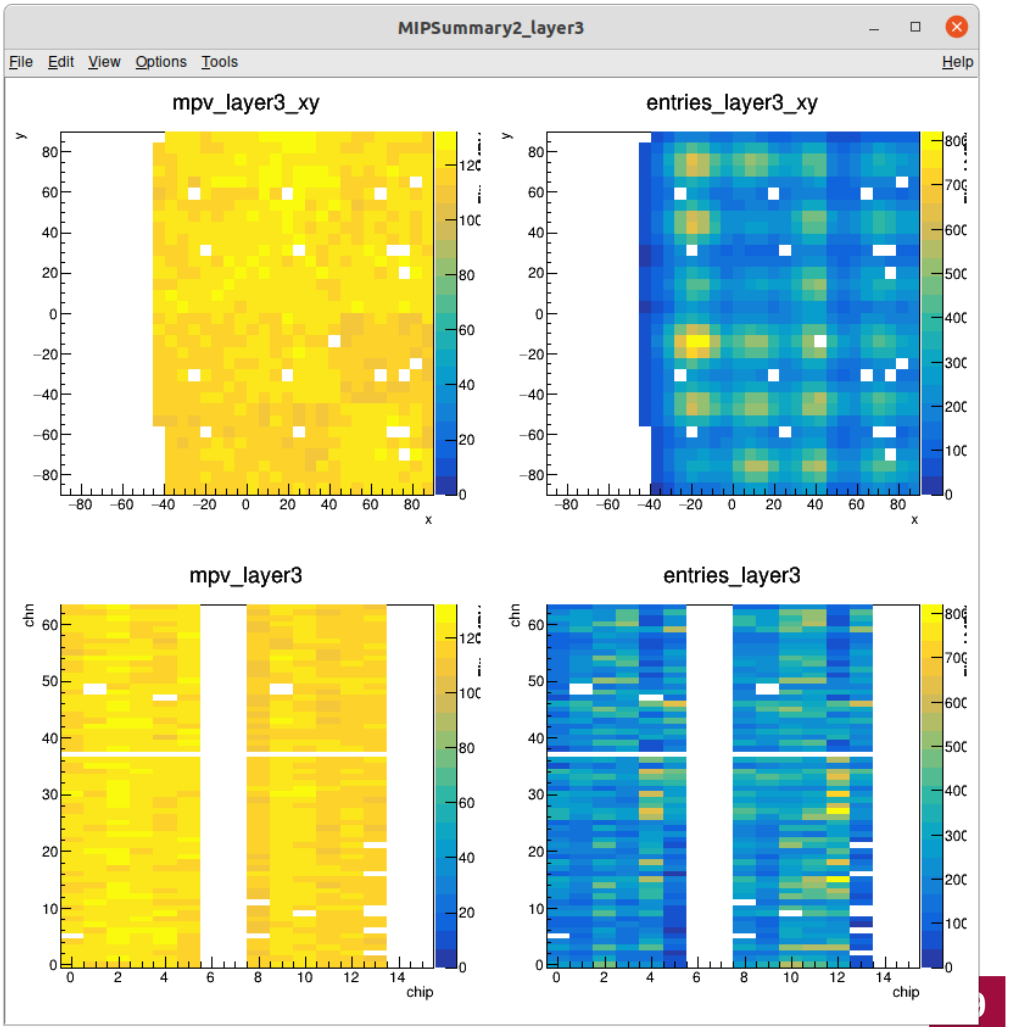
Layer 7, slab30 FEV12 sk2a, 500um (reference slab)

- 1) MPV value (fit to landau+gaussian)
- 2) Number of events in coincidence
  - Simple event building
  - 7 layers in coincidence (+-1 bcid)
- 3) & 4) the same bu in chip-chn instad of x-y



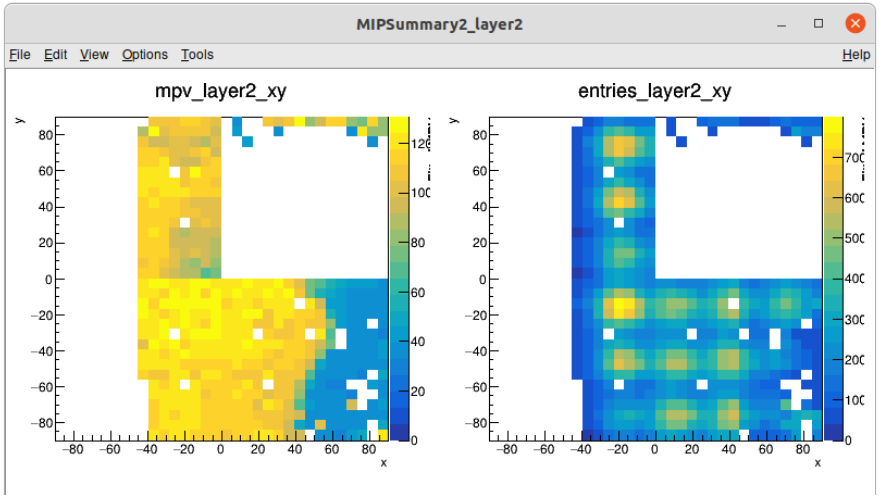
Few more plots

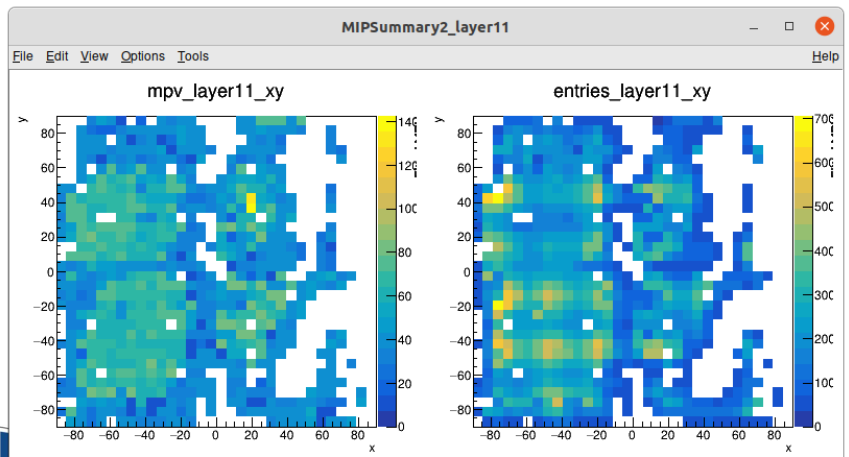
- The empty spaces are corners where we did not shoot the beam

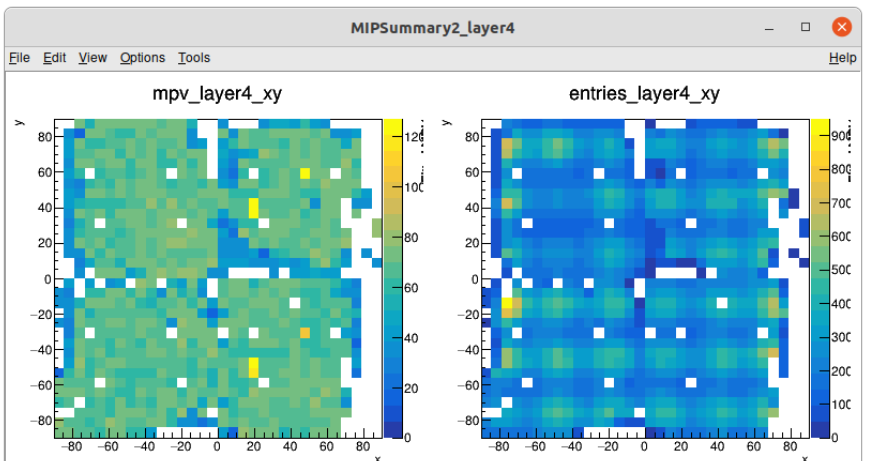


Few more plots

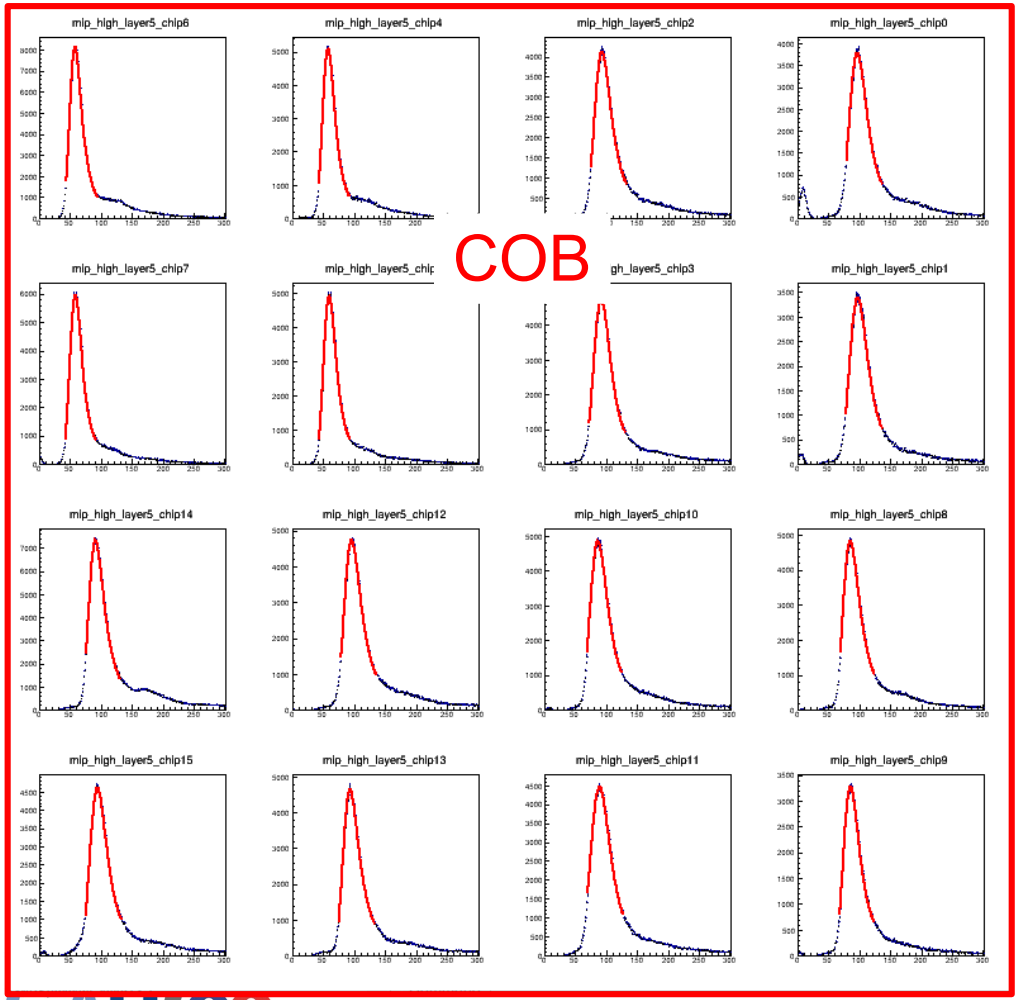
- Some slabs present problems...
  - Associated to detachment of wafers (glued)
  - Worrisome situation than is to be understood with high priority
  - ~1/3 of 15 slabs seem difficult to be recovered
  - Other slabs are in the pipeline (at least 3 equipped FEV13s + 2 new boards FEV12/COB/orFEV2.)

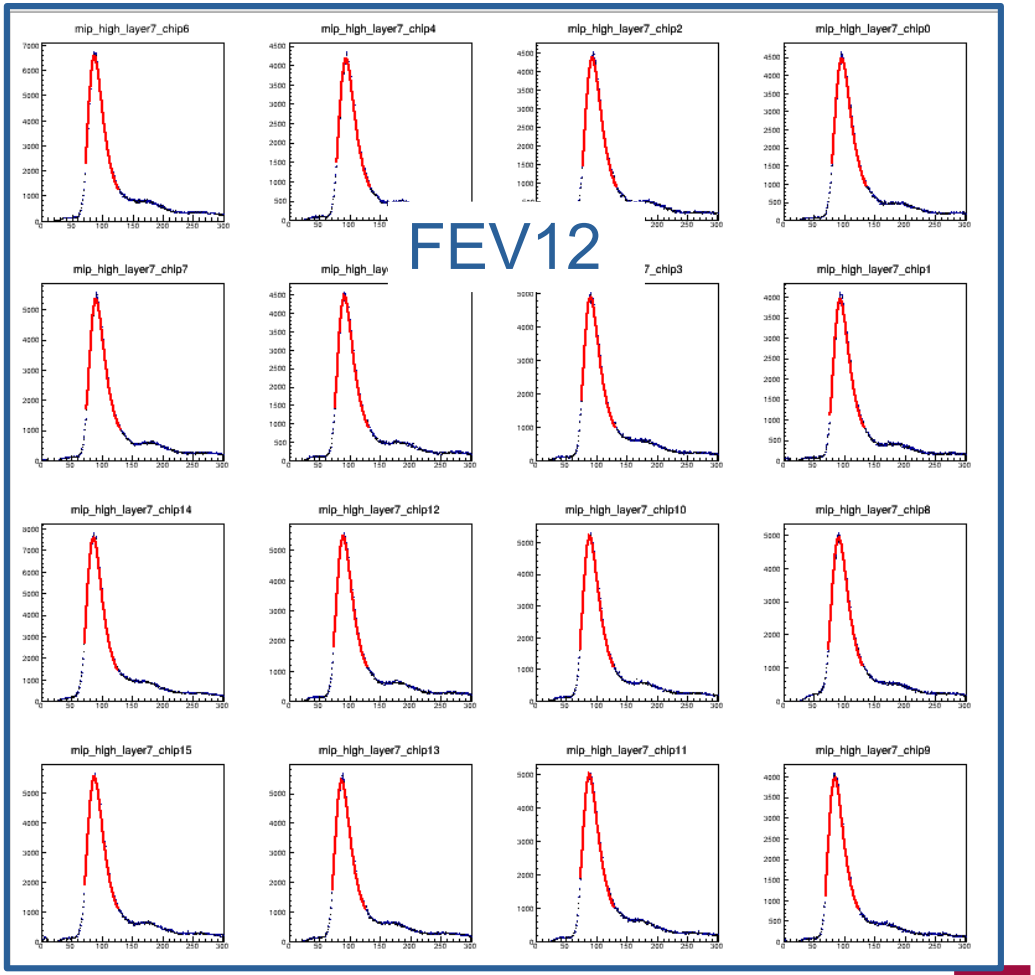






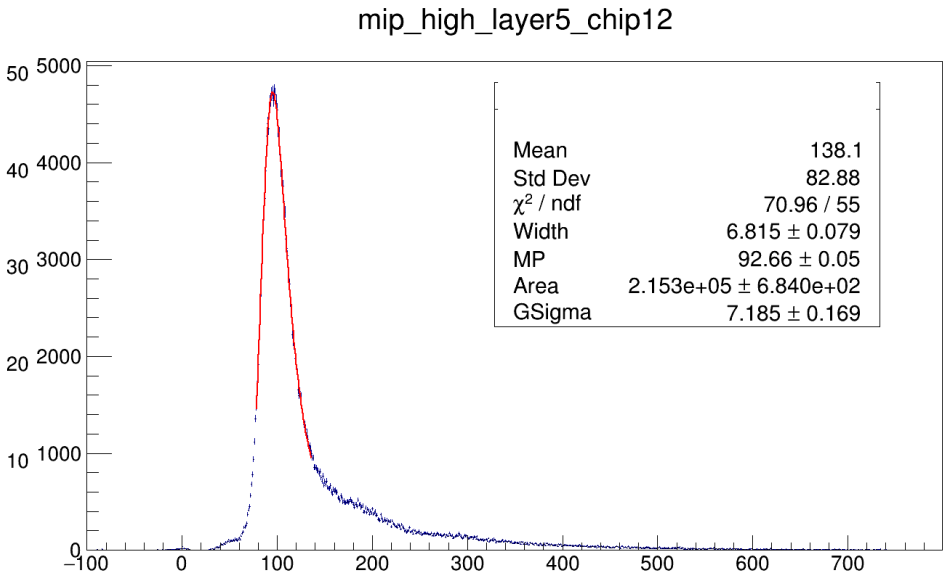
COB vs BGA


mip_high_layer5_chip6
mip_high_layer5_chip4
mip_high_layer5_chip2
mip_high_layer5_chip0
COB
mip_high_layer5_chip7
mip_high_layer5_chip3
mip_high_layer5_chip1
mip_high_layer5_chip14
mip_high_layer5_chip12
mip_high_layer5_chip10
mip_high_layer5_chip8
mip_high_layer5_chip15
mip_high_layer5_chip13
mip_high_layer5_chip11
mip_high_layer5_chip9

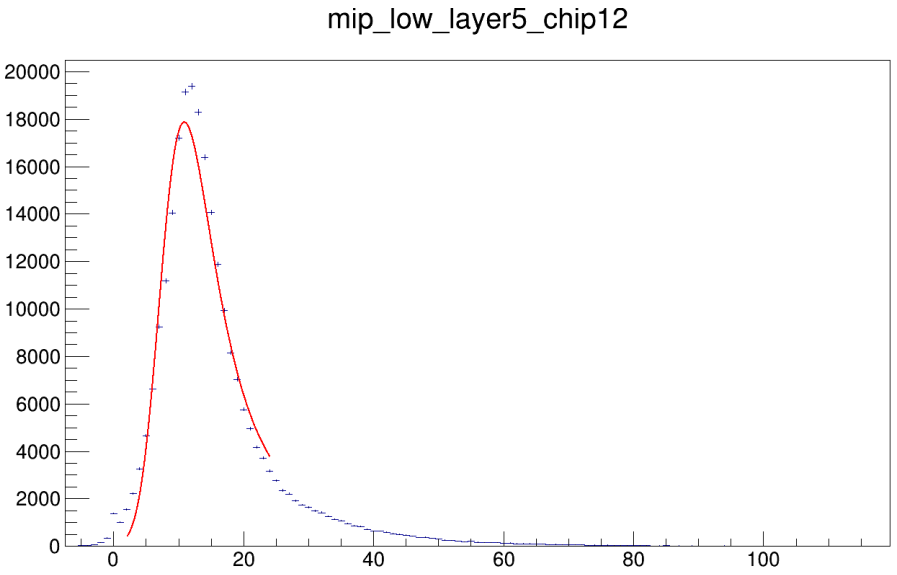

mip_high_layer7_chip6
mip_high_layer7_chip4
mip_high_layer7_chip2
mip_high_layer7_chip0
FEV12
mip_high_layer7_chip7
mip_high_layer7_chip1
mip_high_layer7_chip14
mip_high_layer7_chip12
mip_high_layer7_chip10
mip_high_layer7_chip8
mip_high_layer7_chip15
mip_high_layer7_chip13
mip_high_layer7_chip11
mip_high_layer7_chip9

DESY gain: high vs low branch gains

DESY gain high gain branch



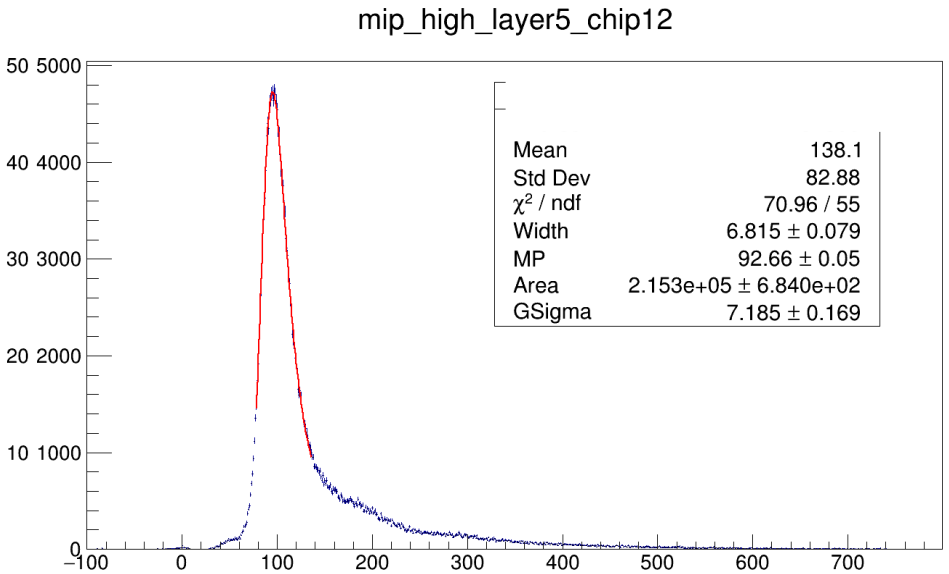
DESY gain low gain branch



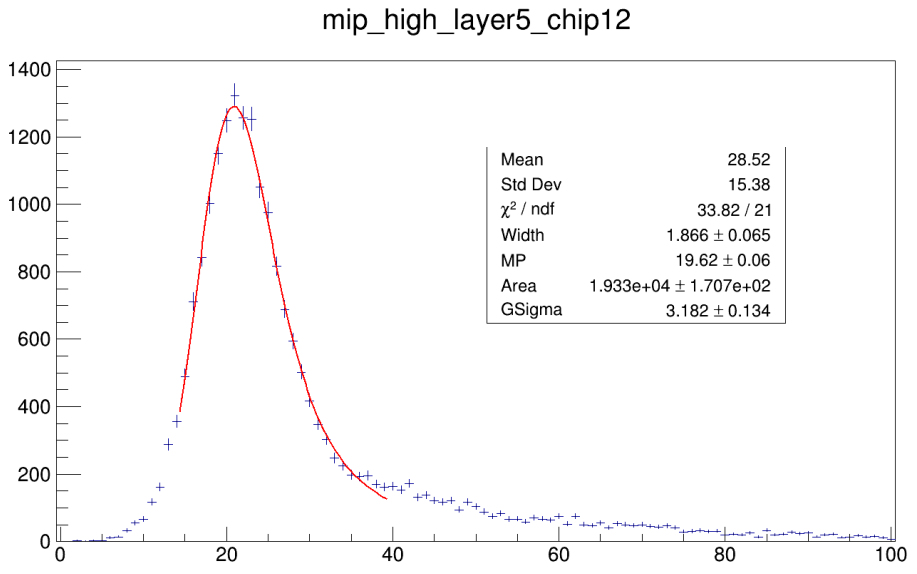
The low gain branch fits are not as optimal as the high gain...

DESY vs ILC gain

DESY gain
high gain branch



ILC gain
High gain branch



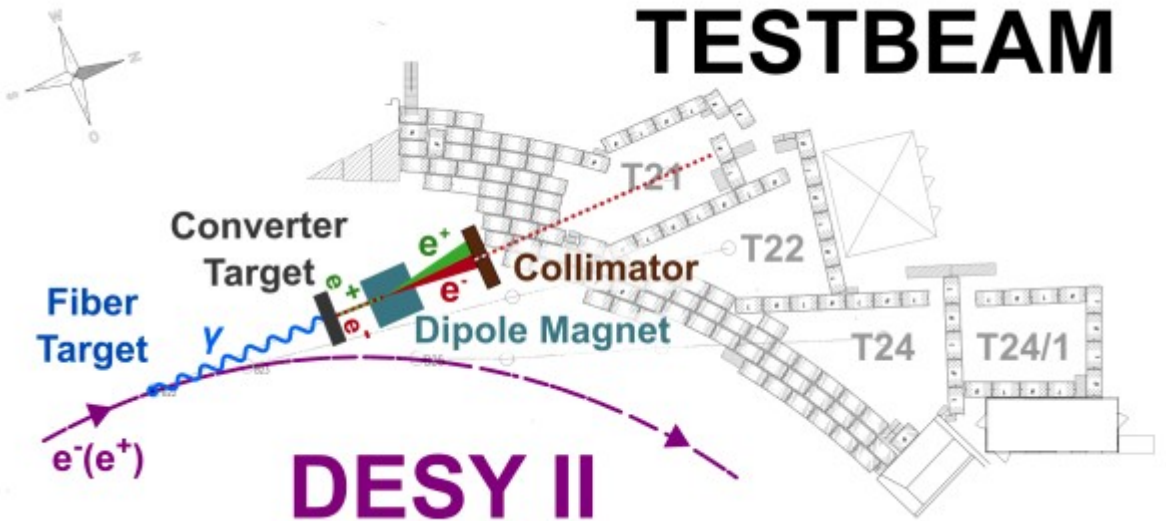
1.2pF vs 6pF ~ x4.73

Summary and outlook

- We had 4 weeks of training, commissioning and debugging with beam
  - **and data** for calibration and shower studies
  - See J. Kunath and Y. Okugawa's talks on friday (data) and F. Jimenez (simulation)
- Worrisome situation for ~1/3 of slabs related to gluing issues
  - To be understood
  - And to be replaced (for CERN)
- Next challenge: common running with AHCAL
  - See talk by J. Maalmi
  - Online DAQ based on EUDAQ.

Lucky to have you...

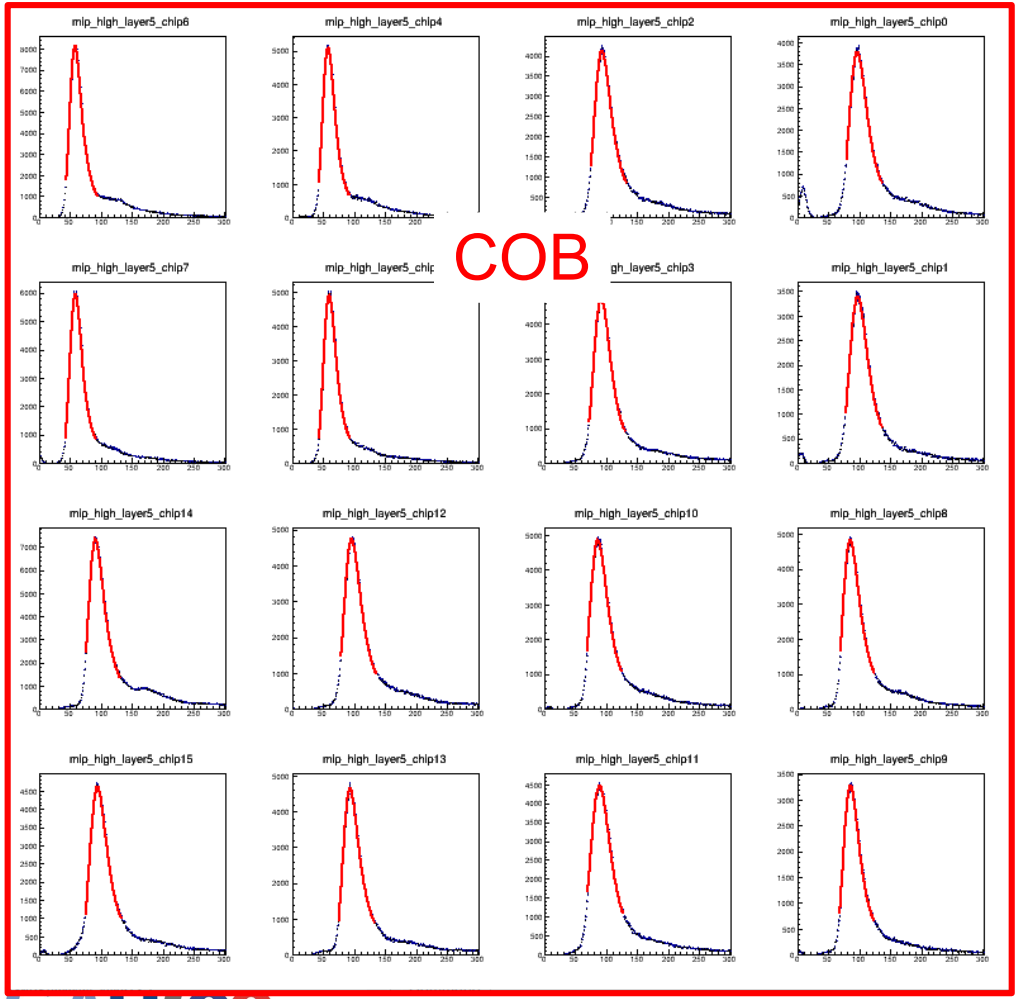
- Very strict sanitary requirements
  - But we are extremely happy of having access to beam time.
- Testbeams are crucial for our community
- Thanks!

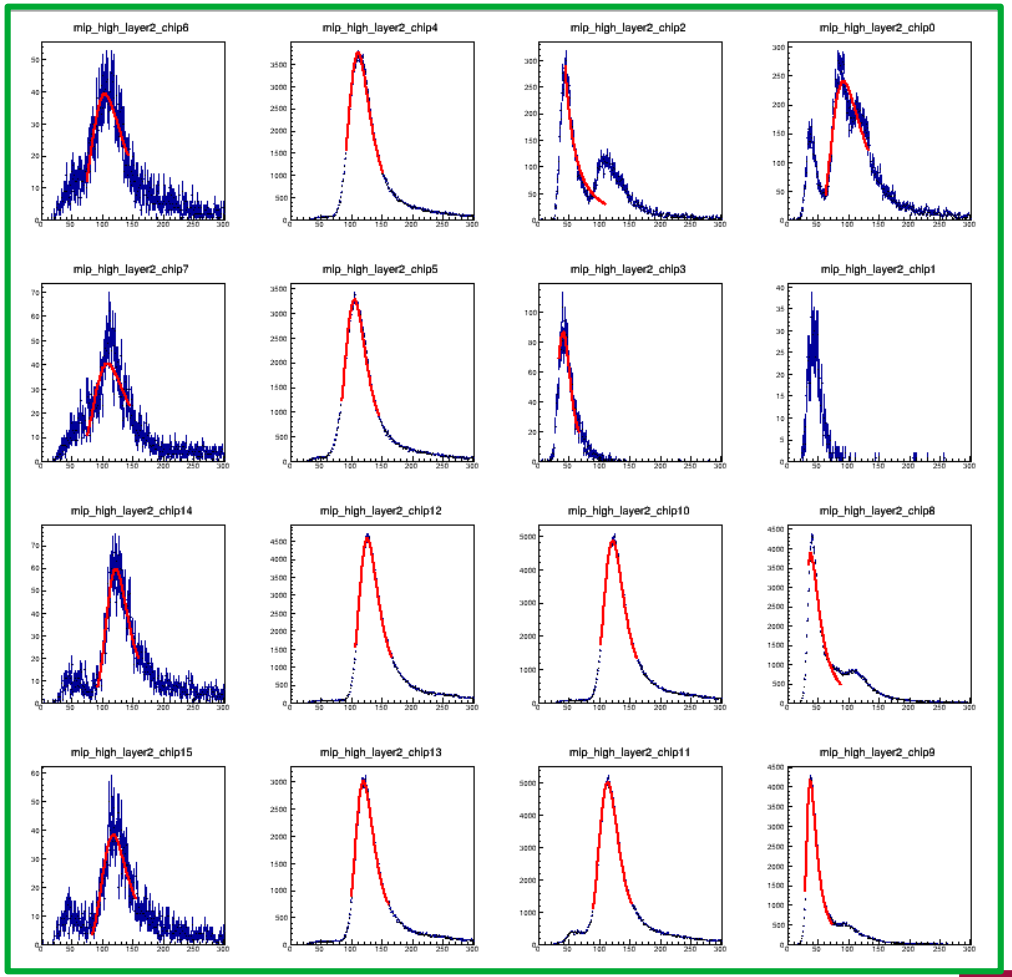


The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

back-up

COB vs BGA


mip_high_layer5_chip6
mip_high_layer5_chip4
mip_high_layer5_chip2
mip_high_layer5_chip0
COB
mip_high_layer5_chip7
mip_high_layer5_chip3
mip_high_layer5_chip1
mip_high_layer5_chip14
mip_high_layer5_chip12
mip_high_layer5_chip10
mip_high_layer5_chip8
mip_high_layer5_chip15
mip_high_layer5_chip13
mip_high_layer5_chip11
mip_high_layer5_chip9


mip_high_layer2_chip6
mip_high_layer2_chip4
mip_high_layer2_chip2
mip_high_layer2_chip0
mip_high_layer2_chip7
mip_high_layer2_chip5
mip_high_layer2_chip3
mip_high_layer2_chip1
mip_high_layer2_chip14
mip_high_layer2_chip12
mip_high_layer2_chip10
mip_high_layer2_chip8
mip_high_layer2_chip15
mip_high_layer2_chip13
mip_high_layer2_chip11
mip_high_layer2_chip9