# TPC Development by the LCTPC Collaboration for the ILD Detector at ILC (and other future colliders)

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for LCTPC

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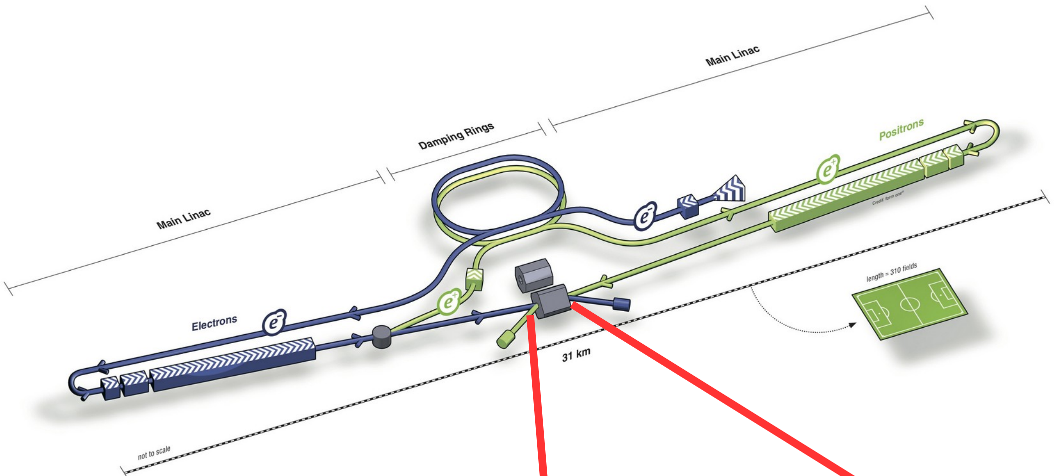
UNIVERSITÄT BONN

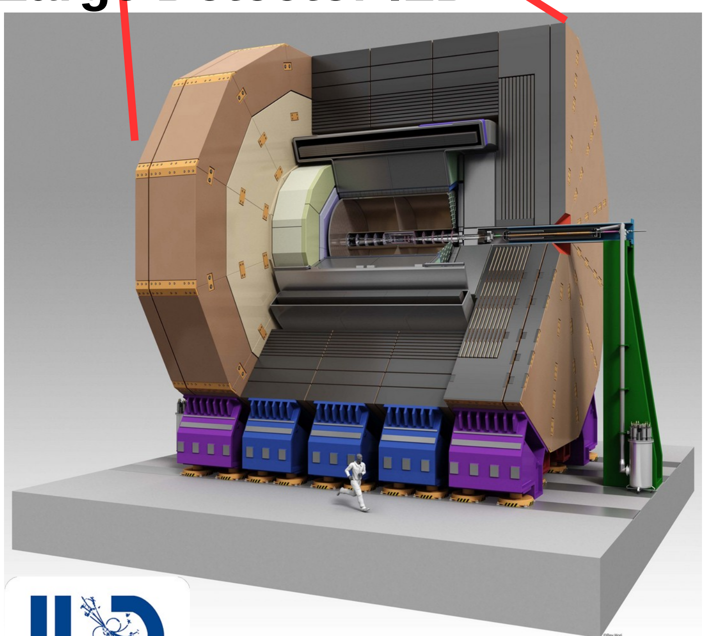
# International Linear Collider

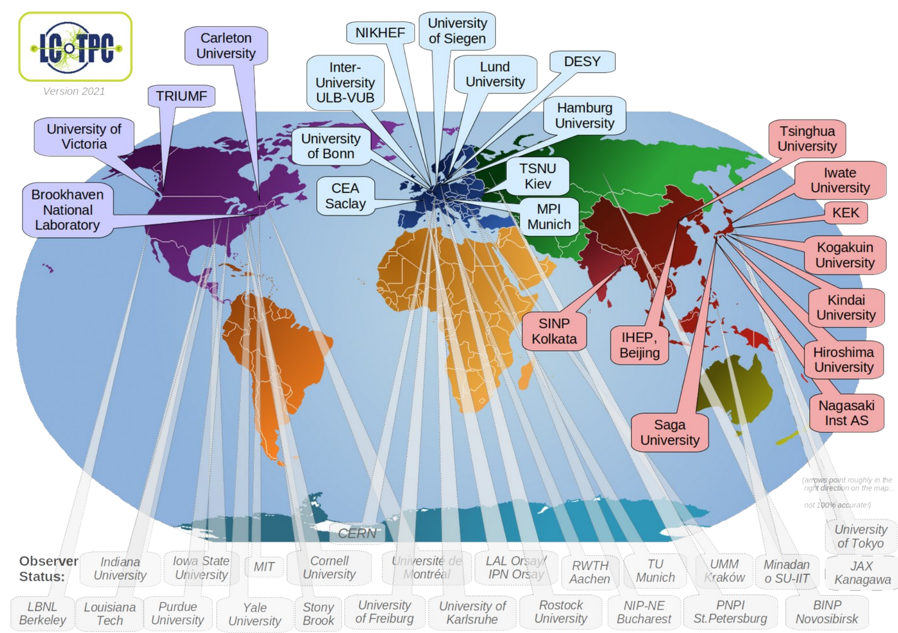



International Linear Collider (ILC) / Chinese Electron Position Collider (CEPC) are both $e^+e^-$ colliders with:
$\sqrt{s}$ = 90 GeV – 1 TeV / 90-240 GeV
Overall length of 21-50 km / 100 km

## International Large Detector ILD

- Standard layout HEP detector with improved performance
- TPC as main tracker
- In addition Si-strip detectors outside of the inner and outer field cage of the TPC.

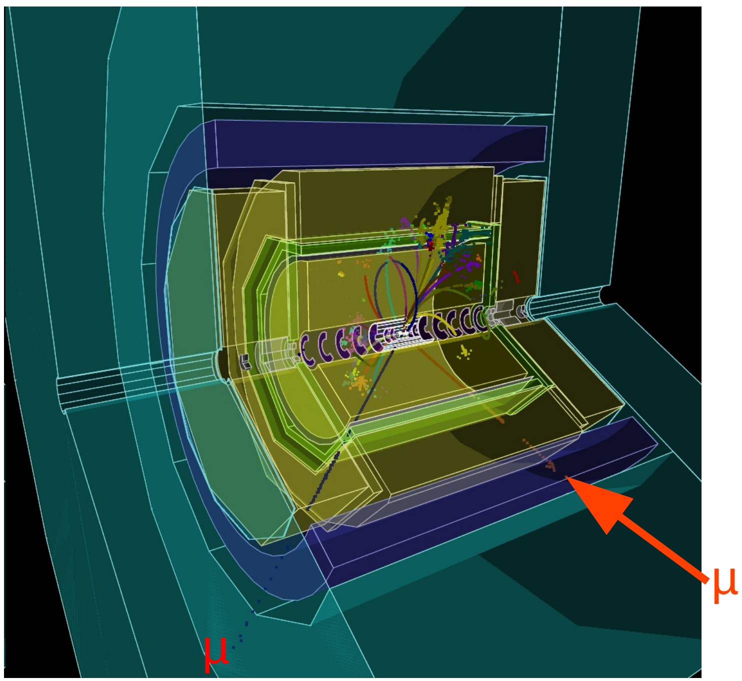





LCTPC collaboration studies MPGD-based readouts of TPCs for the ILD-type experiments and generic TPC-R&D for other future colliders.

# ILD-TPC Requirements

Requirements are driven by benchmark processes, in the case of ILD – TPC the most stringent measurement is the Higgs-recoil measurement:




Requirements of TPC from ILC TDR vol. 4

| Parameter | | | |
|---|---|---|---|
| Geometrical parameters | $r_{in}$ 329 mm | $r_{out}$ 1808 mm | z $\pm$ 2350 mm |
| Solid angle coverage | up to $\cos\theta \simeq 0.98$ (10 pad rows) | | |
| TPC material budget | $\simeq 0.05\ X_0$ including outer fieldcage in $r$ | | |
| | $< 0.25\ X_0$ for readout endcaps in $z$ | | |
| Number of pads/timebuckets | $\simeq$ 1-2 $\times$ $10^6$/1000 per endcap | | |
| Pad pitch/ no.padrows | $\simeq 1\times 6$ mm$^2$ for 220 padrows | | |
| $\sigma_{point}$ in $r\phi$ | $\simeq 60\ \mu$m for zero drift, $< 100\ \mu$m overall | | |
| $\sigma_{point}$ in $rz$ | $\simeq 0.4 - 1.4$ mm (for zero – full drift) | | |
| 2-hit resolution in $r\phi$ | $\simeq 2$ mm | | |
| 2-hit resolution in $rz$ | $\simeq 6$ mm | | |
| dE/dx resolution | $\simeq 5$ % | | |
| Momentum resolution at B=3.5 T | $\delta(1/p_t) \simeq 10^{-4}$/GeV/c (TPC only) | | |

Momentum resolution at B = 3.5 T $\delta(1/p_t) \approx 2{\cdot}10^{-5}$ /GeV/c (full tracking)

In addition: very high efficiency for particle of more than 500 MeV.

These requirements can not be fulfilled by conventional wire-based read out.

**New Micropattern-based readouts have to be applied featuring many benefits:**

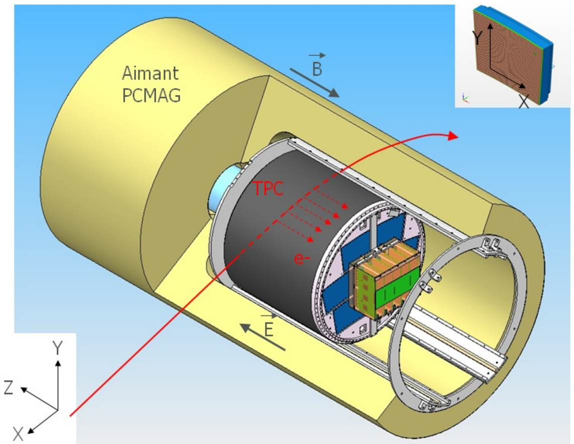
- Ion backflow can be reduced significantly
- Small pitch of gas amplification regions => strong reduction of E×B-effects
- No preference in direction => all 2 dim. readout geometries possible



arXiv: 1306.6329

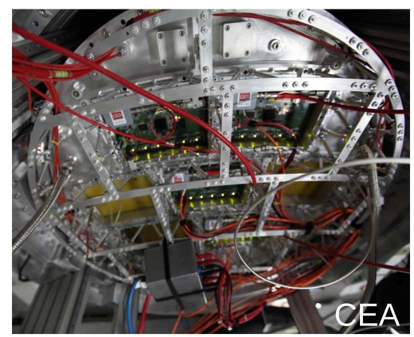
# Test setup at DESY

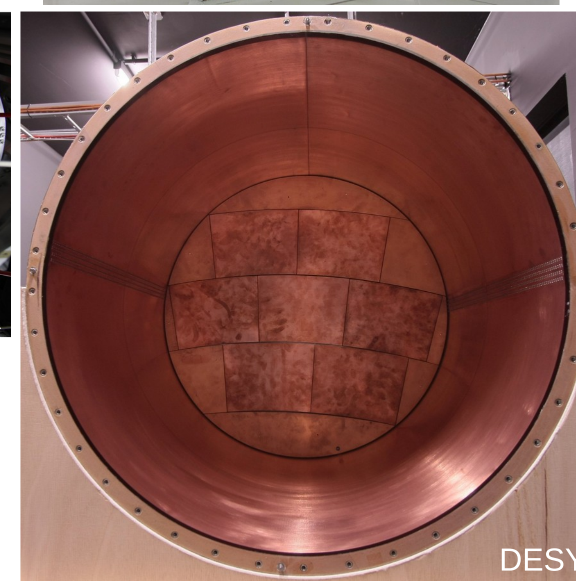
Large Prototype setup has been built to compare different detector readouts under identical conditions and to address integration issues.




PCMAG: B < 1.2 T, bore Ø: 85 cm
Electron test beam: E = 1- 6 GeV
LP support structure (3D movable)
Beam and cosmic trigger
Silicon tracker inside PCMAG
  LYCORIS (single point res.: 7 µm)

<u>LP Field Cage Parameter:</u>
length = 61 cm, inner Ø = 72 cm
drift field up to E ≈ 350 V/cm
made of composite materials: 1.24 % $X_0$



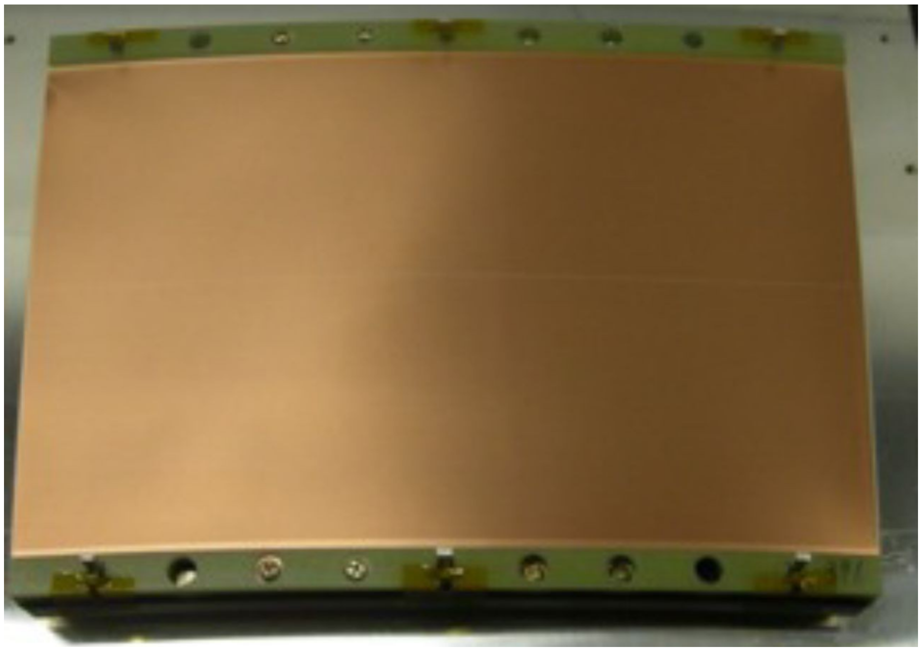



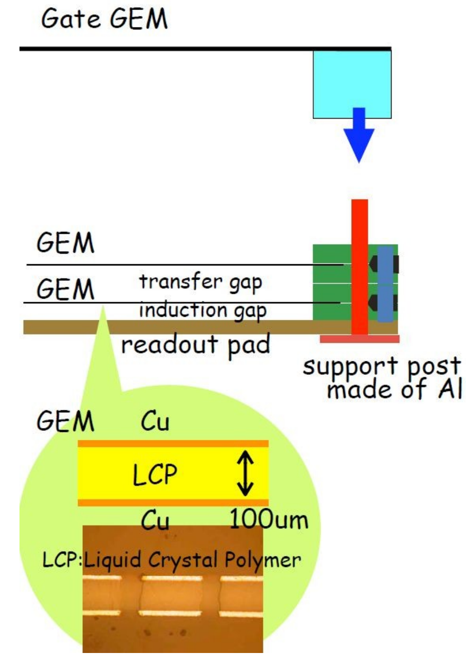

<u>Modular End Plate</u>
two end plates for the LP made from Al
with 7 module windows (one end plate has space frame)
→ size of module ≈ 22 × 17 $cm^2$ (ILD: 240 modules/endcap)

ALTRO based readout electronics (7212 channels)

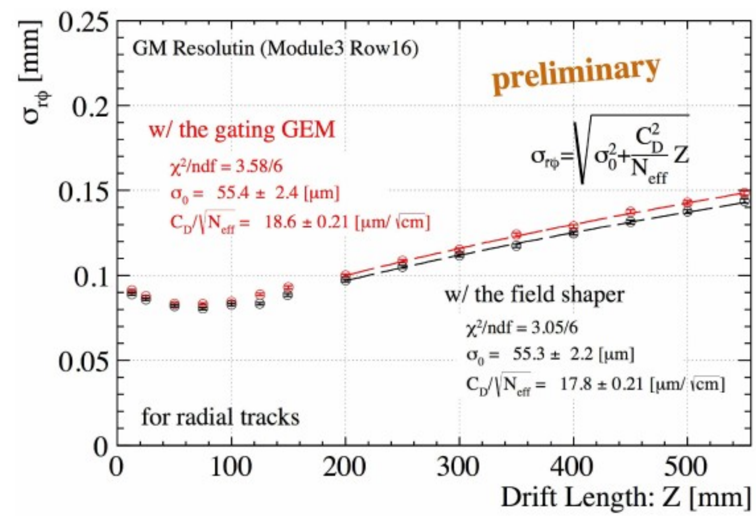
# GEM Modules (I) – double GEMs

**GEMs:** copper-insulator- copper sandwich with holes
2 configurations are being tested:
- double GEMs with 100 µm LCP insulator
- triple GEMs with 'standard CERN GEMs'




GEM Modules 1:
- 2 GEMs made of 100 µm thick LCP
- $1.2\times5.4\text{mm}^2$ pads




Design idea of GEM Modules 1:
- Minimize insensitive area pointing towards IP => no frame at modules sides
- Use thicker GEMs to give more stability
- Broader arcs at top and bottom

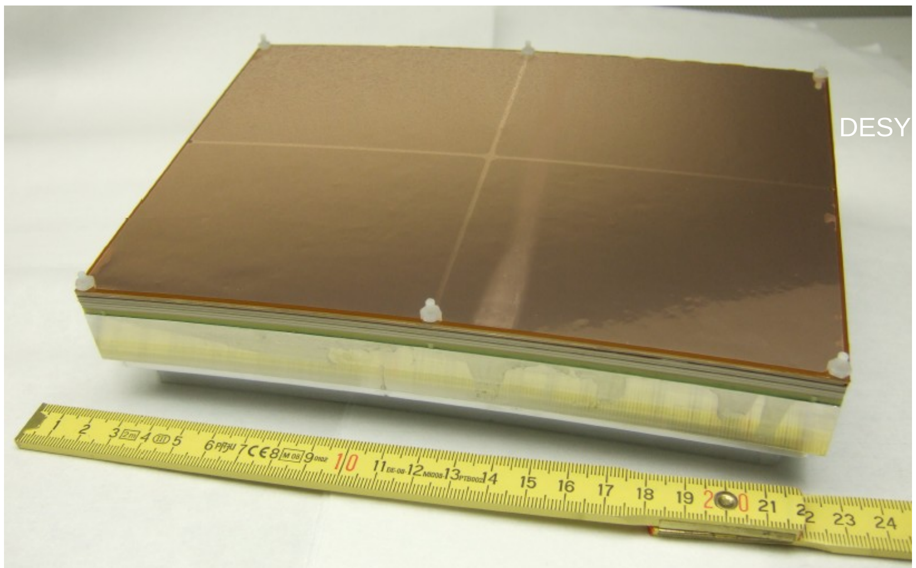

NIM A608 (2009) 390-396

# GEM-Modules (II) – triple GEMs

Design idea of GEM Modules 2:

Minimize dead area

Do not use frame to stretch GEMs,
but a 1 mm grid to hold GEM



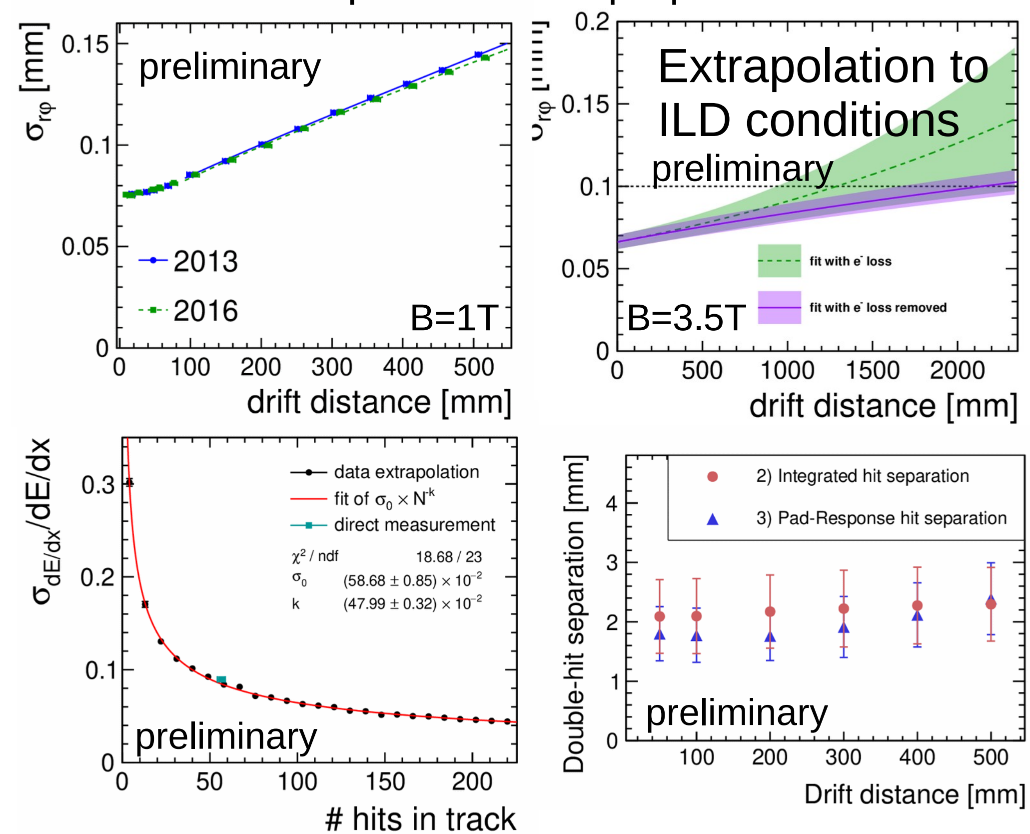

Spatial resolution published in first publication. Now, double track resolution and dE/dx performance is scrutinized, also, in dependence on the pad sizes.

2 iterations of modules built:

$1.26 \times 5.85 mm^2$ pads – staggered

Field shaping wire on side of module to compensate the field distortions

New publication in preparation:

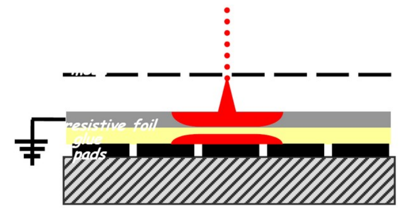




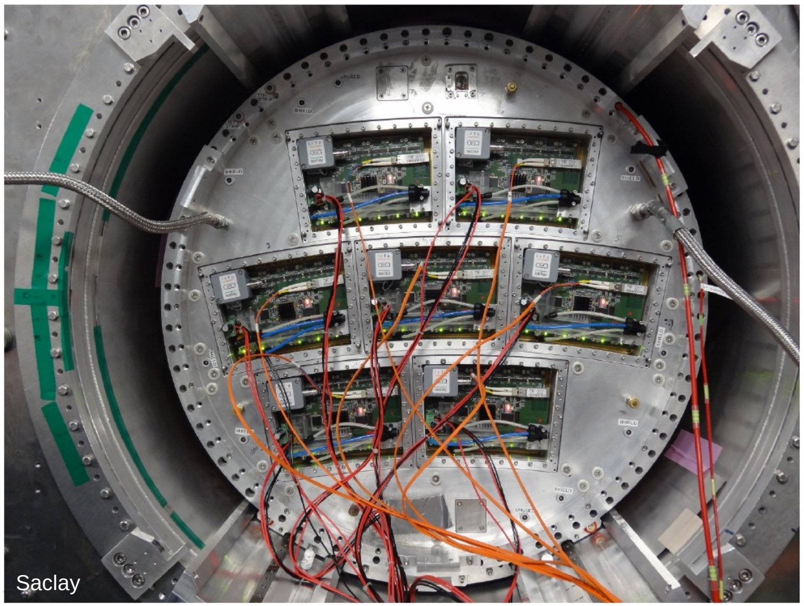

First publication:
NIM A856 (2017) 109-118

# Resistive Micromegas

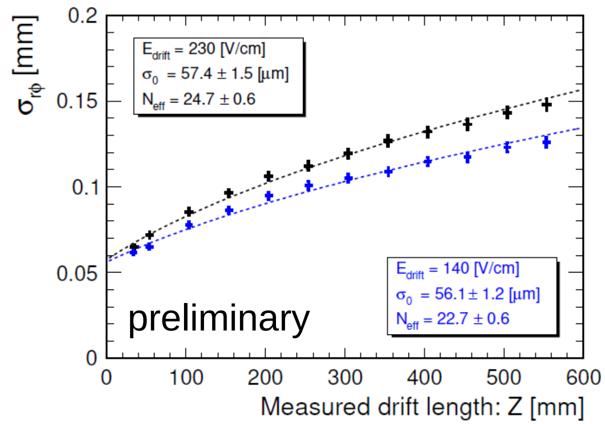
**<u>Resistive Micromegas:</u>** Bulk-Micromegas with 128 µm gap size between mesh and resistive layer (developed in LCTPC!).

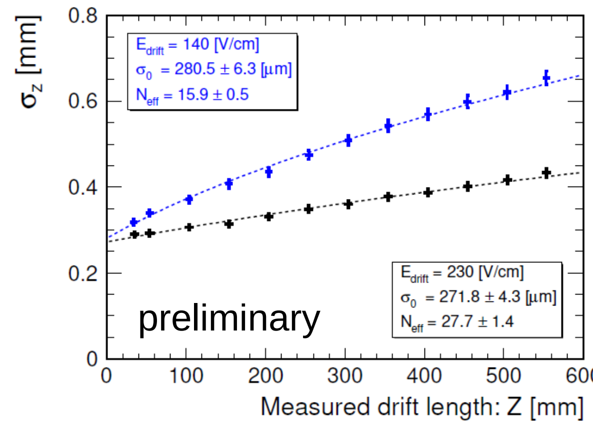



NIM A581(2007) 254



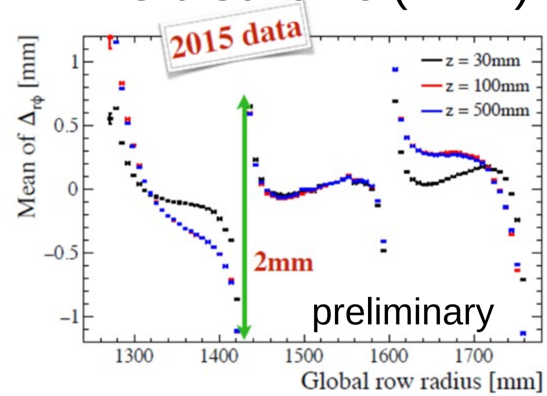

New publication in preparation:



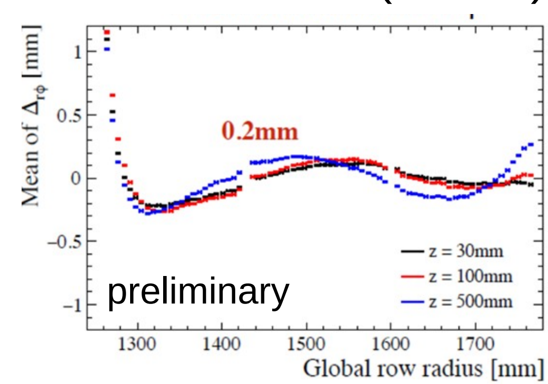




A new HV scheme of the module (ERAM) places grid on ground potential and reduces field distortions between modules by a factor of 10.

Old scheme (RAM)




New scheme (ERAM)



# Detector Modules

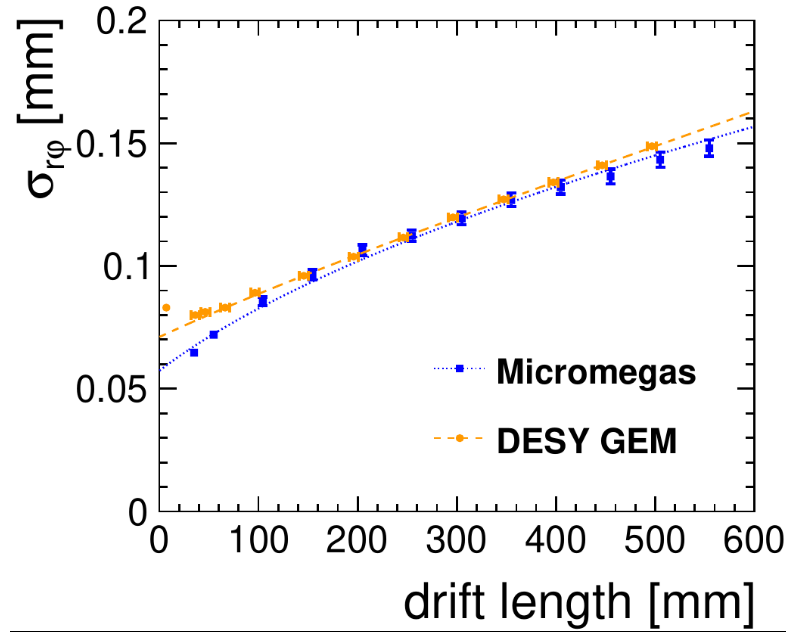
GEM and Micromegas groups have finished analysis of test beam data with previous set of detector modules. Both technologies show very similar performance. Now groups want to implement improvements in a new generation of modules. They are discussing new common modules, which should have a

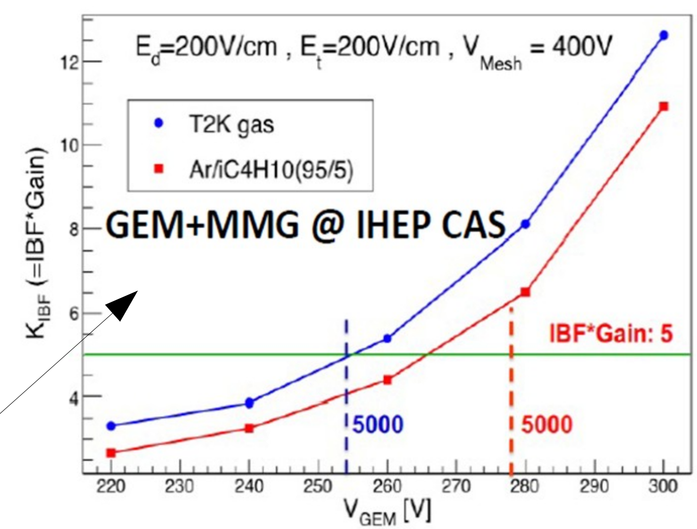
- a more final design and
- a more comparable design.
- common readout electronics (sALTRO),
- an identical gating device (gating GEM) and
- possibly a common pad plane

→ Only the gas amplification stage differs

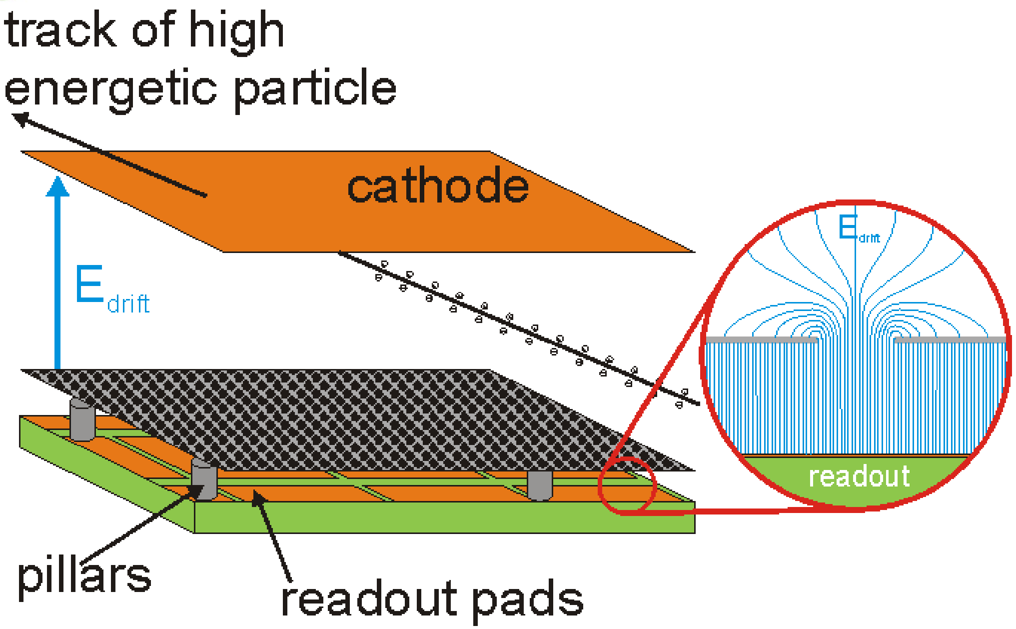
=> better comparison of performance for a technology decision.

Also combined Micromegas + GEM readout is tested, which promises a lower ion backflow, if gating is not possible (e.g. at the CEPC).



# Improving Micromegas: GridPix




Could the spatial resolution of single electrons be improved?

Diffusion in amplification region:

$Ar:CO_2$ 80:20 → σ = 11 μm

$Ar:iC_4H_{10}$ 95:5 → σ = 11 μm

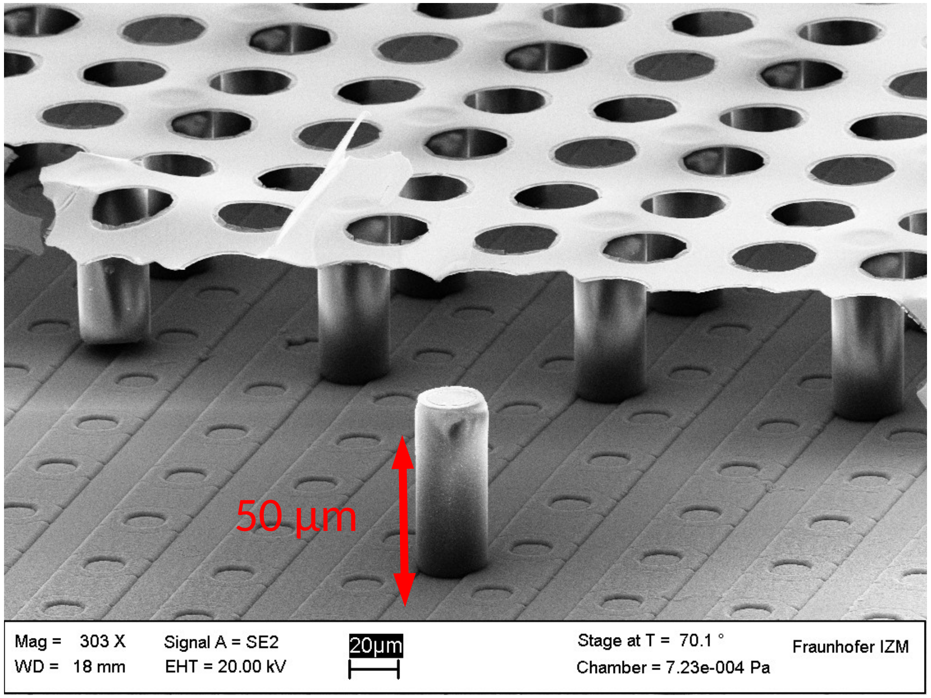
$Ar:CF_4:iC_4H_{10}$ 95:3:2 → σ = 11 μm

Smaller pads/pixels could result in better resolution!

At NIKHEF the GridPix was invented.

Standard charge collection:
Pads / long strips

Instead: Bump bond pads of pixel ASIC are used as charge collection pads.



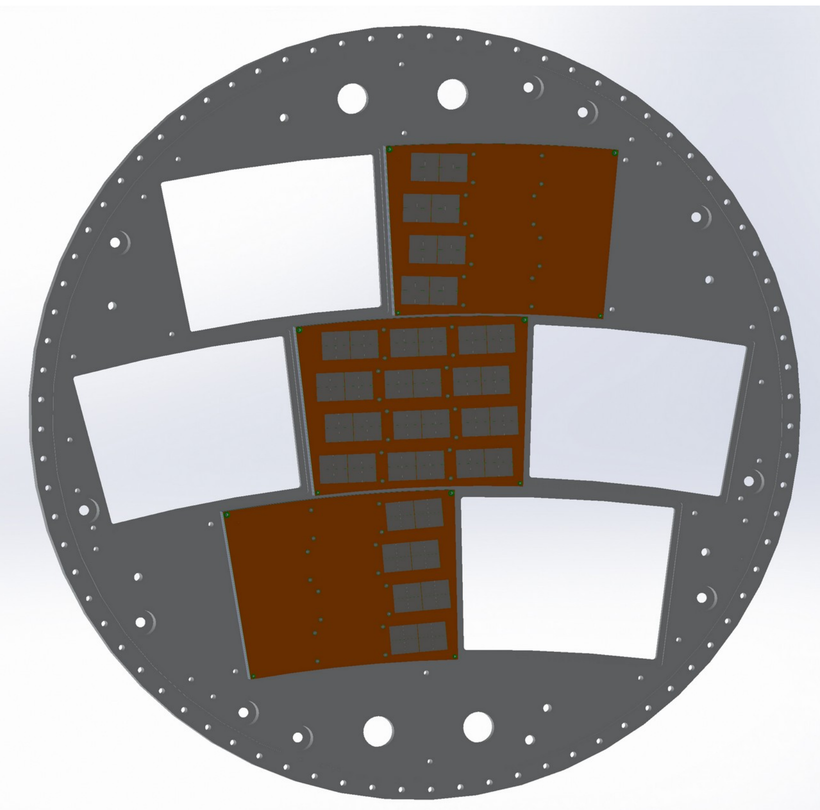

- Lower occupancy → easier track reco
- Removal of δ-rays and kink removal
- Improved dE/dx (4% seems possible)
- No angular pad effect

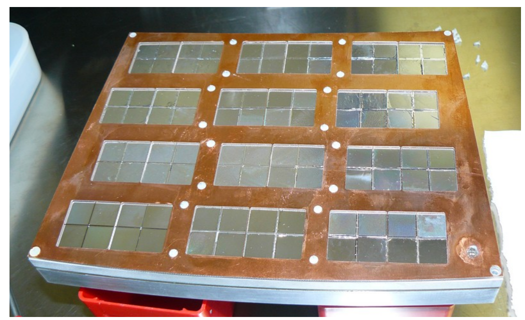


NIM A535 (2004) 506-510
NIM A845 (2017) 233-235

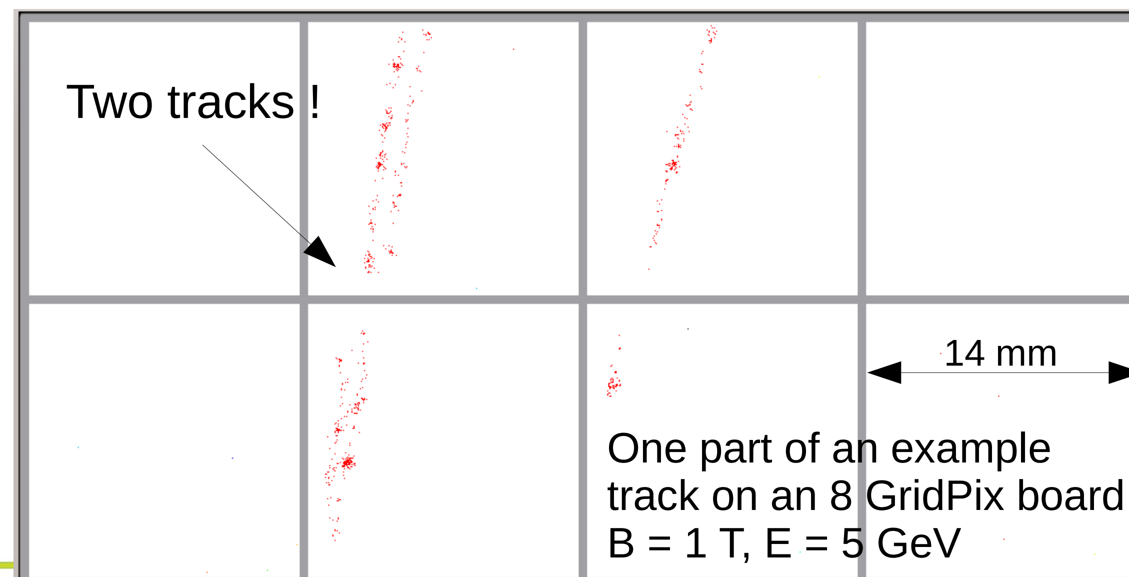
# Large Scale Readout

To readout the TPC with GridPixes:
~100-120 chips/module 240 module/endcap (10 m²) → 50000-60000 GridPixes
Demonstration of mass production: One LP-module covered completely with GridPixes (96 → coverage 50%) and two partially covered modules.
In total 160 GridPixes covered an active area of 320 cm² (10M pixel detector).





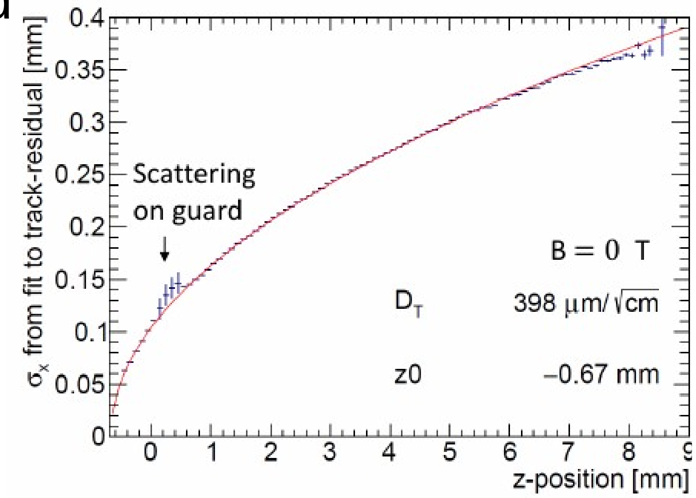
The test beam was a success:
A pixel TPC is realistic.
During the test beam ~$10^6$ events were collected.

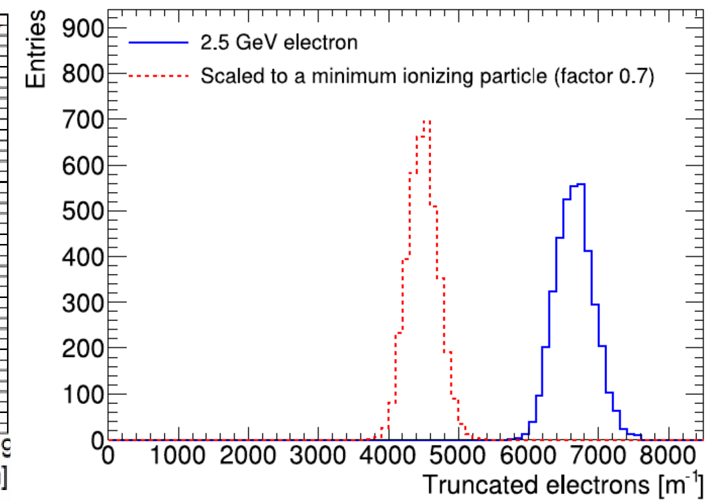


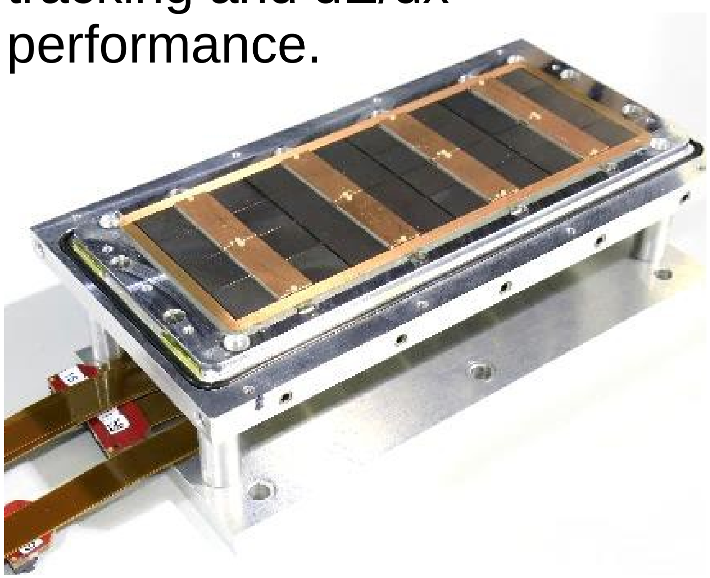

IEEE TNS 64 (2017) 1150

# Timepix3-based GridPix

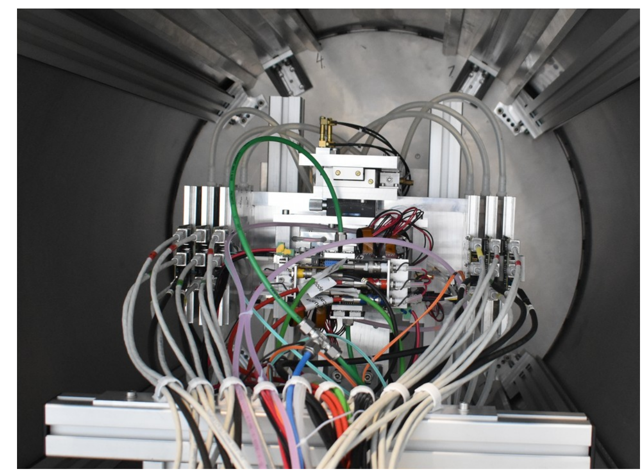
GridPix detector have moved from Timepix to Timepix3 ASICs. Tests with single and quad devices have been successfully done and published. As expected the spatial resolution of single electrons is diffusion limited and the very high detection efficiency results in excellent tracking and dE/dx performance.



A first module with 32 GridPixes has been constructed and was in a test beam at DESY in June 2021.
- including a test in a magnetic field of B = 1 T.



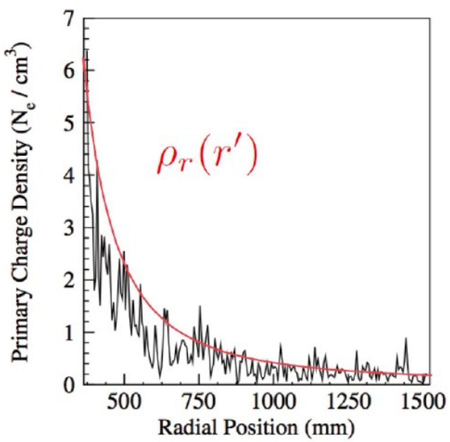
The ion back flow of the module has been measured and can be further reduced by applying a double grid. Also the resistivity of the protection layer will have to be reduced and Timepix4 development is observed.



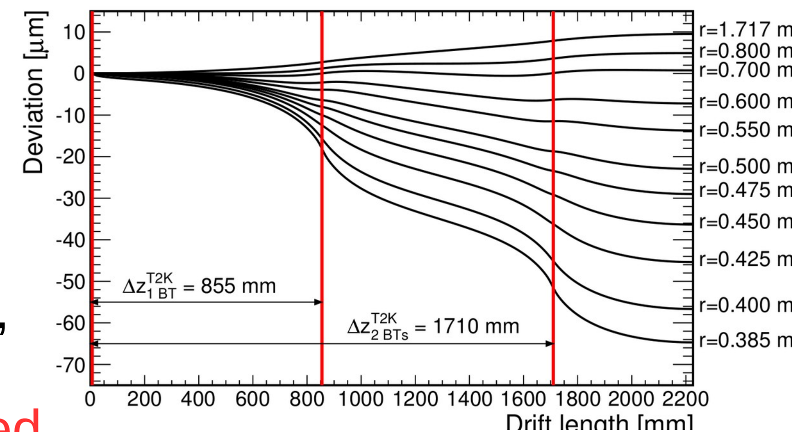

NIM A908 (2018) 18-23
NIM A956 (2020) 163331

# Ion Feedback and Gating

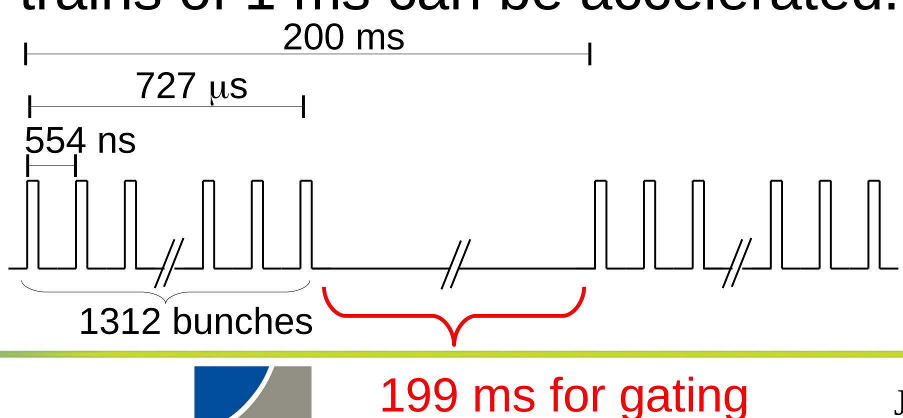
Primary ions create distortions in the electric field which result in O(<1µm) track distortions including a safety margin of estimated BG.




- Machine induced background has 1/r shape
- Ions from gas amplification stage build up discs
- Track distortions are 20 µm per disc without gating device, if IBF is 1/gain
- Total: 60 µm => Gating is needed

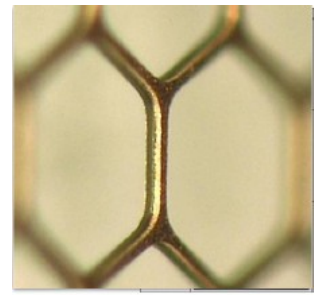


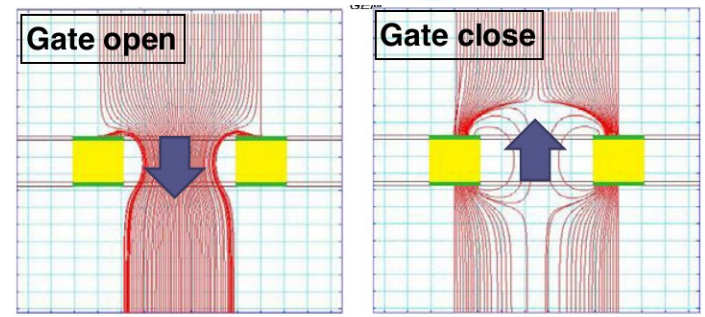

<u>Bunch structure at ILC:</u>
Charging the superconducting cavities takes 0.1-0.2 s, then bunch trains of 1 ms can be accelerated.



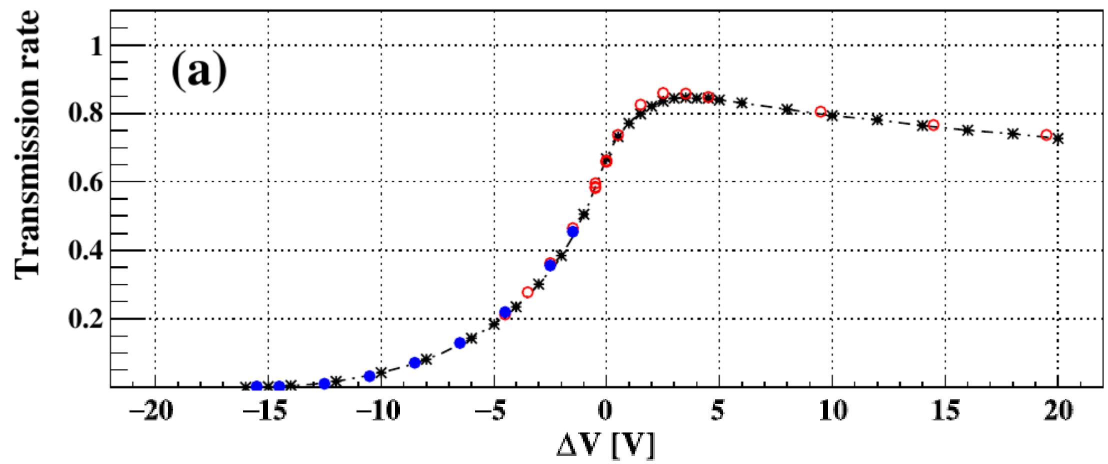

- Wire gate is an option
- <u>Alternatively:</u> GEM-gate
- Simulation shows:
  Maximum electron transparency is close to optical transparency
- Fujikura Gate-GEM Type 3
  Hexagonal holes: 335 µm pitch,
  27/31 µm rim
  Insulator thickness 12.5 µm

# Gating GEM






The gating GEM is the favorite gating device. It has large holes (Ø 300 µm) and thin strips inbetween (30 µm).

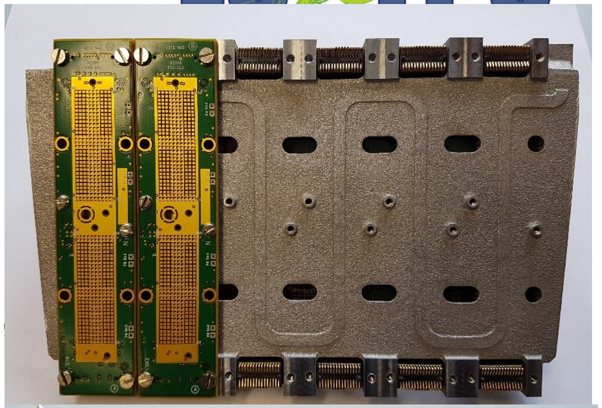


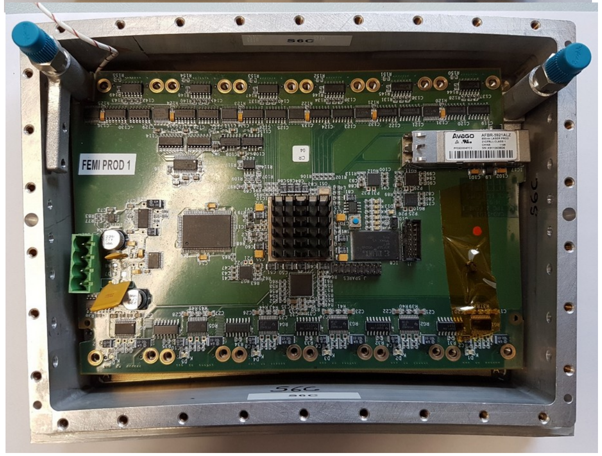

The electron transparency has been determined with different measurements and corresponds to 82 % as expected from simulations.

The ion blocking power has also been demonstrated, now gating should be tested in B = 3.5-4 T.
Also a fast HV switching circuit has to be developed.

# Cooling

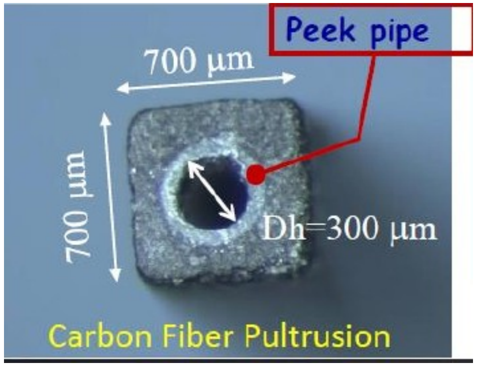
Despite power pulsing, the readout electronics will require a cooling system. 2-phase $CO_2$-cooling is a very interesting candidate. A fully integrated AFTER-based solution has been tested on 7 Micromegas modules during a test beam.

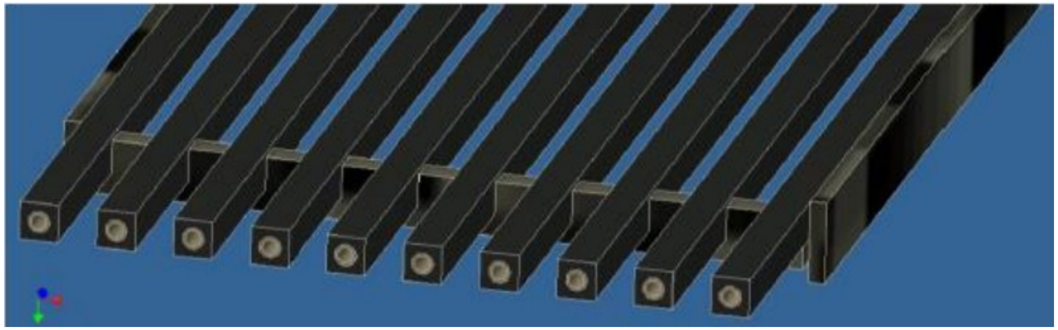





To optimize the cooling performance and the material budget 3D-printing of aluminum is an attractive possibility for producing the complex structures required. A prototype for a full module is available now at CEA, Saclay. It was tested with A full set of electronics in 10/2021 showing excellent cooling performance.

Alternatively, Lund is exploring micro channel cooling together with Pisa. These consist of pipes with Ø 300 µm in carbon fiber tubes.



# Summary

- Continue GEM, Micromegas and GridPix tests at the LP in preparation for the preliminary design of the TPC during the pre-Lab phase.

- A gate should be included in the next-generation GEM, Micromegas and GridPix modules.

- Synergies with T2K / ALICE / CEPC / EIC allow us to continue R&D and of course we learn from their experiences and R&D. We are also open for people interested in applications beyond the scope of ILC.

- Continue electronics, cooling and power pulsing development.

- Many simulations are still necessary to understand the detailed requirements of the final detector (e.g. number of ADC bits, pad sizes, etc.), but also new ideas for old challenges are welcome.