SiW ECAL – Status and outlook

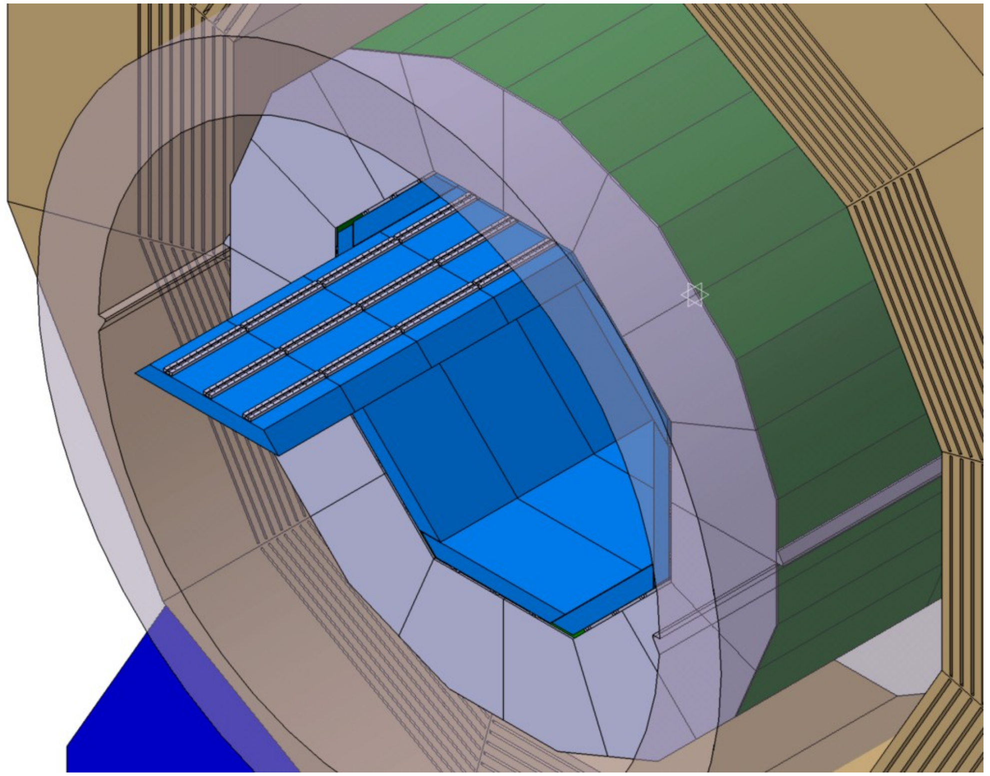
Roman Pöschl

On behalf of the SiW ECAL Groups in CALICE:

ILD Main Meeting – May 2022

Silicon Tungsten electromagnetic calorimeter

- Optimized for Particle Flow: Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

- O(10^8) cells
- "No space"
=> Large integration effort

Basic Requirements:
- Extreme high granularity
- Compact and hermetic
- (inside magnetic coil)

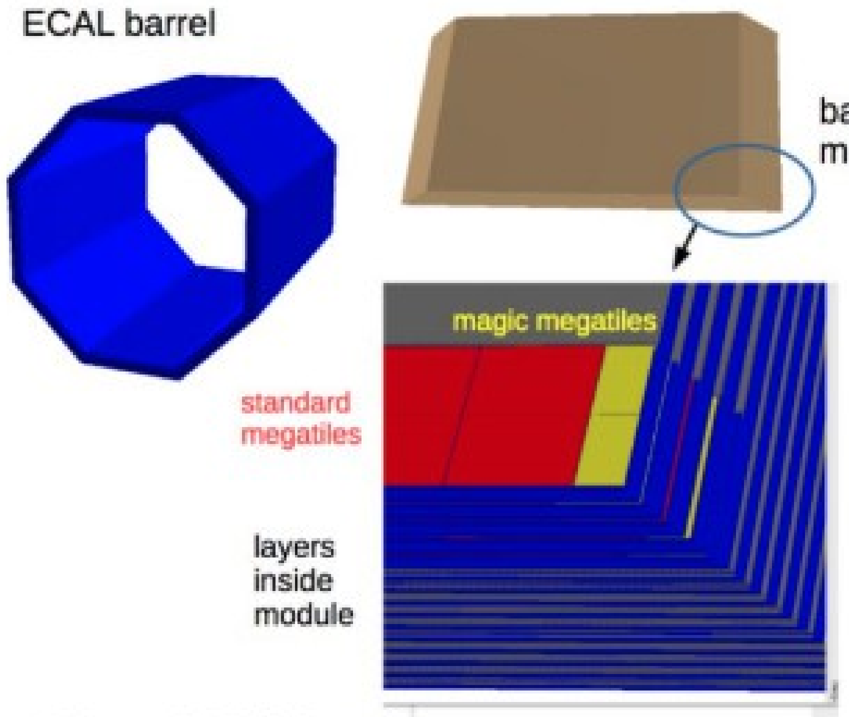
Basic Choices:
- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, λ_I=96mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design
  - Allows for pixelisationRobust technology
  - Excellent signal/noise ratio: 10 as design value

- All future e+e- collider projects feature at least one detector concept with this technology
  - Decision for CMS HGCAL based on CALICE/ILD prototypes

Granular calorimeters – Use case I

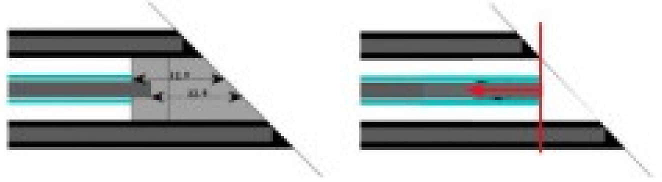
ECAL driver used in ILD models has been largely re-written (➡ DD4HEP)

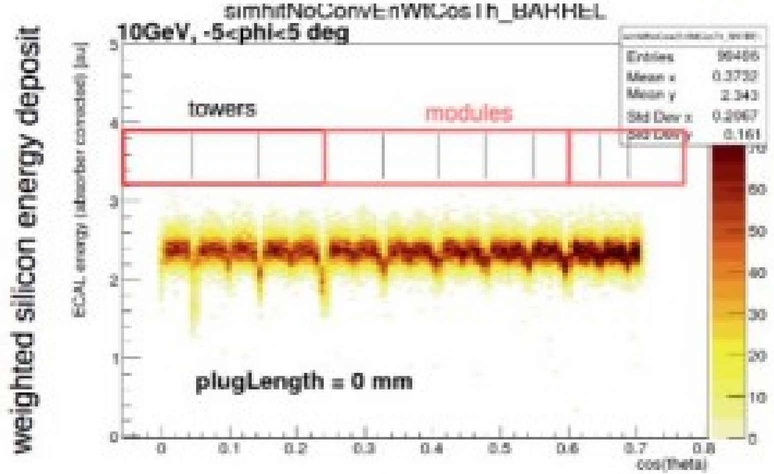
- more modular code:
- less duplication Barrel & Endcap
- more configurable…



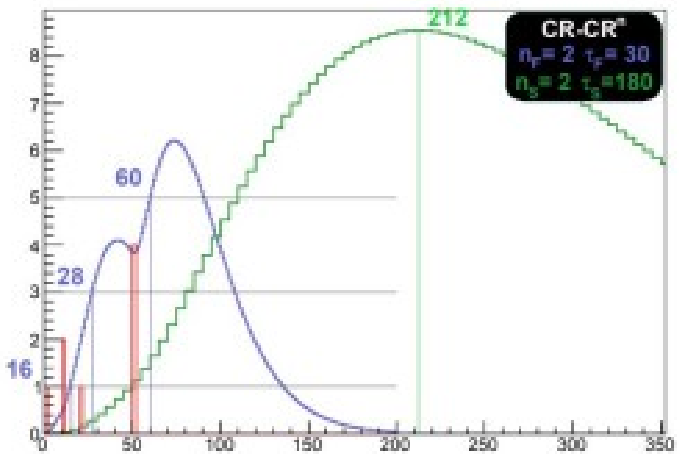
Effect of cracks [RAW= no correction at all!!]

- Drop ~ 15%





Improved digitization, modelling the SK2 (& beyond) ➡ ⊃ timing



SiW-ECAL, CALICE ... 2018

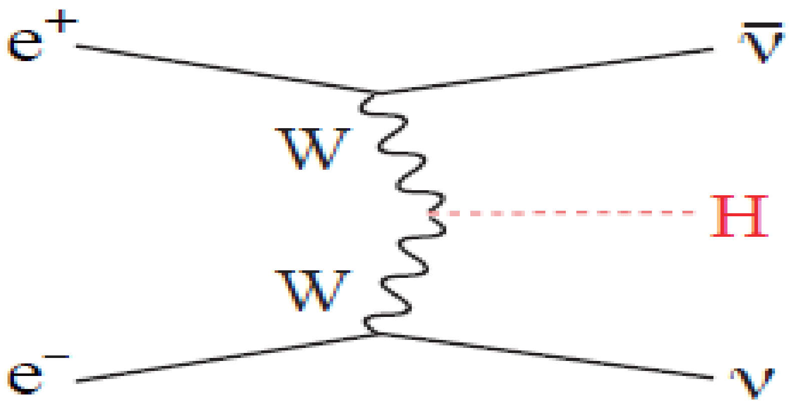
26/36

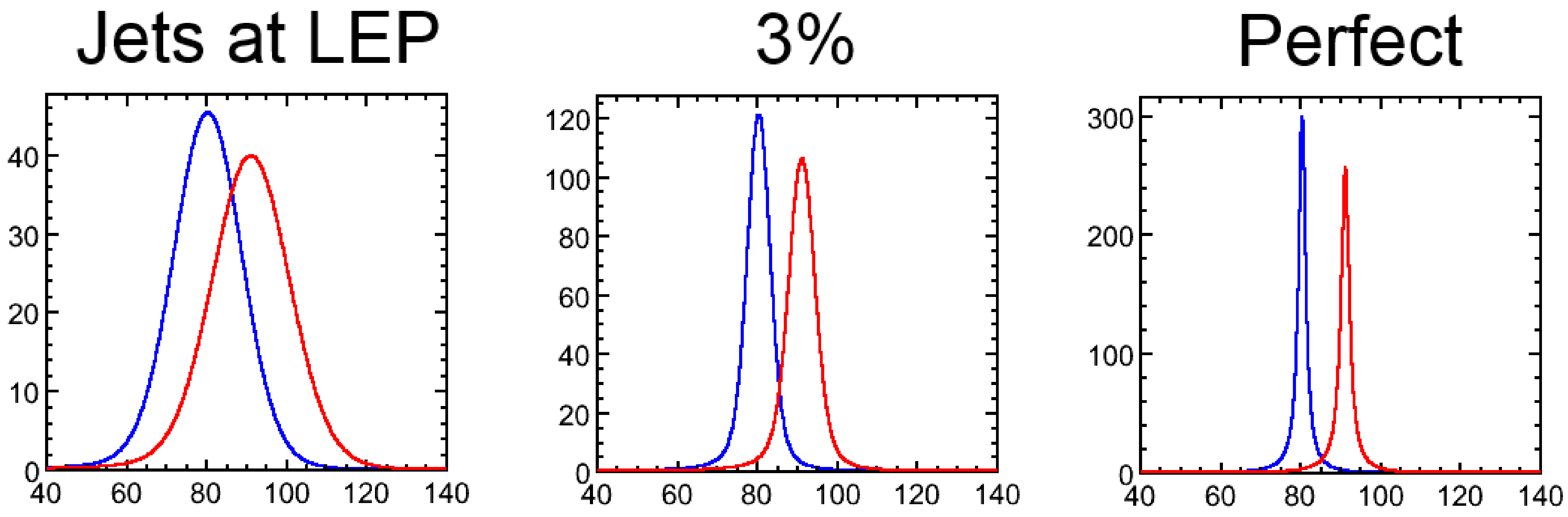
V. Boudry, ILC TC Meeting, March 2022

Granular calorimeters – Use case I

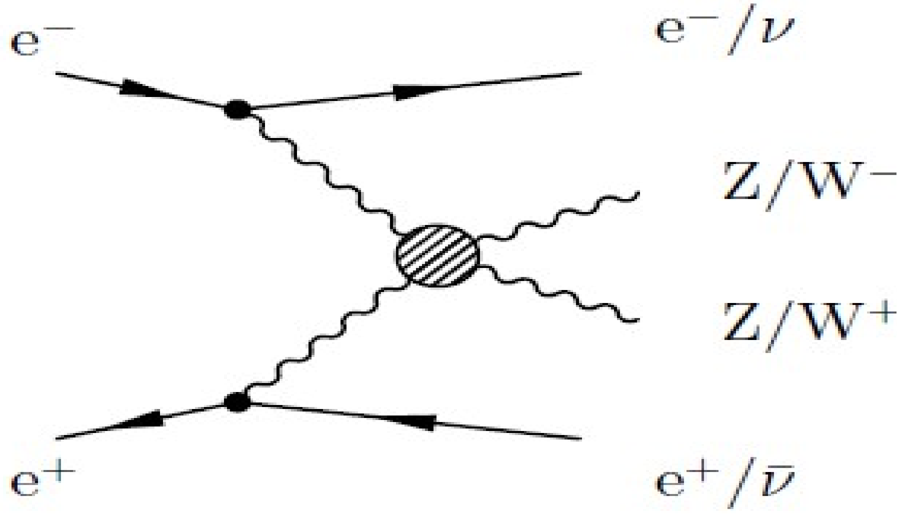
Examples:

- W Fusion with final state neutrinos requires reconstruction of H decays into jets
- Jet energy resolution of ~3% for aclean W/Z separation





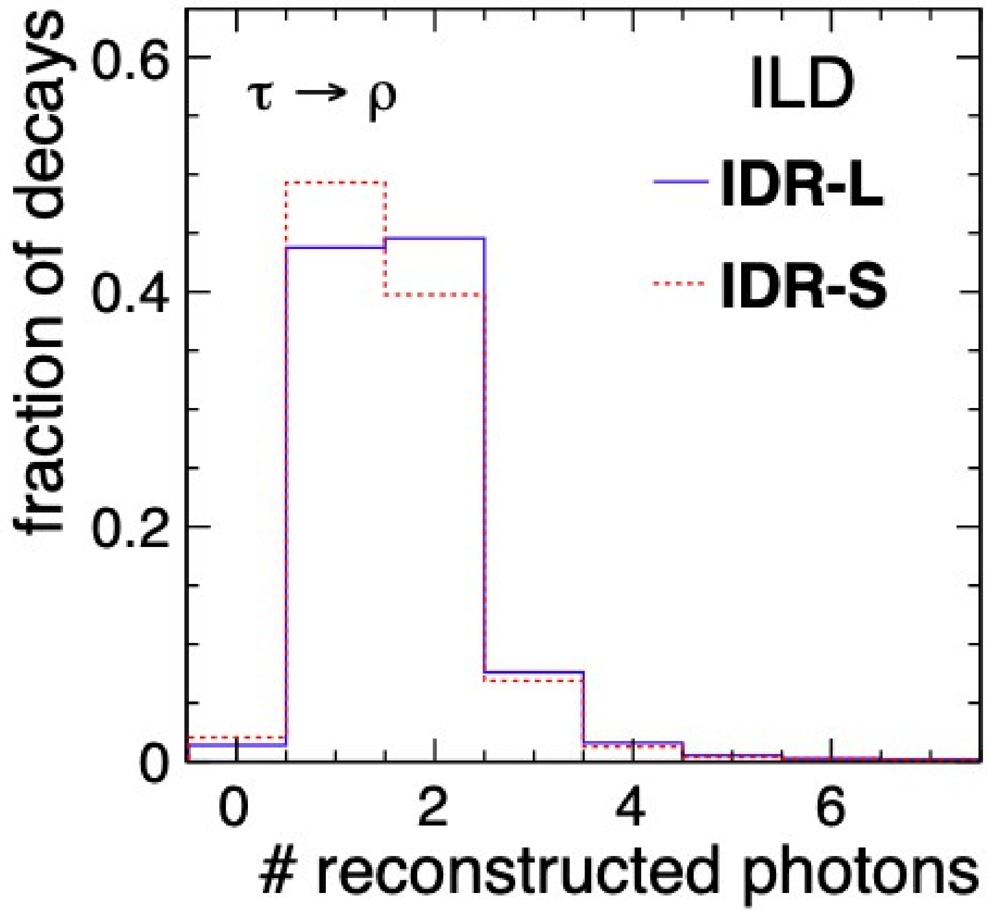
M. Thomson



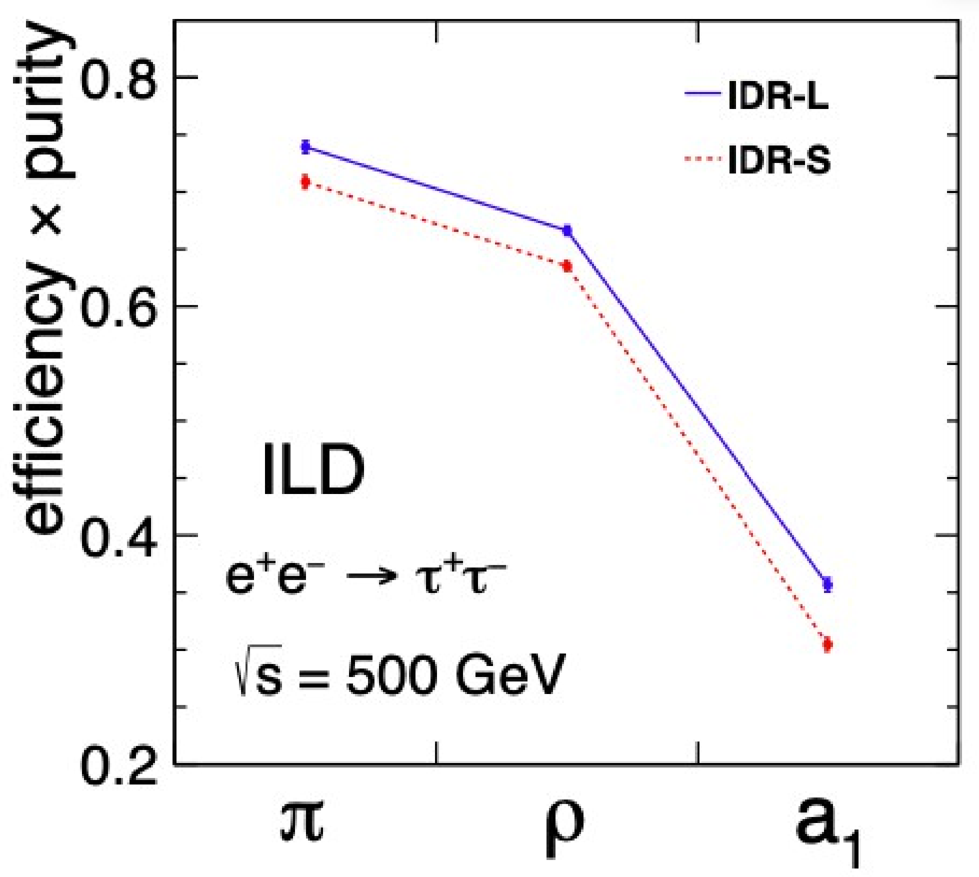
Slide: F. Richard at International Linear Collider – A worldwide event

Granular calorimeters – Use case II

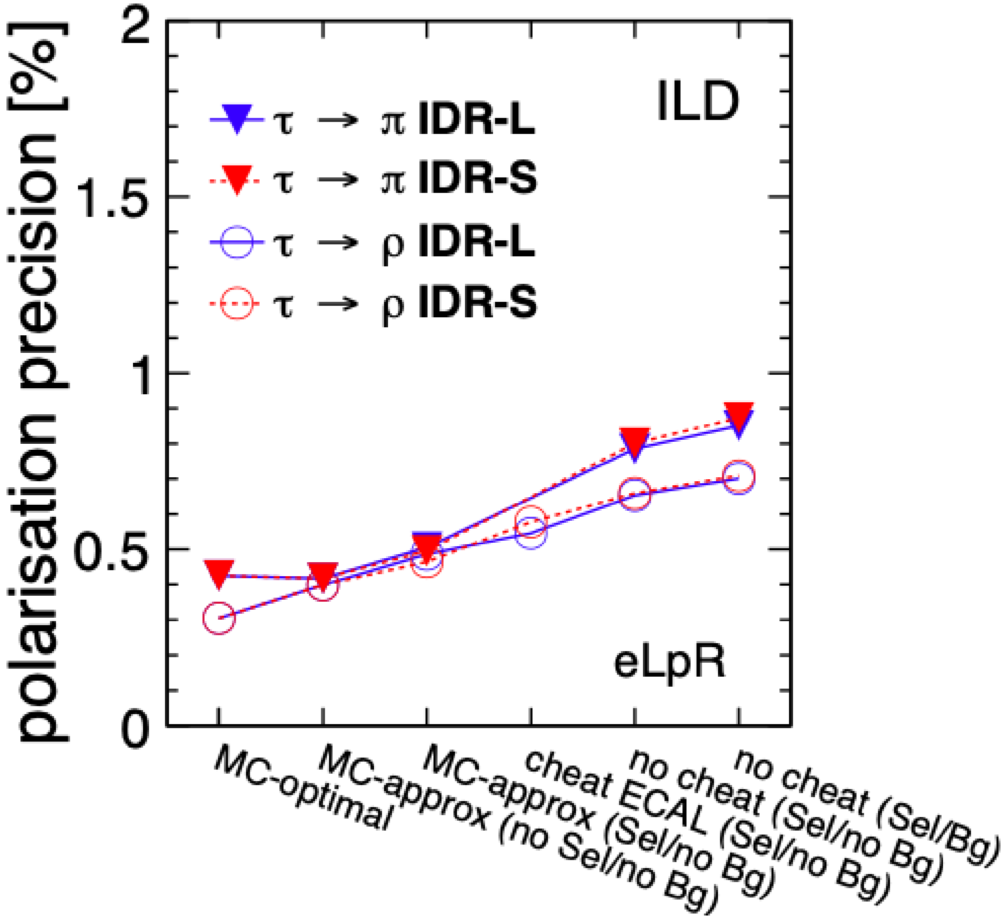
$e^+e^- \to \tau^+\tau^-$ Recent study at 500 GeV for ILD IDR



- Photon separation gets involved at high energies
- Still often only one photon reconstructed



- EfficiencyxPurity drops with increasing photon multiplicity



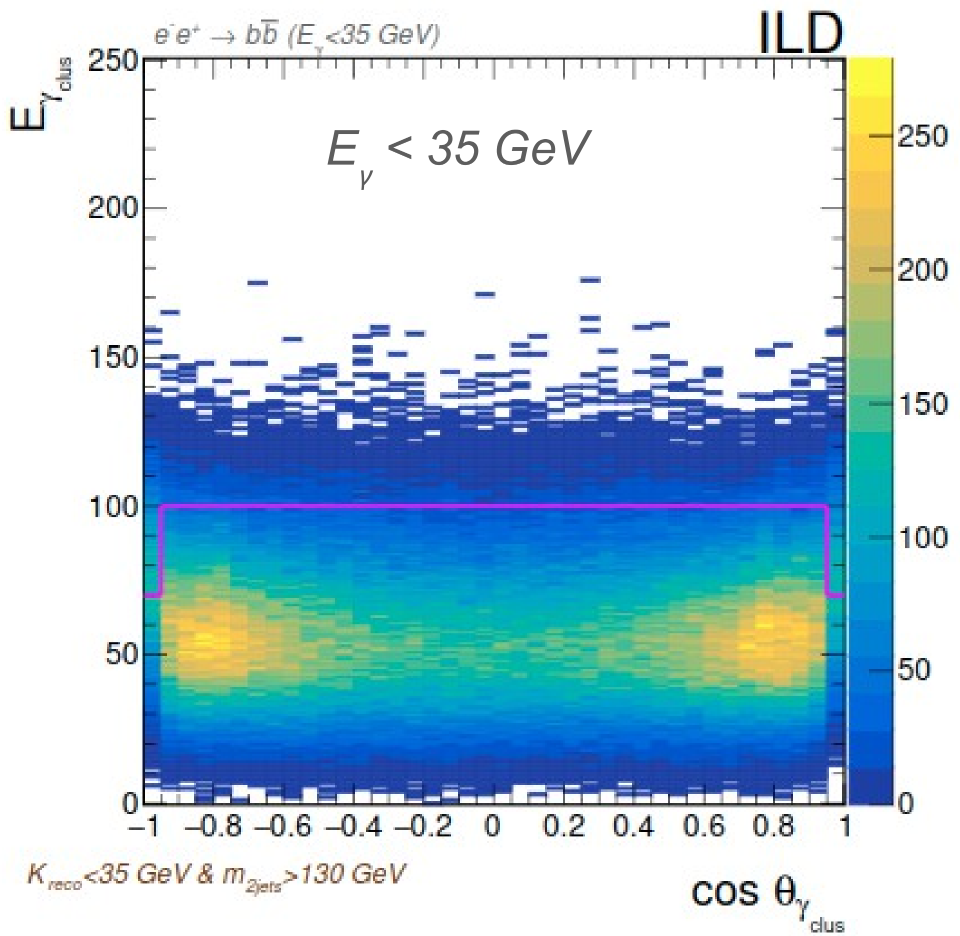
Precision of tau polarisation of order 0.3%-1%

- Close-by photons are challenge for highly granular calorimeters (in particular Ecal) at high-energies
- Ideal benchmark for detector optimisation
- Maybe still room for improvement, better algorithms?

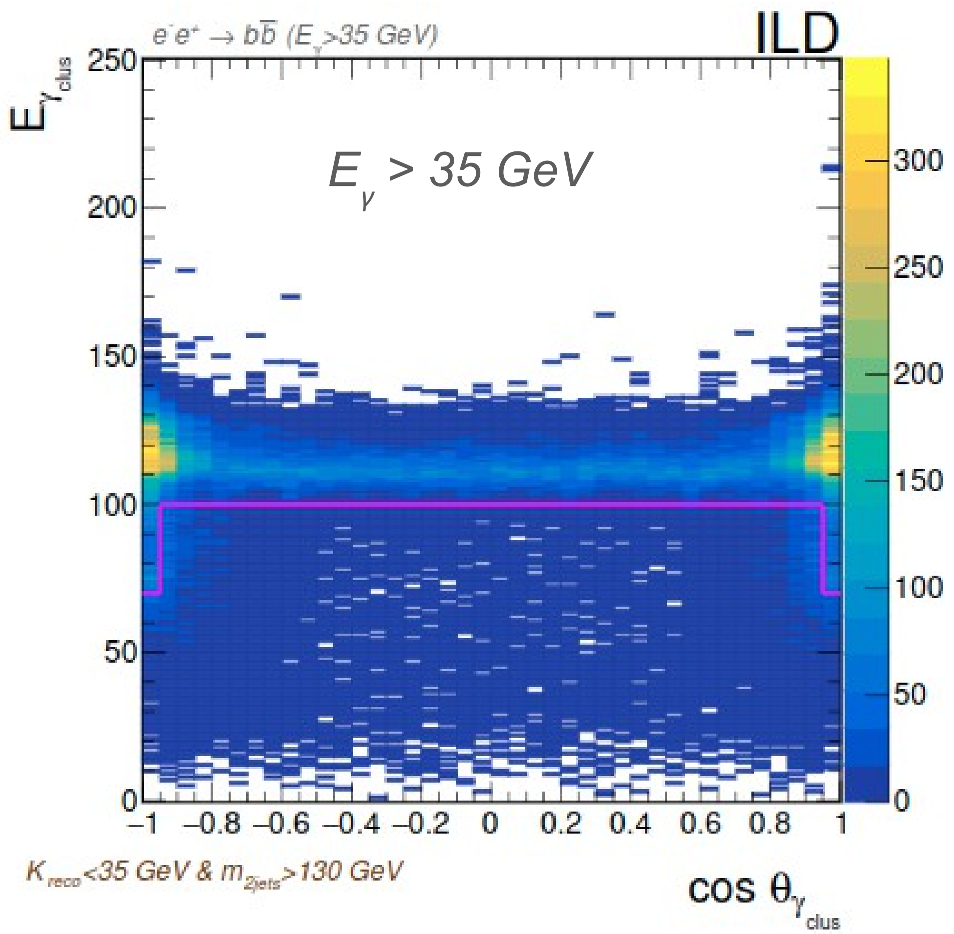
Granular calorimeters – Use case III

- Most ISR Photon are radiated collinearly but lead to a boost -> Check for acolinearity of dijet event
- Method doesn't work when photon is radiated into detector acceptance
  - ... and merged with a jet --> Busy environment

No or mild ISR



"Strong? ISR



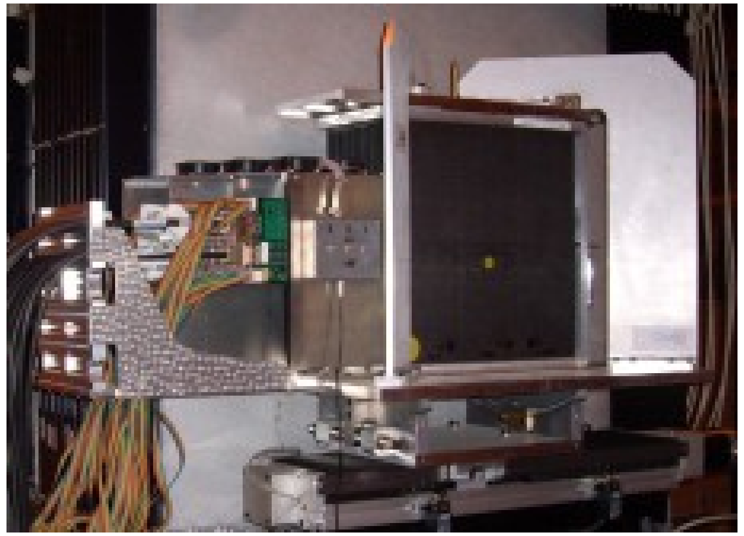
- Excellent photon ID in granular calorimeter is key
- Identification of ISR photon within detector (jet) reduces ISR background by nearly a factor of six
  - (See table in backup)
- Would be interesting to carry out this analysis with less granular calorimeters

ILD: Irles, Richard, R.P.

Steps of R&D

Physics Prototype

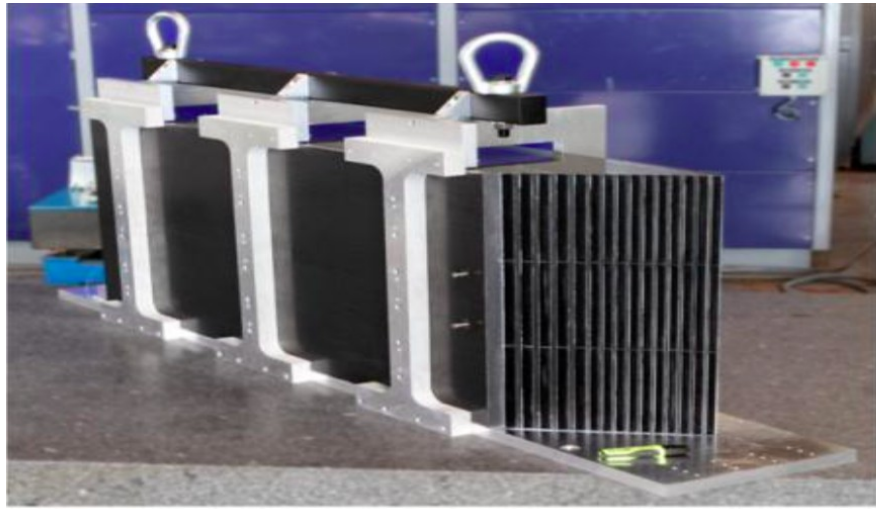
2003 - 2012



- Proof of principle of granular calorimeters
- Large scale combined beam tests

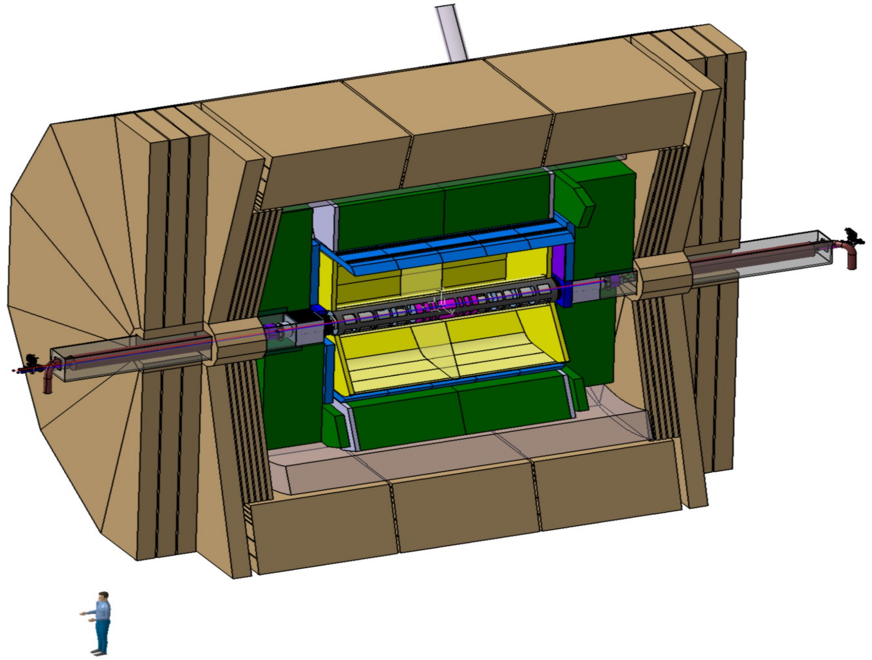
Technological Prototype

2010 - ...



- Engineering challenges
- Higher granularity
- Lower noise
- **Today**

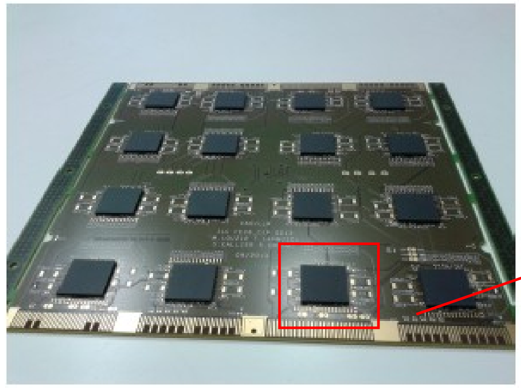
LC detector



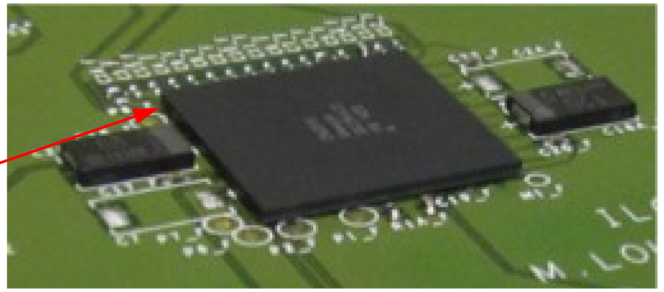
- The goal
  - Typically 10^8 calorimeter cells
- Compare:
  - ATLAS LAr ~10^5 cells
  - CMS HGCAL ~10^7 cells

SiW Ecal – Elements of (long) layer

ASIC+PCB+SiWafer =ASU
Size 18x18 cm^2
(IJCLab, Kyushu, OMEGA, LLR, SKKU)

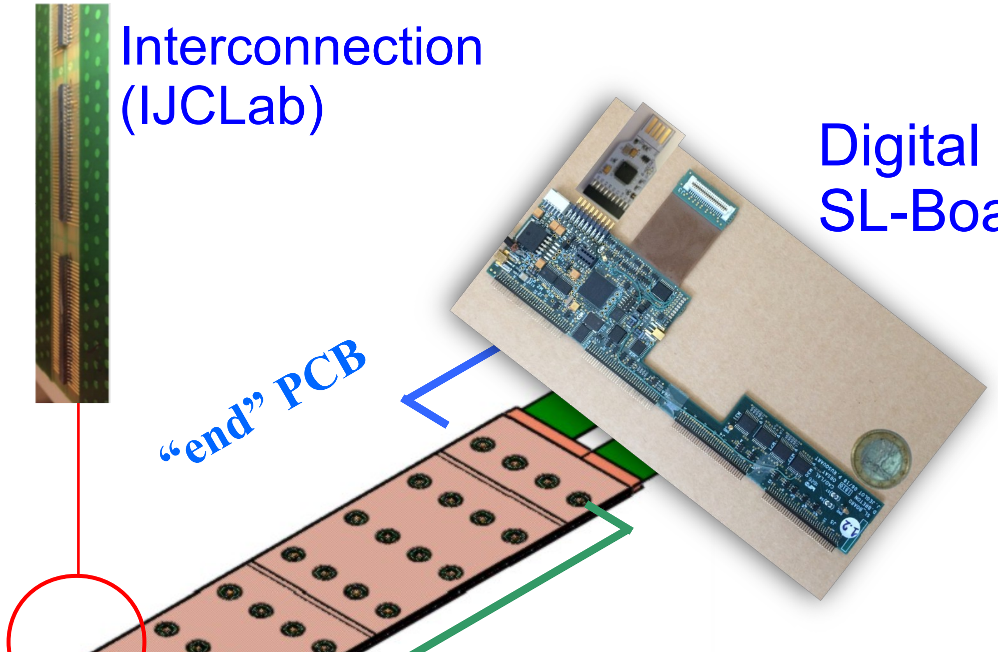


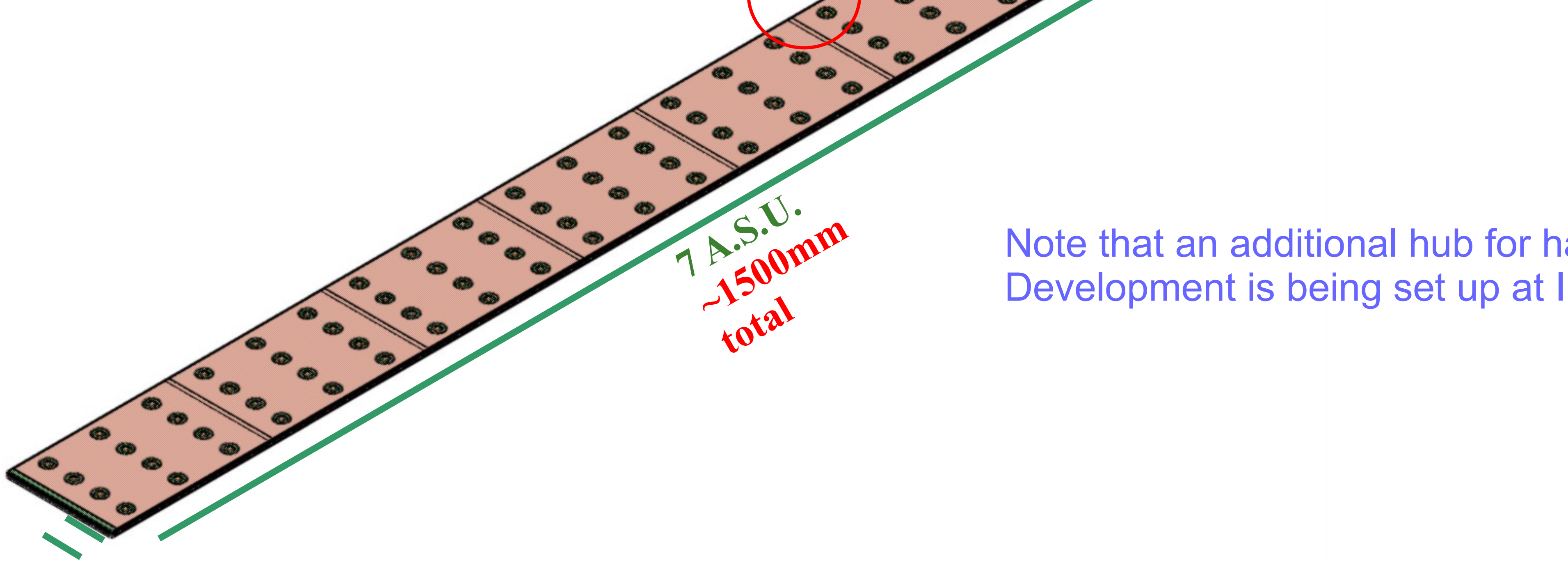
ASIC SKIROC2(a)
(OMEGA)
Wire Bonded or In BGA package
(IJCLab, Kyushu, LLR)



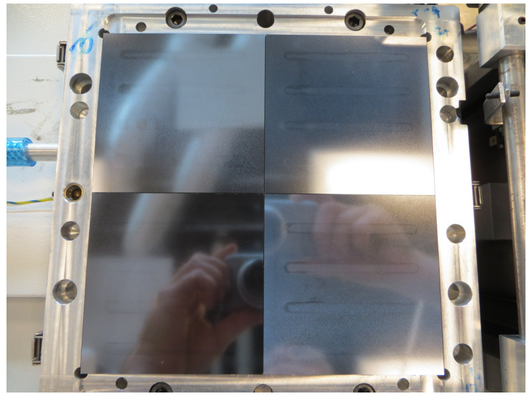
Interconnection (IJCLab)

Digital readout SL-Board (IJCLab)





SiWafers glued onto PCB
Pixel size 5.5x5.5 mm^2
(LPNHE)

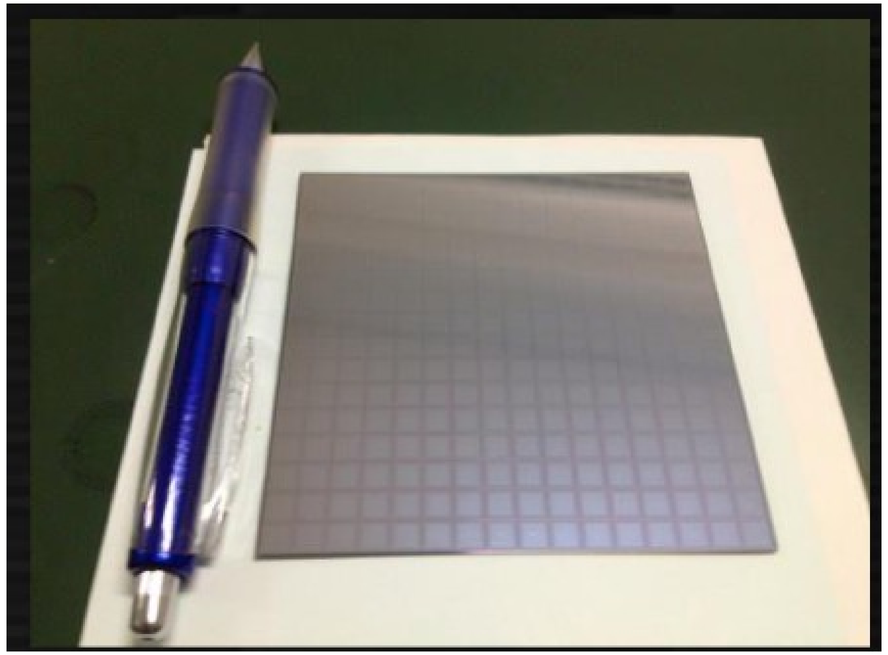


Note that an additional hub for hardware Development is being set up at IFIC/Valencia

- The beam test set up will consist of a **stack of short layers** consisting of one ASU and a readout card each

SiW Ecal – Wafer R&D I

Si Sensor (9x9cm^2 from 6" wafer)



N-type silicon
Crystal Orientation: <100> or <111>

Wafer specs

Tab 1 : Summary of the substrate characteristics

	Min.	Typ.	Max.
N type silicon	-	-	-
Resistivity (kOhms.cm)	4	5	-
Thickness (μm), option T1	310	320	**330**
Thickness (μm), option T2	490	500	**510**
Width (mm), option S1	89.7	89.8	89.9
Width (mm), option S2	44.7	44.8	44.9

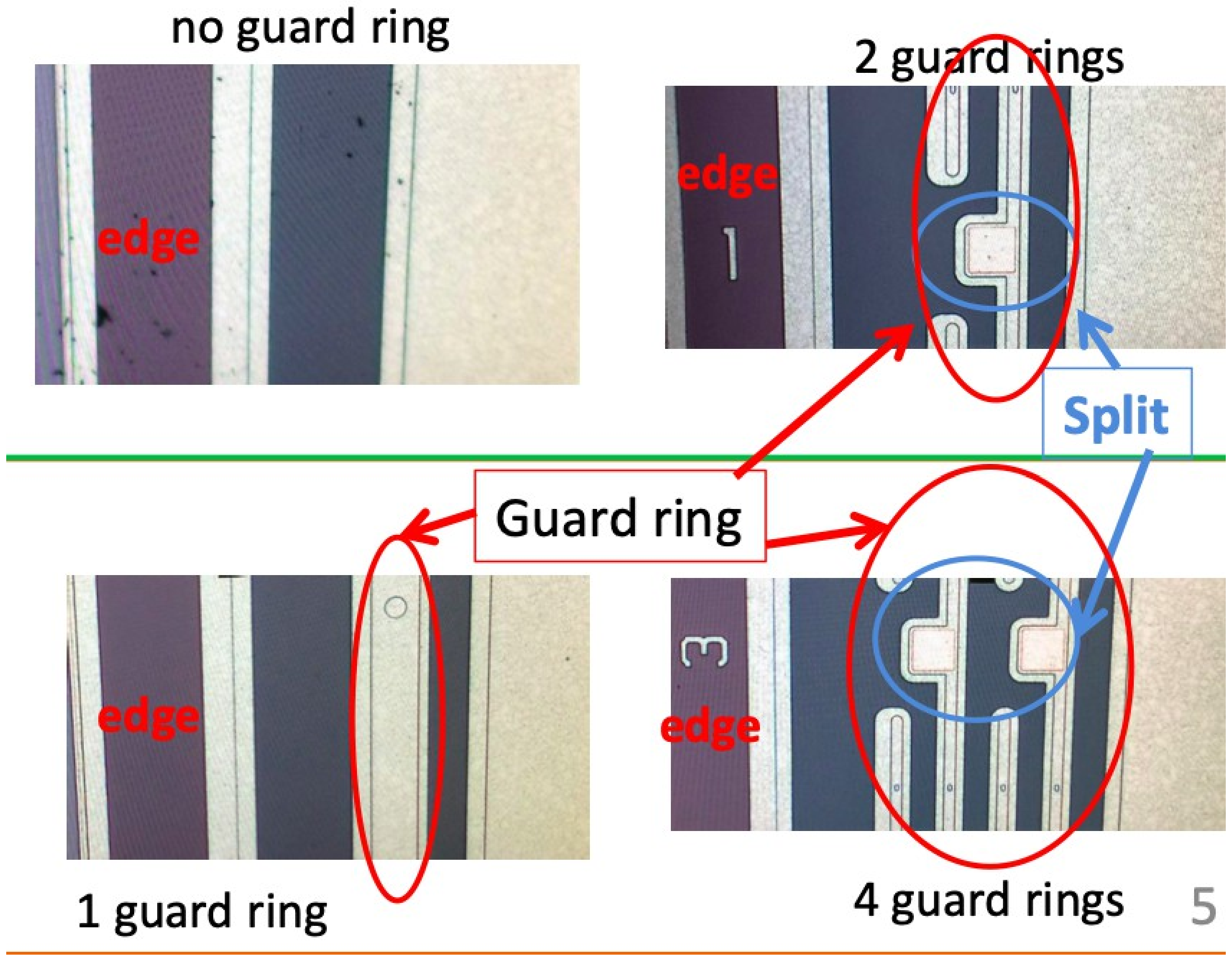
Definition of specifications for different wafer types:
Resisitvity: > 5 kΩxcm
Price: Typically 1000-1500 EUR/wafer (when ordering small quantities)

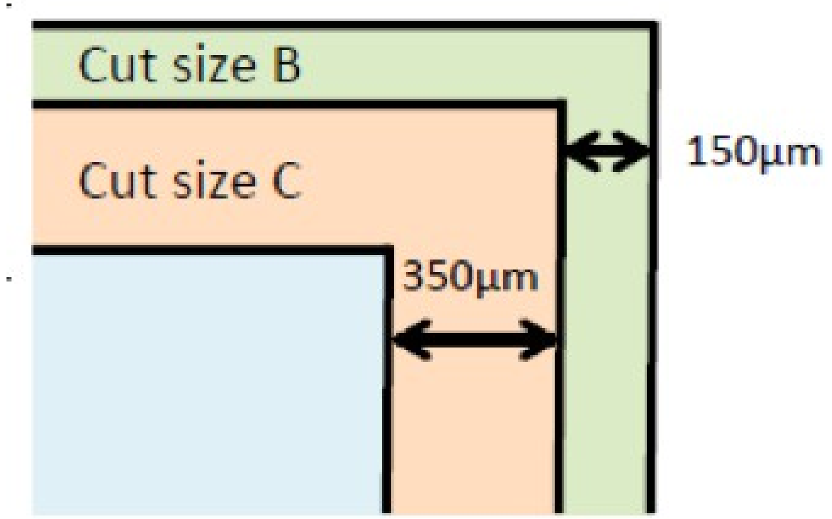
- In addition we require small leakage current:s under full depletion a few nA/pixel
  but for cost reasons we tolerate a certain fraction of pixels with higher leakage currents

- Vendors: OnSemi (CZ) and Russian company for physics prototype (~2003)
  Hamamatsu for technological prototype (since ~2010)
  Contacts with other vendors (e.g. LFoundry) hibernating mainly for funding reasons
  The drop-out of Infineon for the CMS HGCAL was/is bad news

SiW Ecal – Wafer R&D II

We (i.e. Mainly Kyushu) have tested several wafer types in previous years





- Cut size determine the actual sensitive area of a wafer
- Different designs mainly on test samples of "baby wafers"
- The "Hamamatsu" standard is still 0 or 1 full guard ring
  - 0 is "fake 0" guard ring, in fact there is still a small guard ring

Observations in recent years (see also backup for more details)

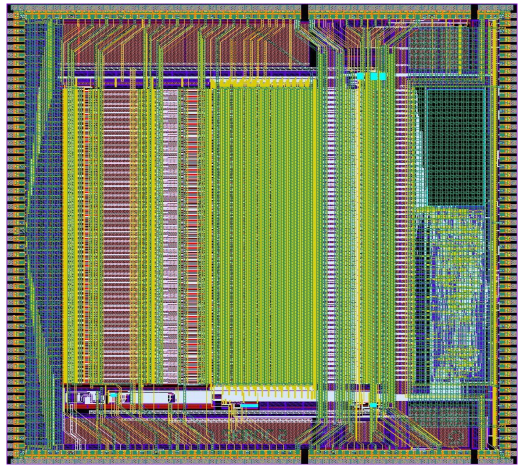
- Split or no guard ring lead to suppression of square events
- In prototype we still use full wafers with 0 or 1 guard ring
- General trend of reduction of bias voltage
- Can operate 500mum wafers at 60-80 V in full depletion

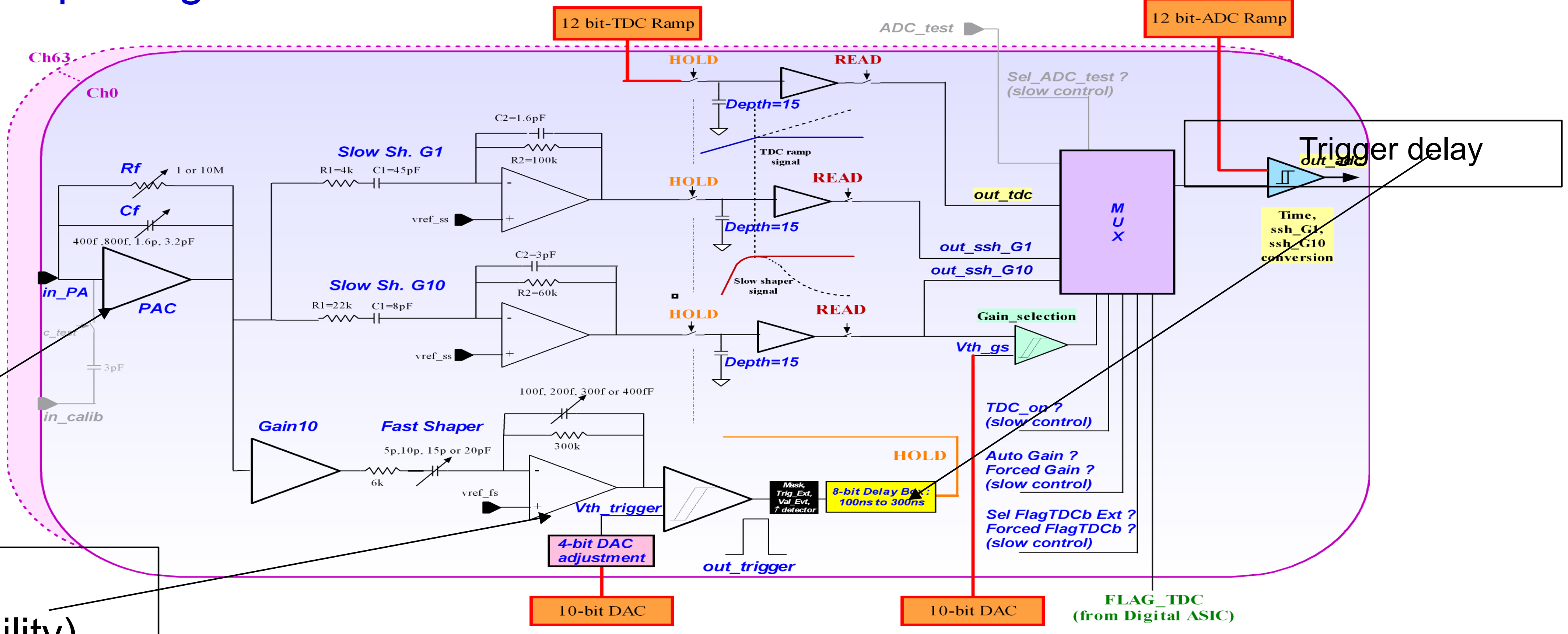
- Towards 8" wafers?
  - General trend (e.g. CMS) is to use 8" wafers
  - Larger surface/wafer =>smaller cost
  - Standard thickness 725mum
  - Impossible to get access to HPK production
  - Lines (CMS HGCAL Production)

SiW Ecal – Front end electronics

SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

- SiGe 0.35µm AMS, Size 7.5 mm x 8.7 mm, 64 channels
- High integration level (variable gain charge amp, 12-bit Wilkinson ADC, digital logic)
- Large dynamic range (~2500 MIPS), low noise (~1/10 of a MIP)
- Auto-trigger at ½ MIP, on chip zero suppression
- Low Power: (25µW/ch) power pulsing





Preamplifier
(adjustable gain)

Internal trigger
(self-triggering capability)

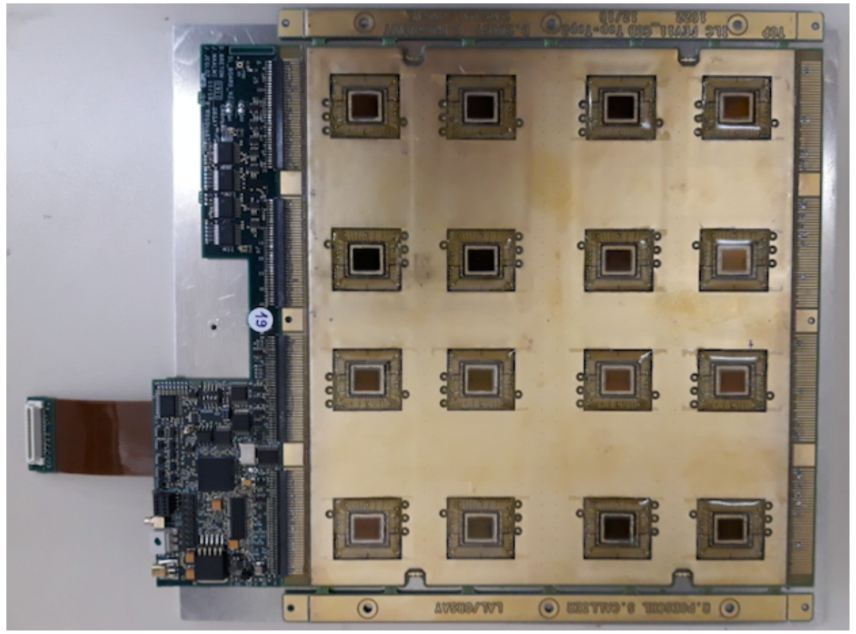
Prologue – “The FEV Zoo”

- In recent years the SiW ECAL has developed and used several PCB variants
  - To make sure that you don't get lost, here comes an introduction

FEV10-12

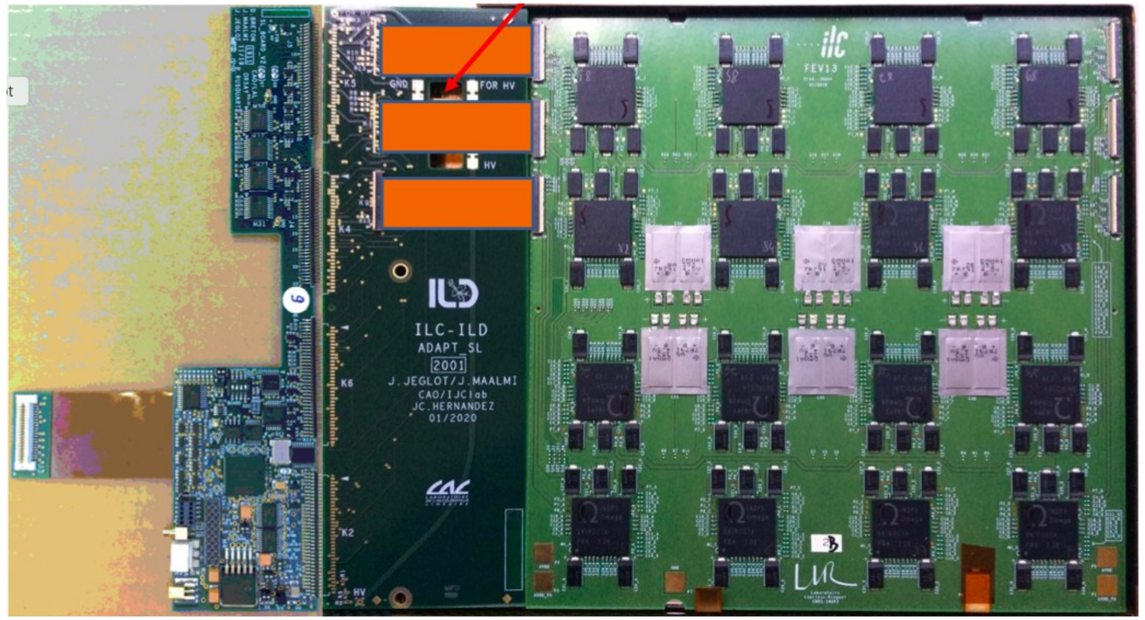
- ASICs in BGA Package
- Incremental modifications From v10 -> v12
- Main “Working horses” since 2014

FEV_COB



- ASICs wirebonded in cavities
  - COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

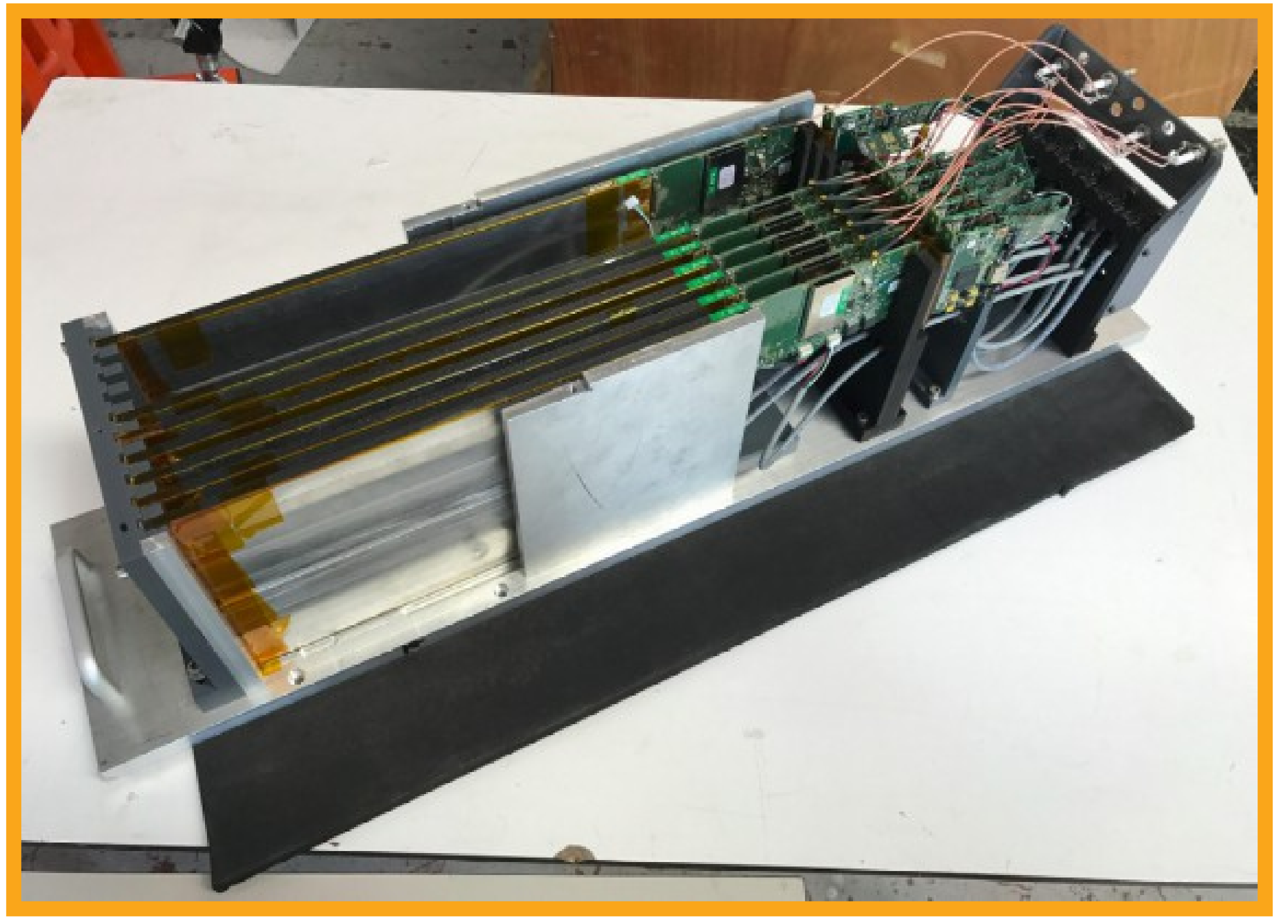
FEV13



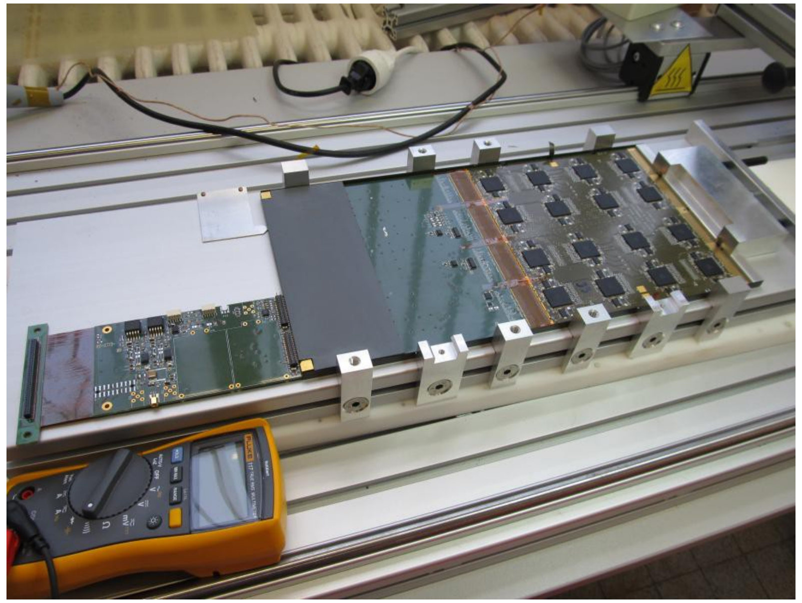
- Also based on BGA packaging
- Different routing than FEV10-12
- Different external connectivity

Current prototype (see later) is equipped with all of these PCBs

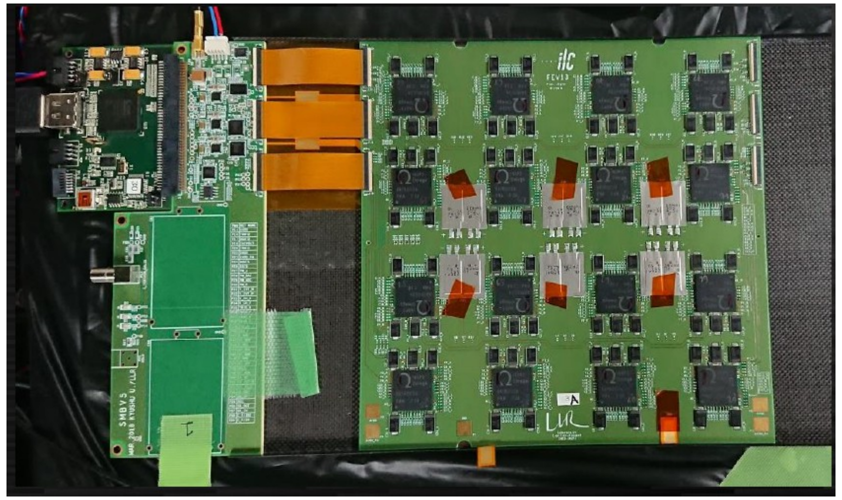
Prototypes until ~2018



- Total ~15 layers constructed
  - Max of ten tested within one stack
- 1024 channels per layer
- Assembly chains in France and Japan
- Beam tests at DESY and CERN since 2016



PCB FEV10-12
with long adapter card
Wafer thickness
325 µm

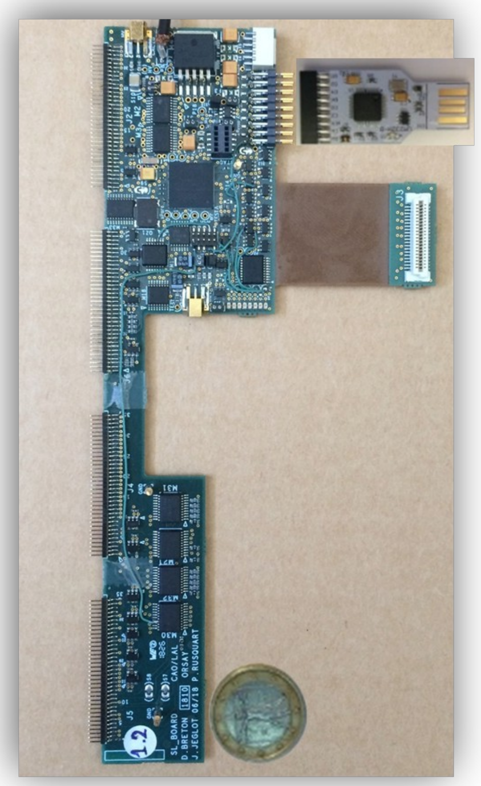


PCB FEV13
with small(er) adapter card
Wafer thickness
650 µm

R&D for thin PCB see backup

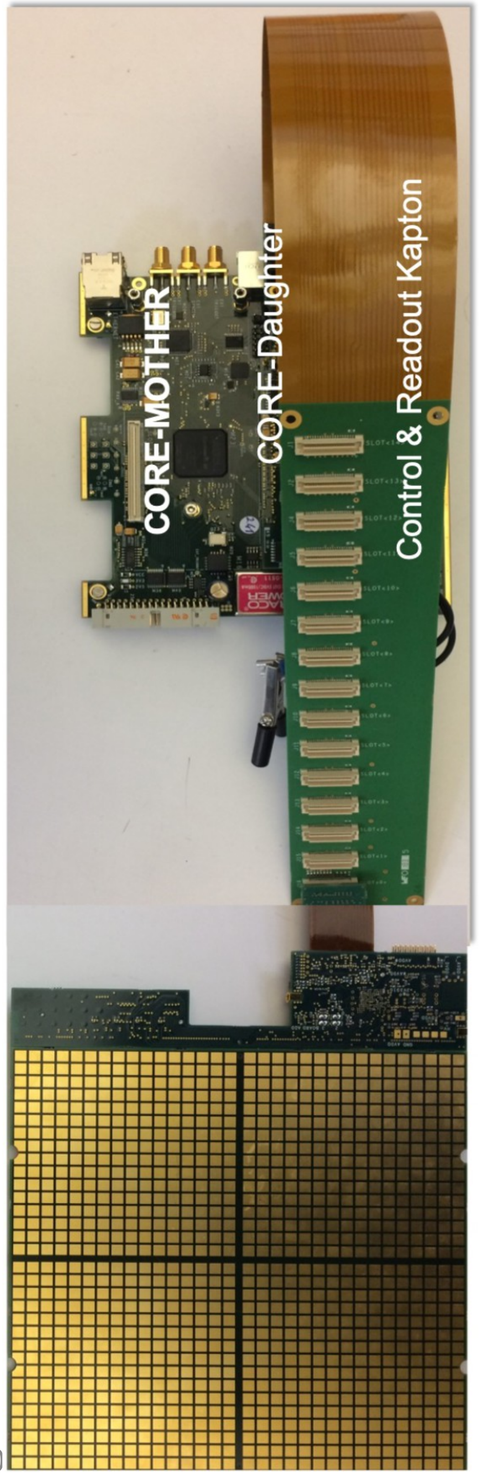
Compact readout

Current detector interface card (SL Board) and zoom into interface region

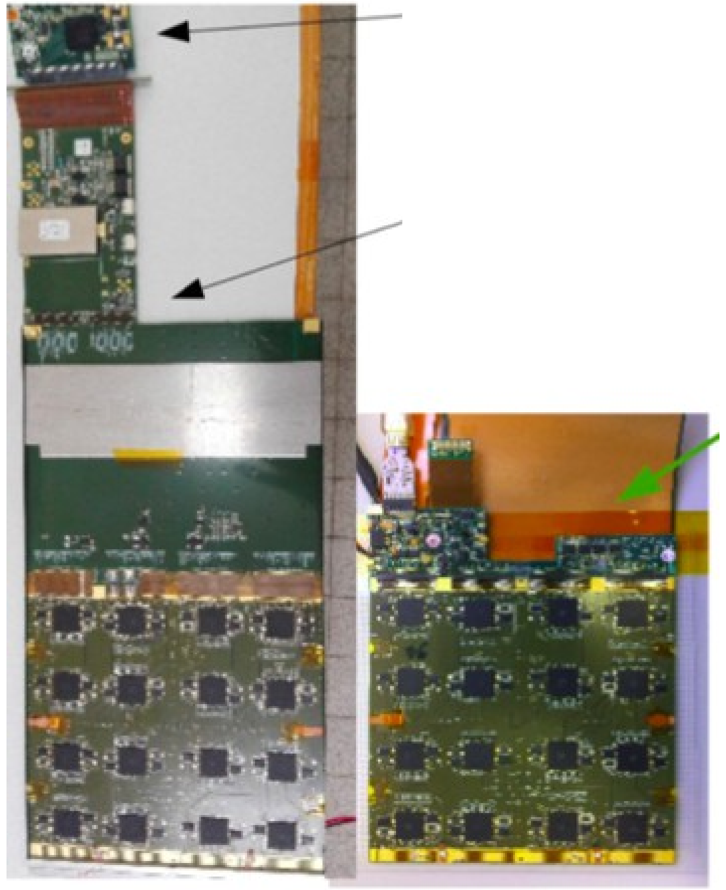


SL Board

Complete readout system

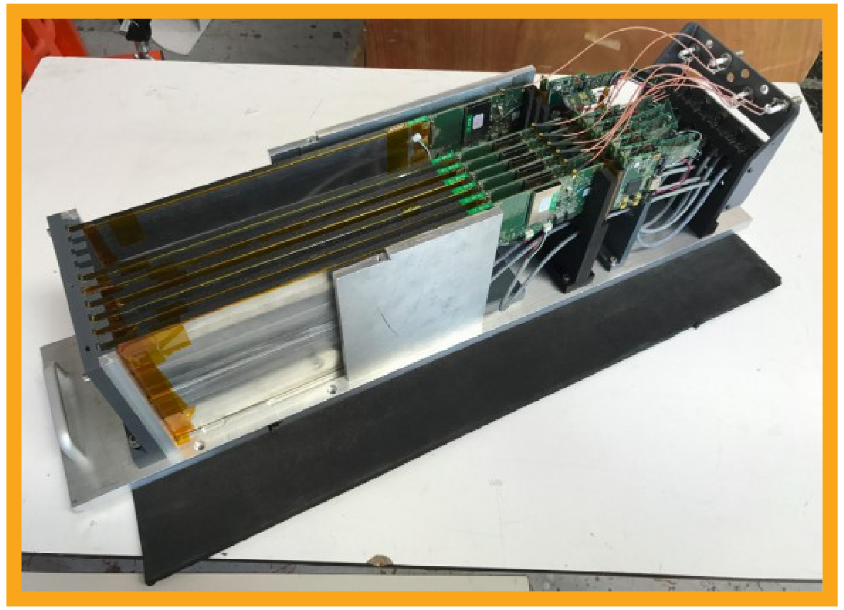


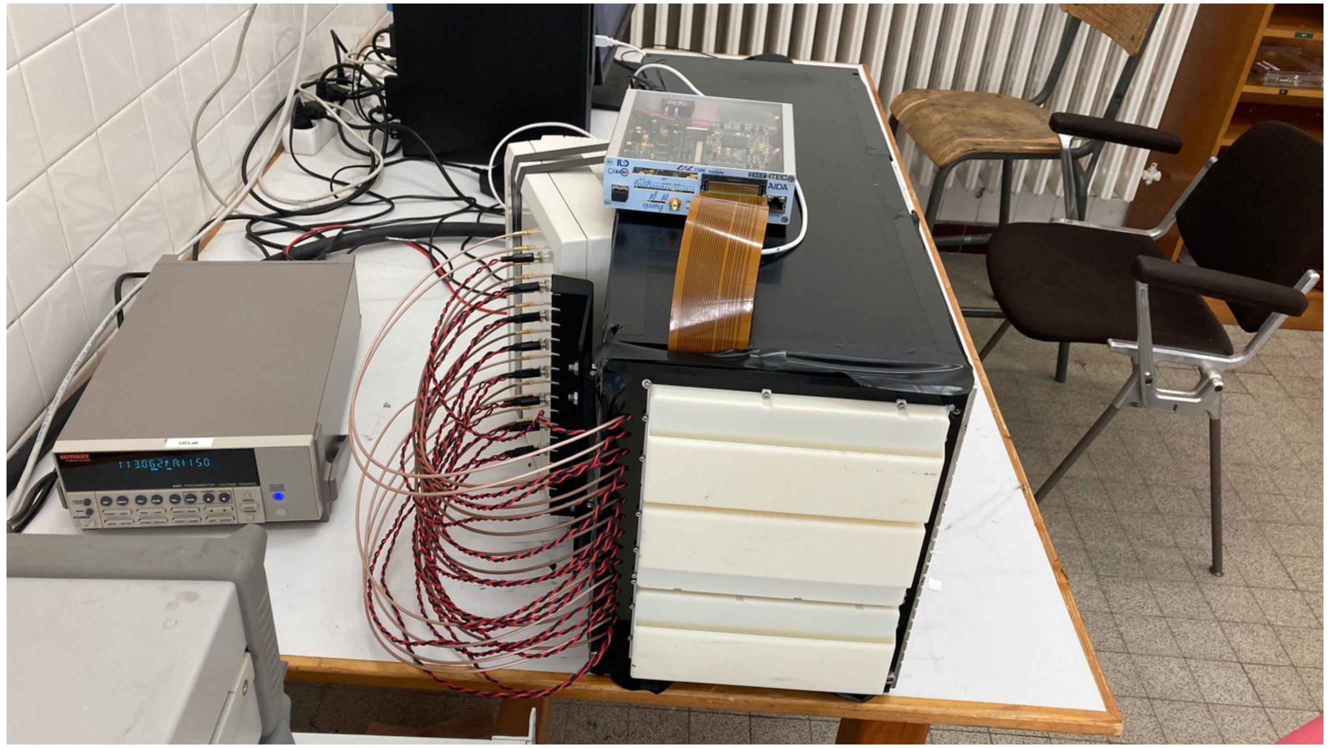
For reference
Comparison old/new r/o system



- “Dead space free” granular calorimeters put tight demands on compactness
  - Current developments in for SiW ECAL meet these requirements
- System allows to read column of 15 layers <-> to be expected in ILD
  - Important that full readout system goes through scrutiny in beam tests

SiW ECAL 2018 -> 2022



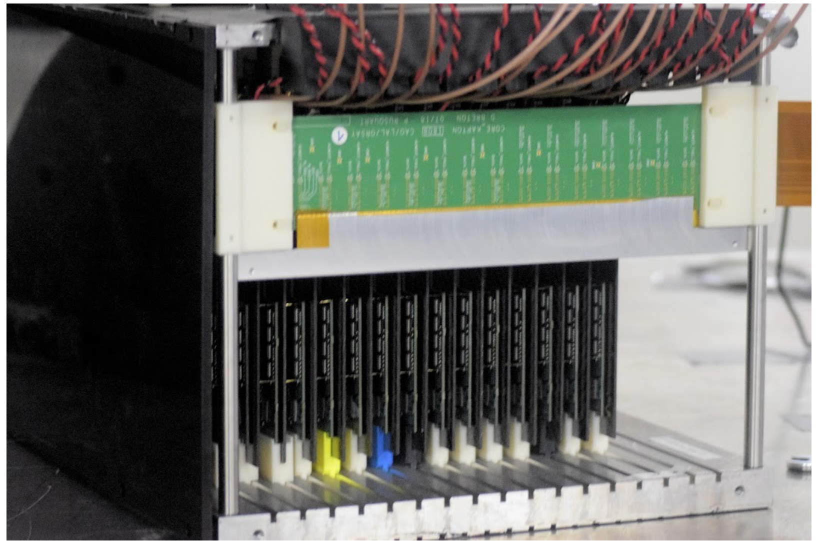


- 7 short layers (18x18x0.5cm^3)
- 1024 channels per layer => 7186 cells
  - Assembly chains in France and Japan
  - Beam tests at DESY and CERN since 2016

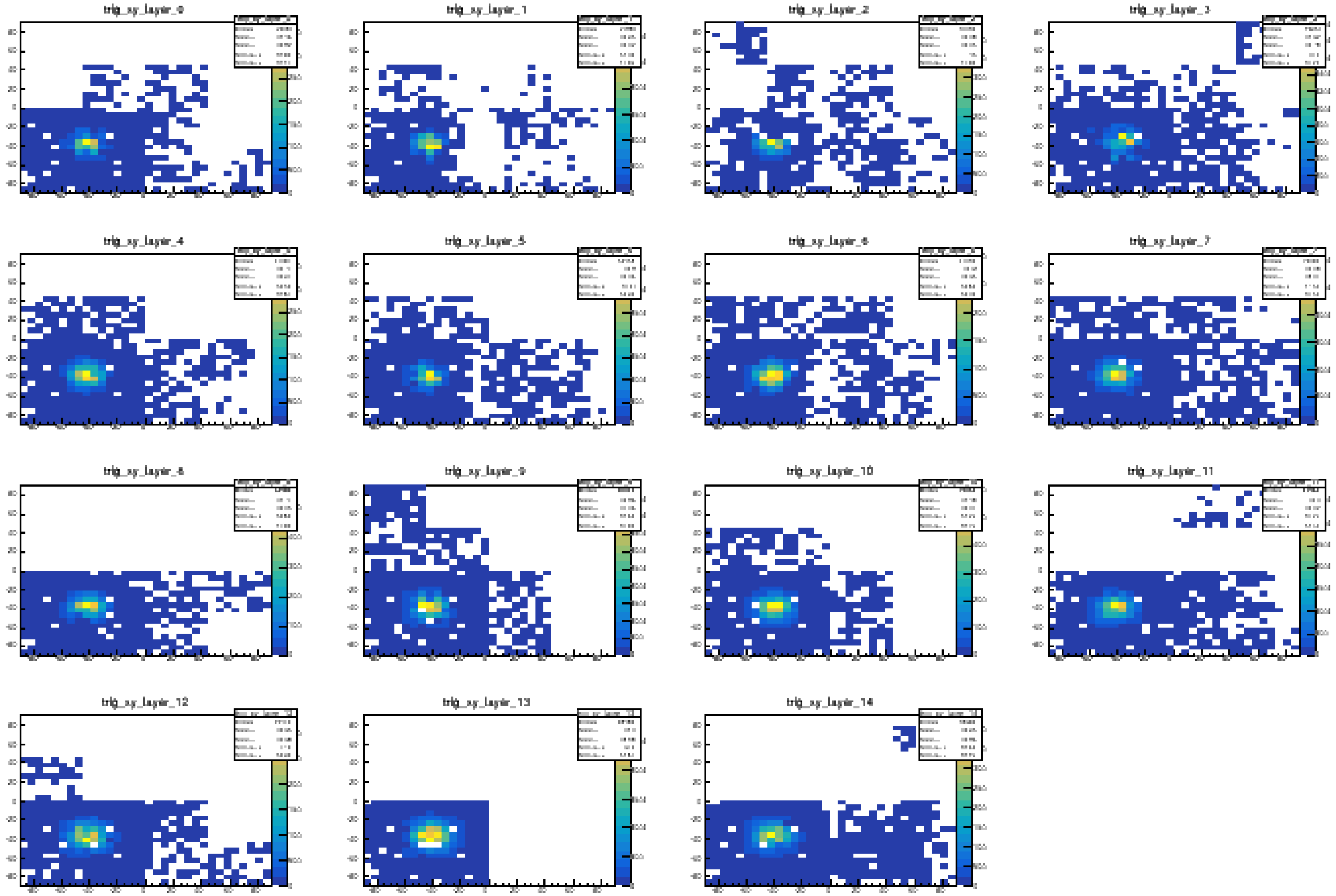
- 15 layers equivalent to 15360 readout cells
- Overall size 640x304x246mm^3
  - Commissioned in 2020 and 2021
  - Testbeams (finally) in November 2021 and March 2022
  - 1.5 years in waiting loop due to pandemic

SiW-ECAL in beam test @ DESY

Detector Setup



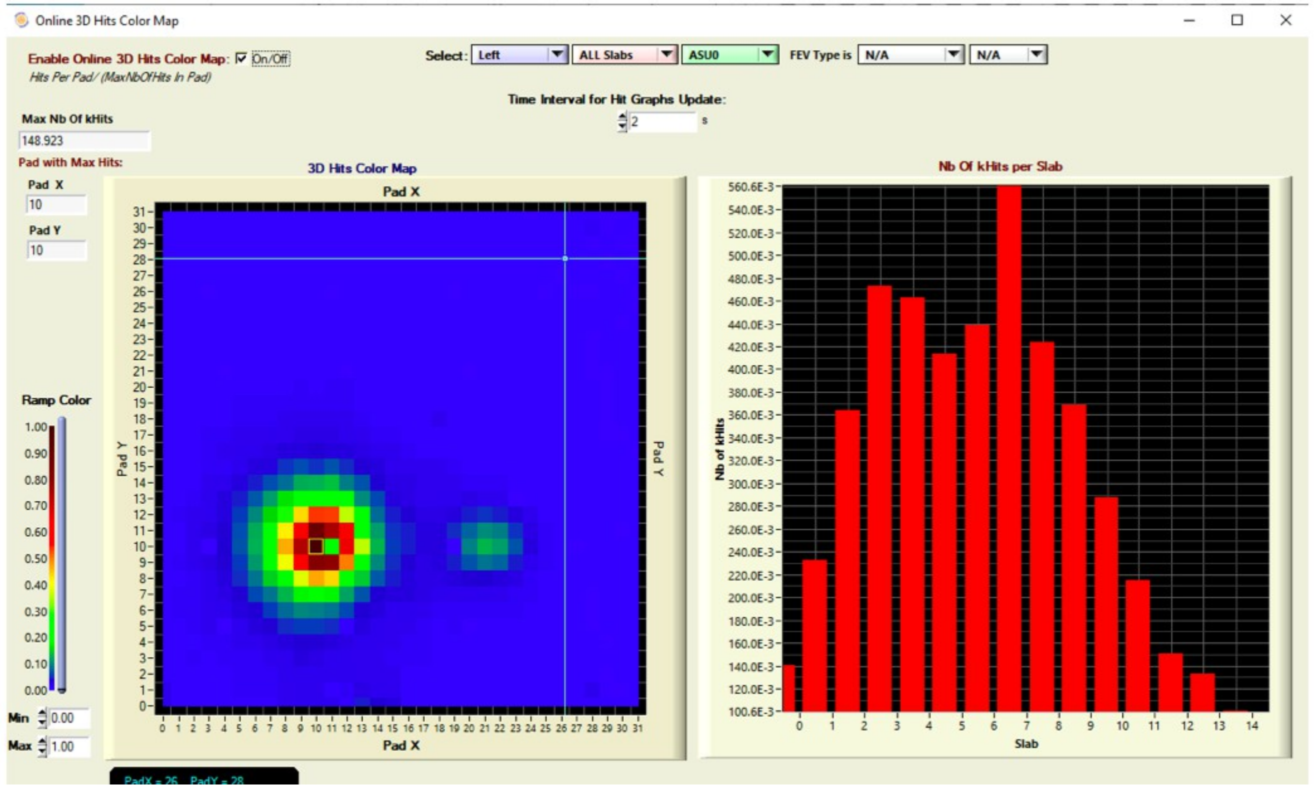
Detector in beam position



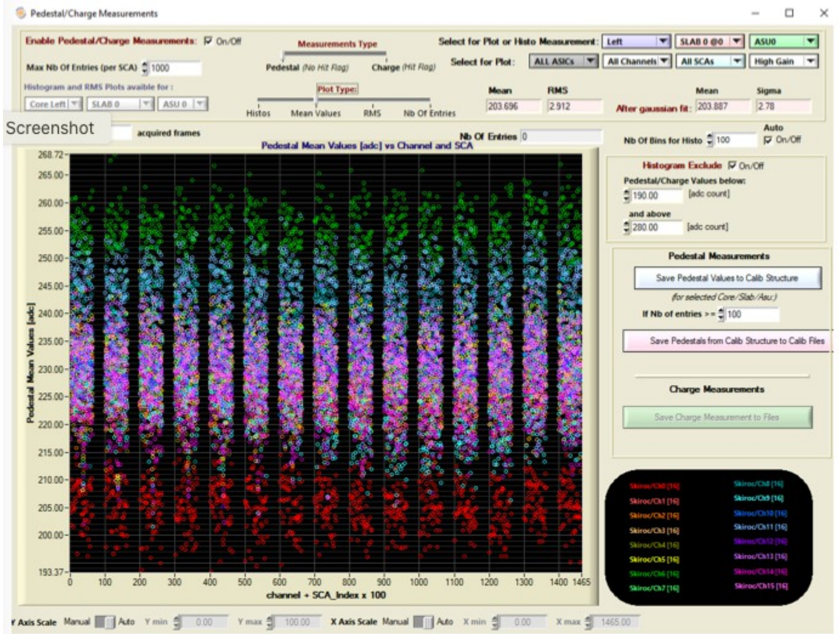
- Stack operational
- Beam spot in 15 layers

SiW-ECAL Beam test – Online Monitoring

Jihane Maalmi, CALICE Meeting Valencia



- Online Hit Maps and shower profiles
- Allow for real time beam and detector tuning
  e.g. Adaptation of beam rates or thresholds



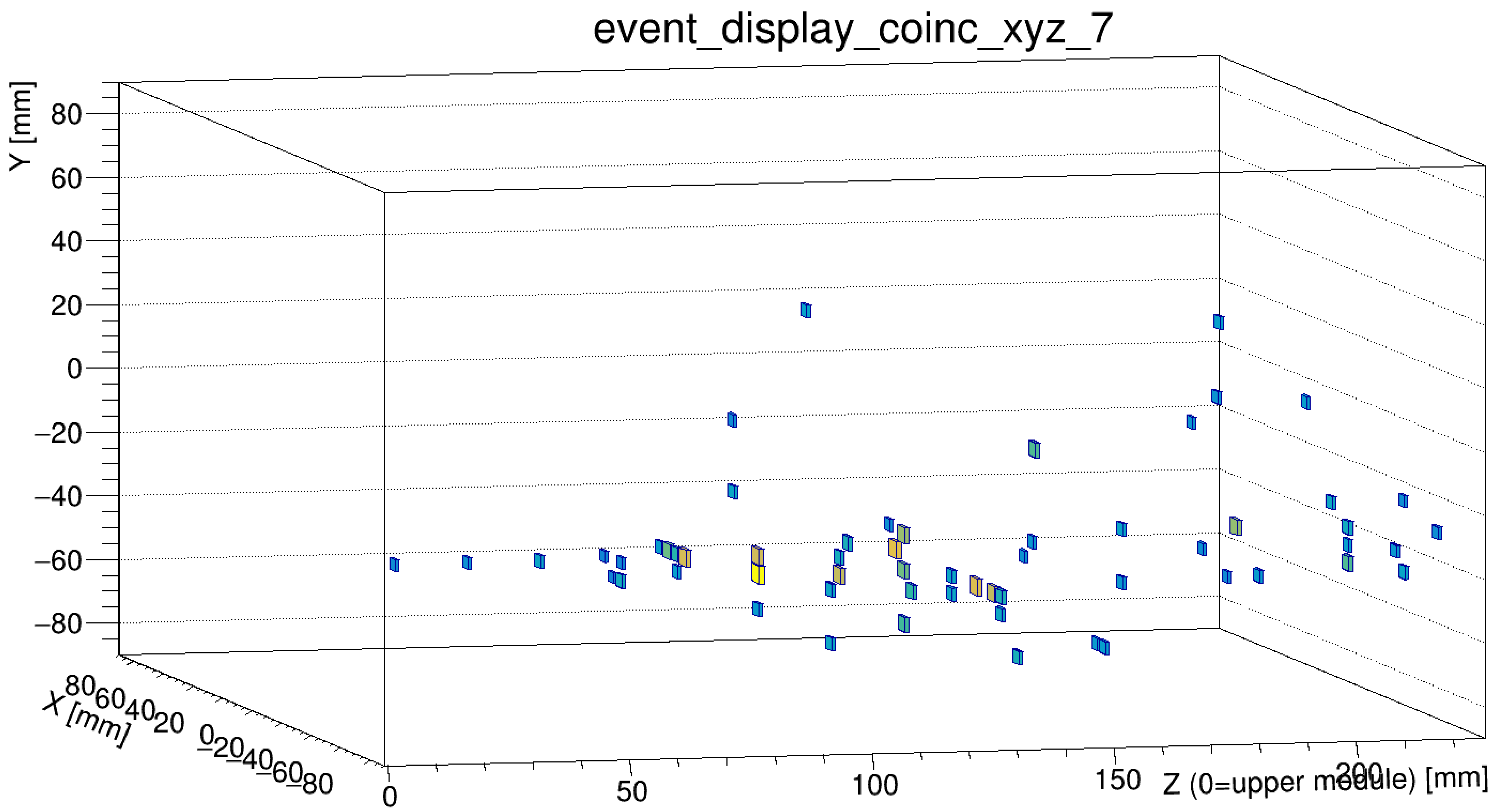
- Further online tools

- Pedestal measurement and subtraction
- Charge measurement and histogramming
- MIP gain correction

These are just a few examples from the powerful online suite

SiW-ECAL Beam test – Onlline/Offline Event Displays

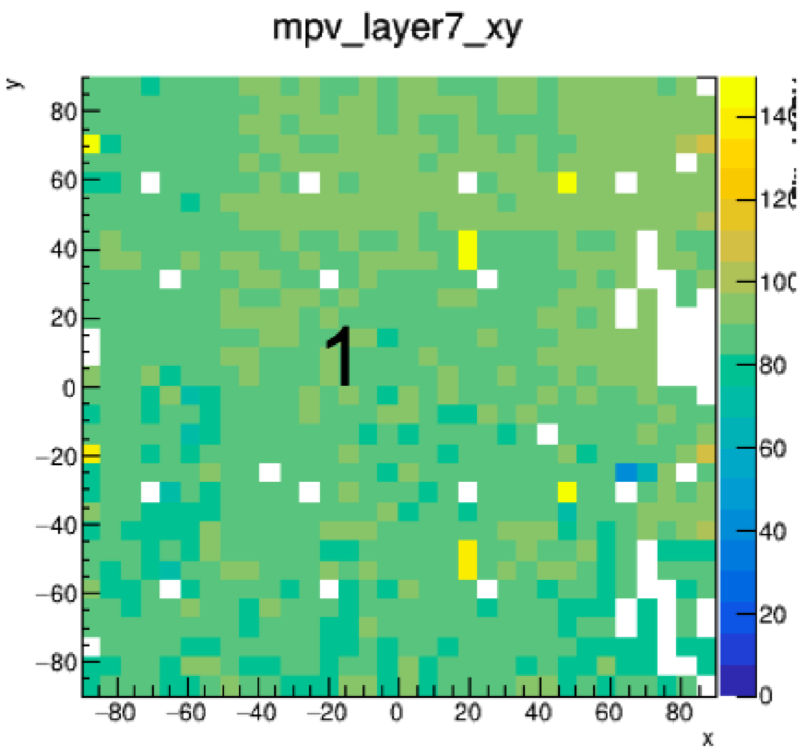
Jonas Kunath

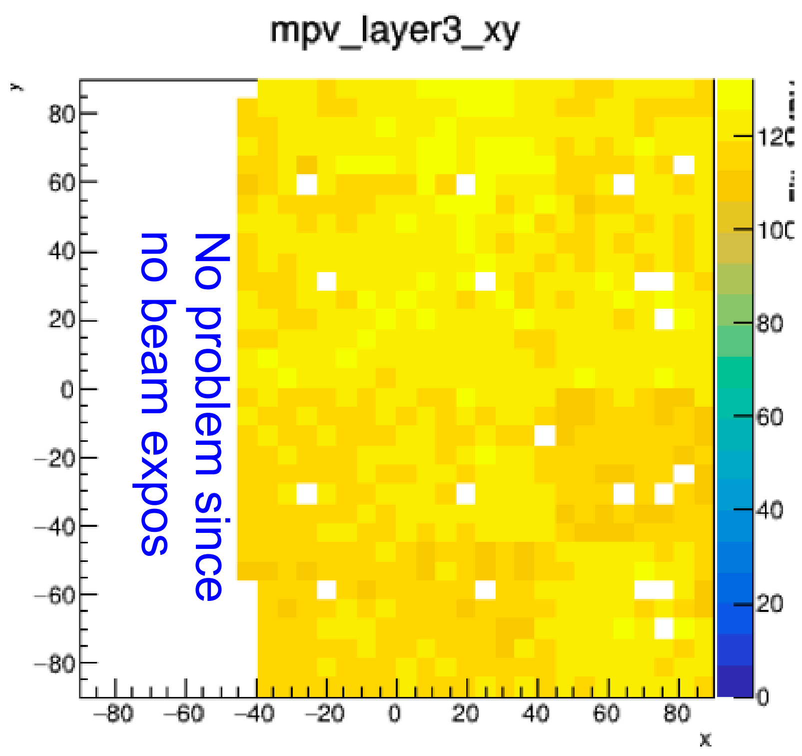


- Clear showers measured during beam test campaigns
- Require full event reconstruction
- These (and more) “high level” views are available already while a run is going on

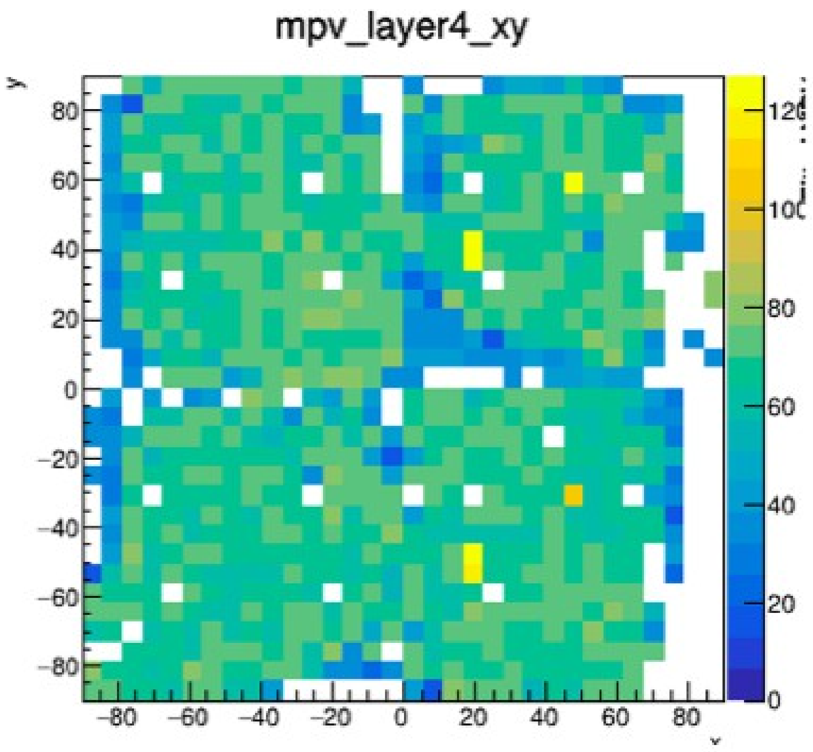
SiW-ECAL Beam test – First feedback

Adrian Irles





- We have good layers ...
  - Homogeneous response to MIPs over layer surface
  - Here white cells are masked cells due to PCB routing
    - Understood and will be corrected

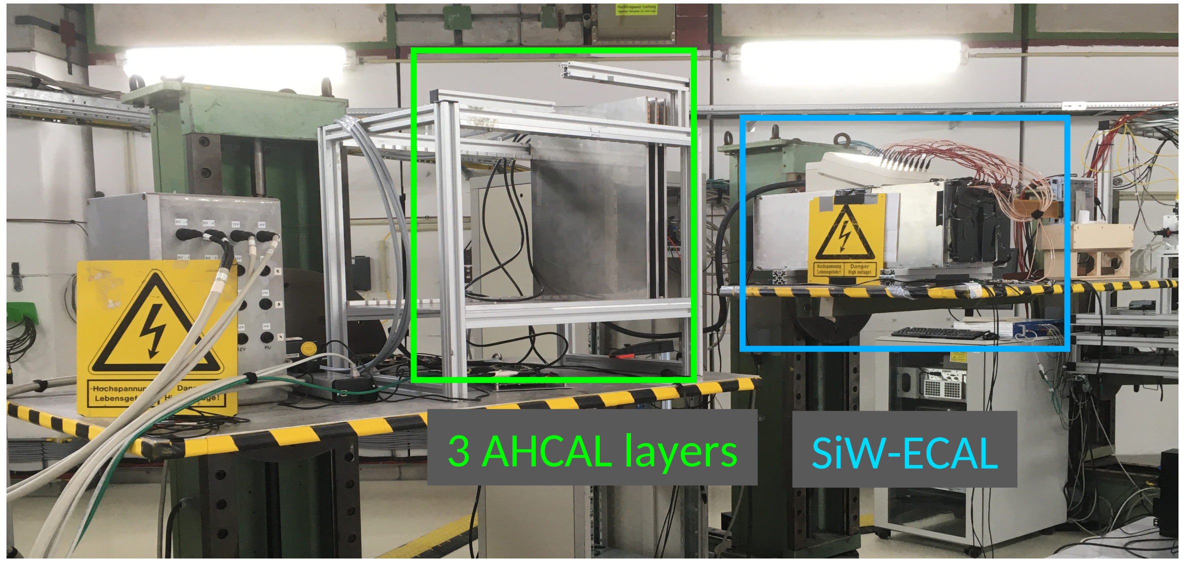


... and not so good layers

- Inhomogeneous response to MIPs
  - Partially even no response at all, in particular at the wafer boundaries
  - To be understood, may require dedicated aging studies
- Have since last week access to the different stages of the ASICs
  - => major debugging tool
- In any case less good layers will be replaced in coming months

Common testbeams

Preparation for common SiW-ECAL AHCAL beam test

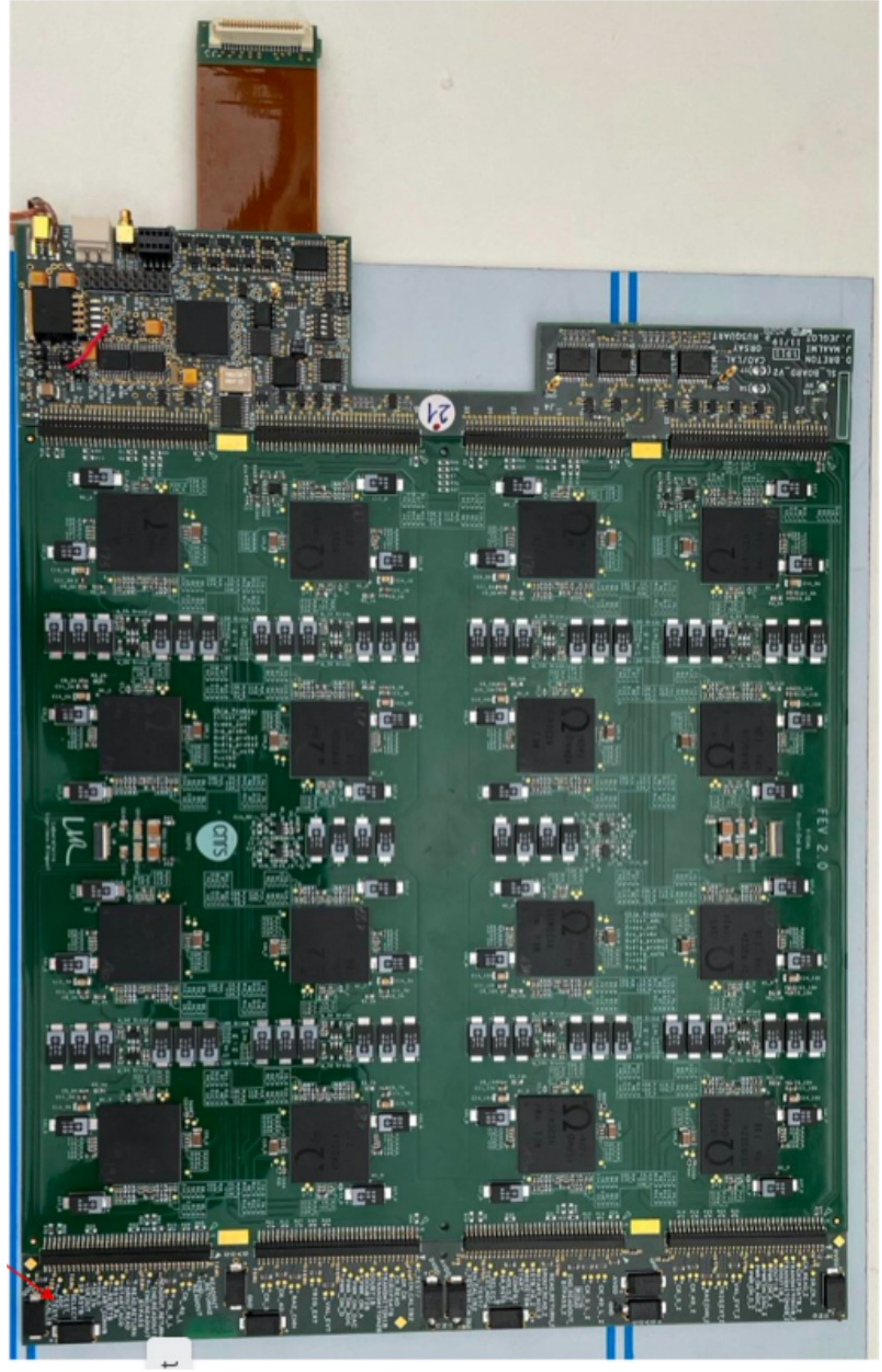


SiW-ECAL + AHCAL DAQ test @ DESY in March 2022

- Successful synchronisation of data recorded with SIW-ECAL and AHCAL
- Common running makes full use of EUDAQ tools (developed within European projects)

New PCB – FEV2.x

LLR, IJCLab, LPNHE, OMEGA



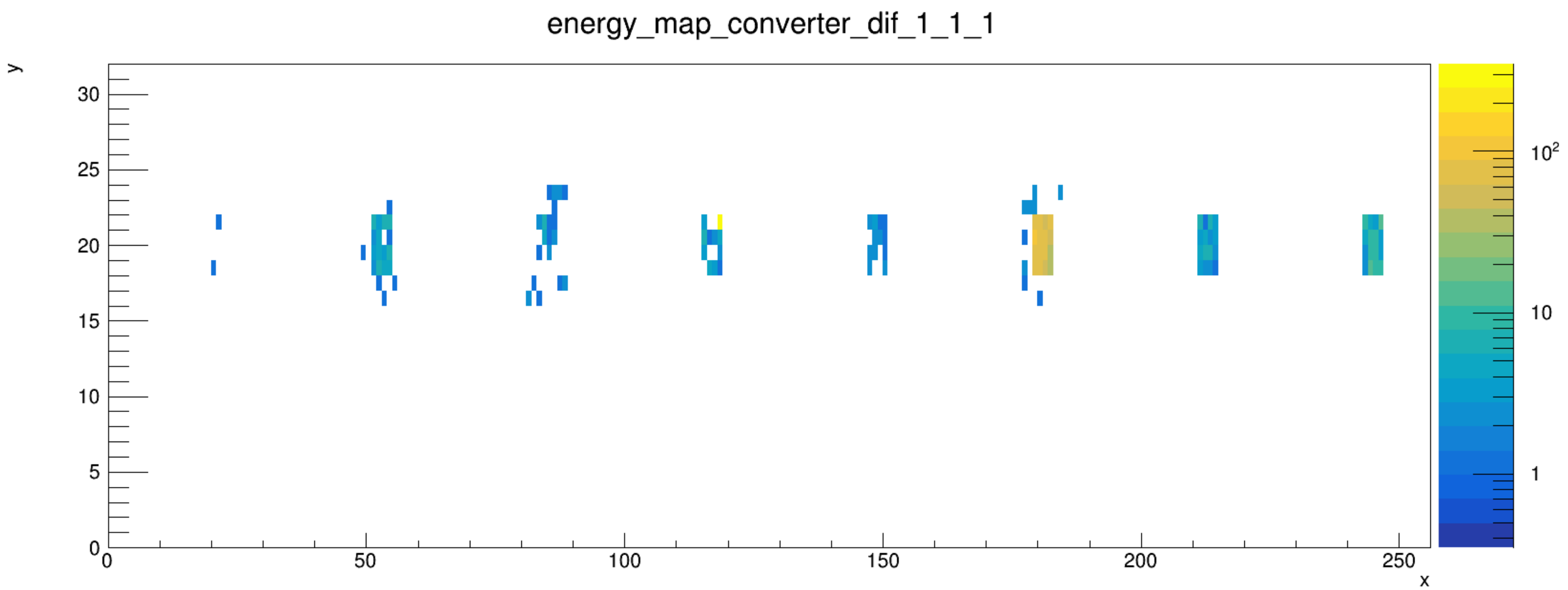
- Improved Layout
  - Better shielding of AVDD and AVDD PA plans and minimisation of cross-talk between inputs and digital signals.

- Power Pulsing Mode: new philosophy
  - limiting the current through the Slab (current limiter present on the SL Board) to:
    - avoid driving high currents through the connectors and makes the current peaks **local** around the SKIROCs chips
    - avoid voltage drop along the slab
    - ensure temperature uniformity
  - We add large capacitors with low ESR for **local** energy storage (around each SKIROC chip)
  - Generate **local** power supply with LDO (Low Drop Out) to avod voltage variations

- Clean clock distribution all over the slab
  - for Slow Control and Readout Clocks
- Parallel configuration and readout over 2 partitions.
- Driving high voltage up to 350V for 750µm wafer (via the ASU connectors)
  - Adding a filter for each wafer HV and limit the current in case of wafer failure

Reminder – Electrical long slab

Chain of
8 detection elements
~3m

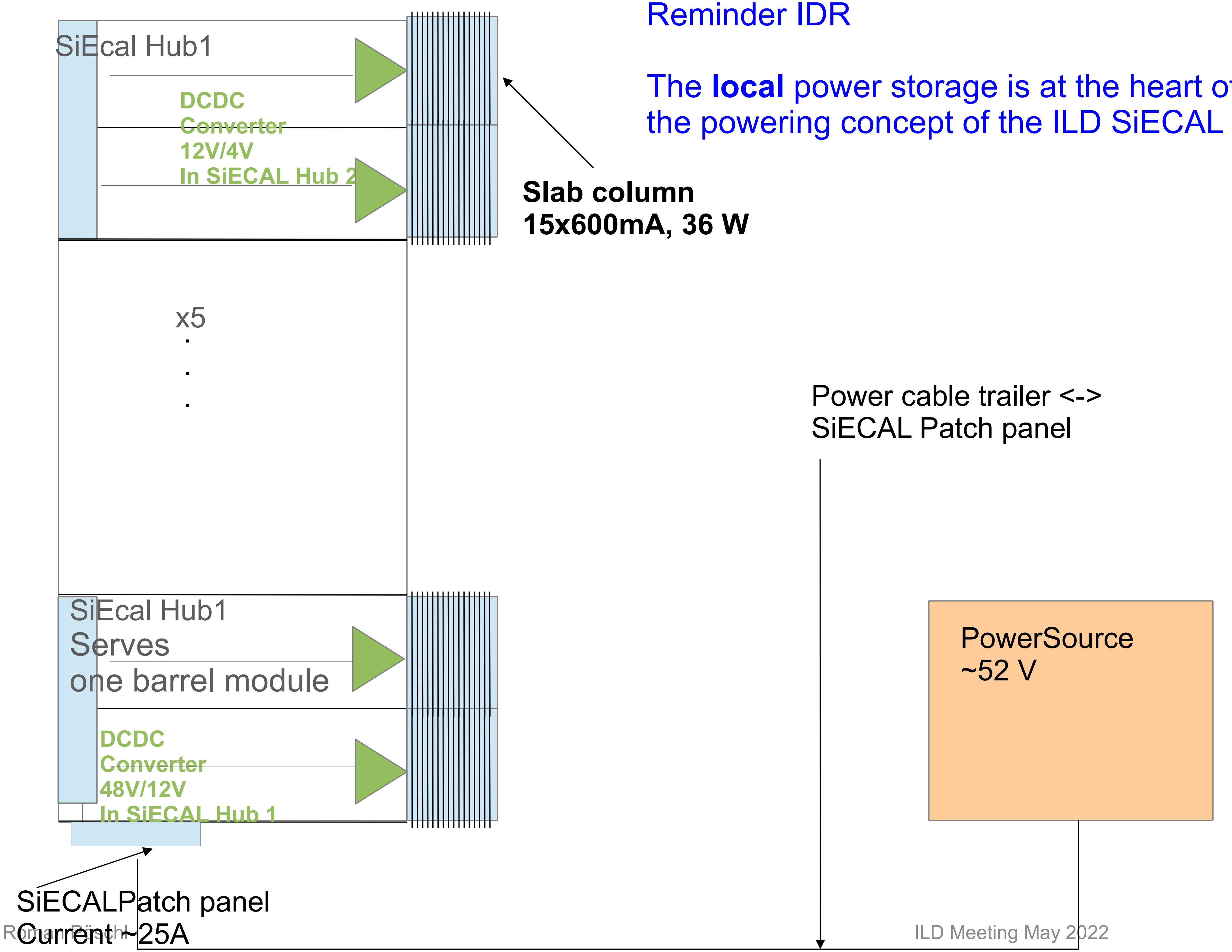


- Very encouraging results in first beam test in 2018
  - Credibility for concept as foreseen for e.g. ILD
  - Issues with signal drop towards extremities
- Long slab studies will be resumed with new FEV
  - Adapted for power pulsing, will avoid voltage drop, etc ...

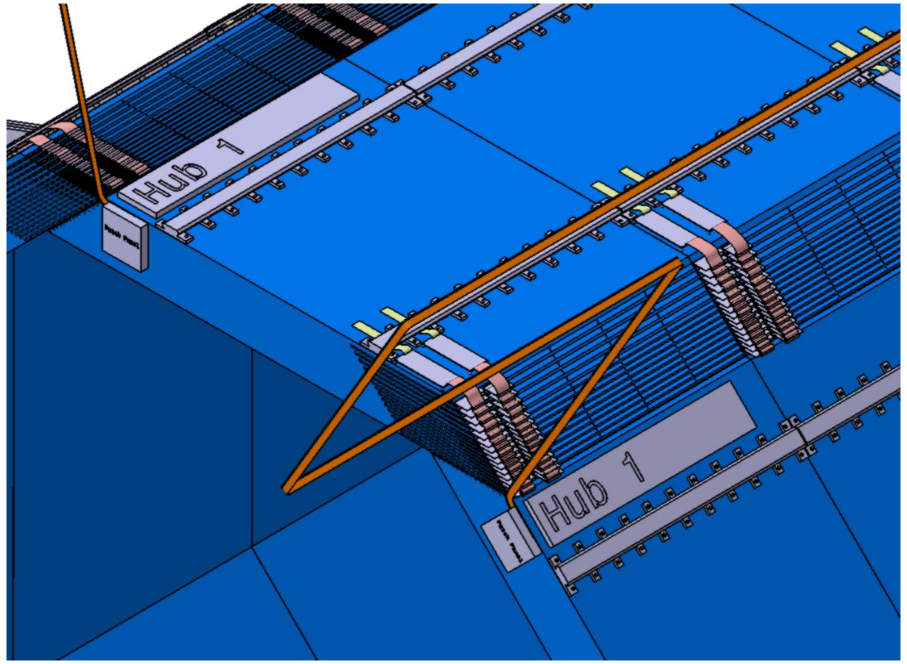
Powering concept/management – ILD SiECAL

Reminder IDR

The **local** power storage is at the heart of the powering concept of the ILD SiECAL



Zoom into ILD Ecal barrel



- Total average power consumption **20 kW** for a calorimeter system with 10^8 cells*
  - Only possible through PP
- The art is to store the power very locally
- Issue for upcoming R&D

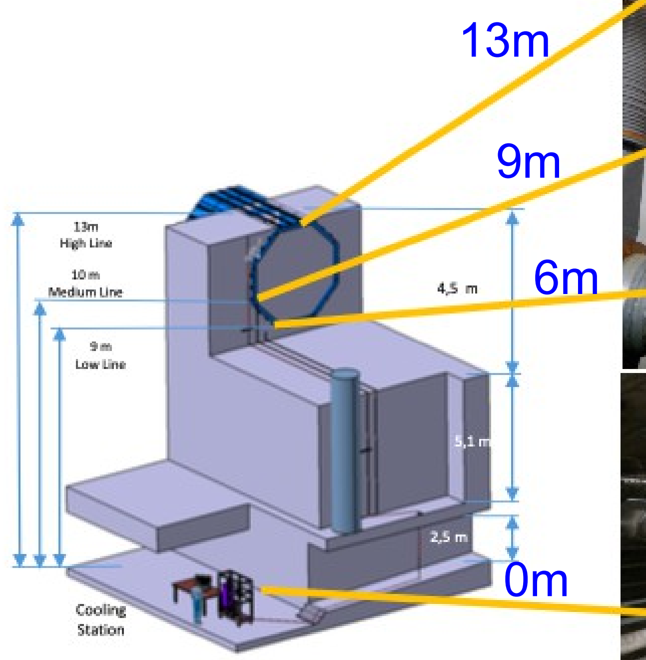
*Compare with 140 kW for CMS HGCAL FEE $6x10^6$ cells

Powering concept/management – ILD SiECAL

Demonstrator of large leakless loop for CALICE/ILD ECAL

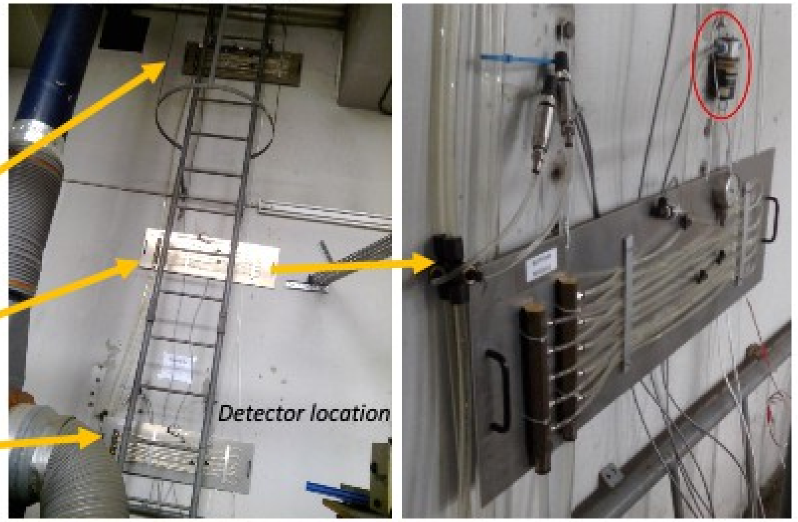
- Thermal model as milestone
- Probes at different heights to establsih full model of Cooling system for large detectors

a large leak-less cooling-loop



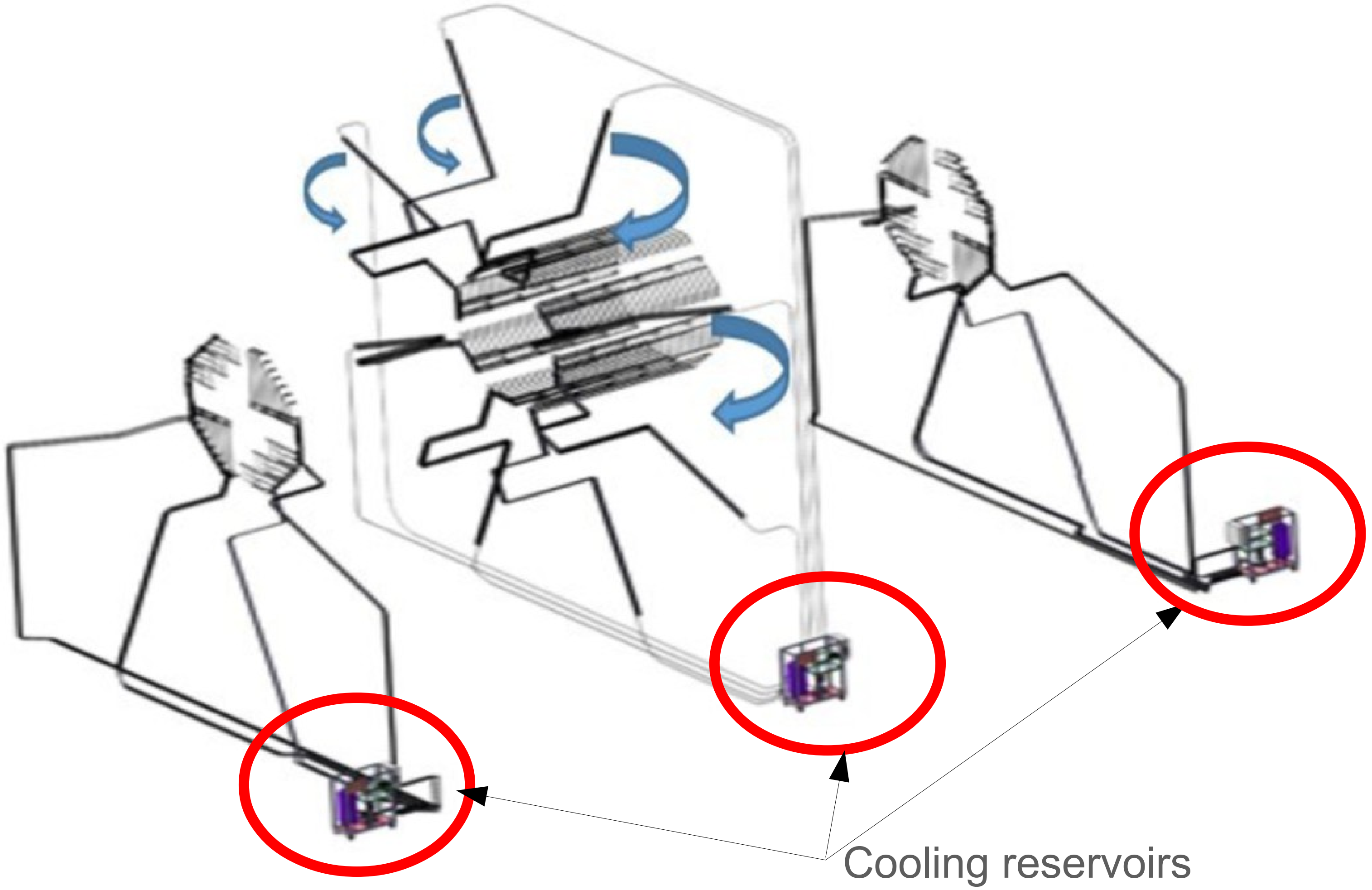
LPSC cooling test area with a drop of 13 m

Upper part of the experiment

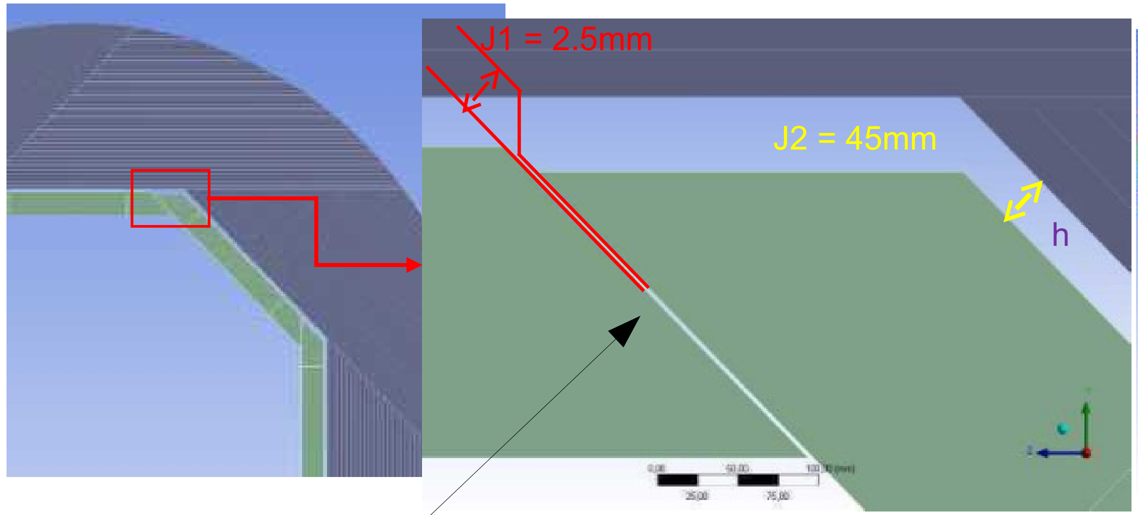


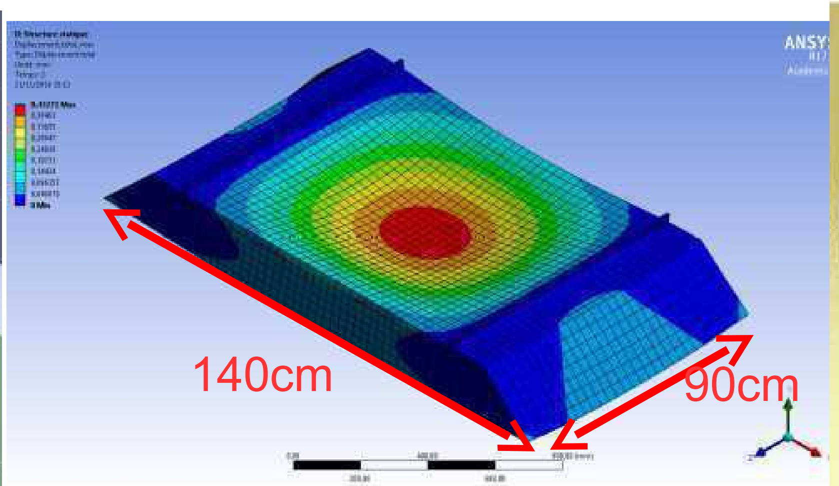
Julien Giraud

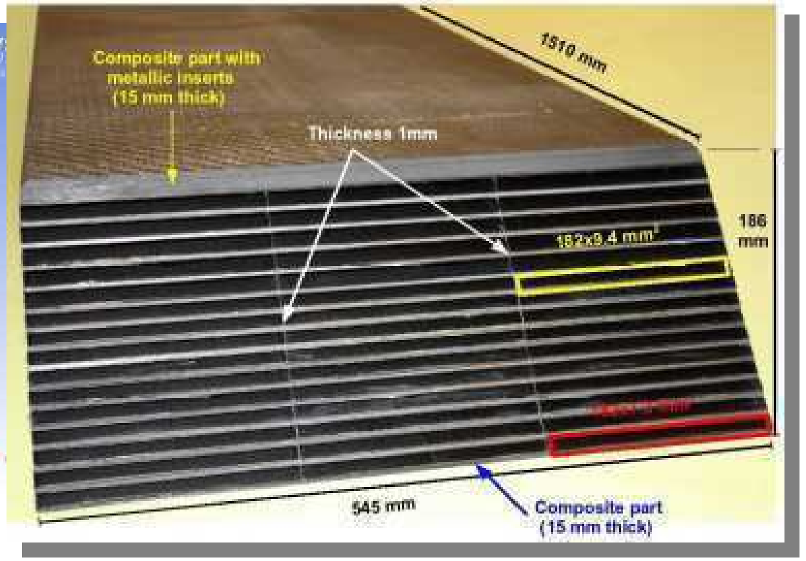
Studies for efficient leak detection Ongoing (Polarographic probe)



ILD SiECAL – Mechanical structures and studies



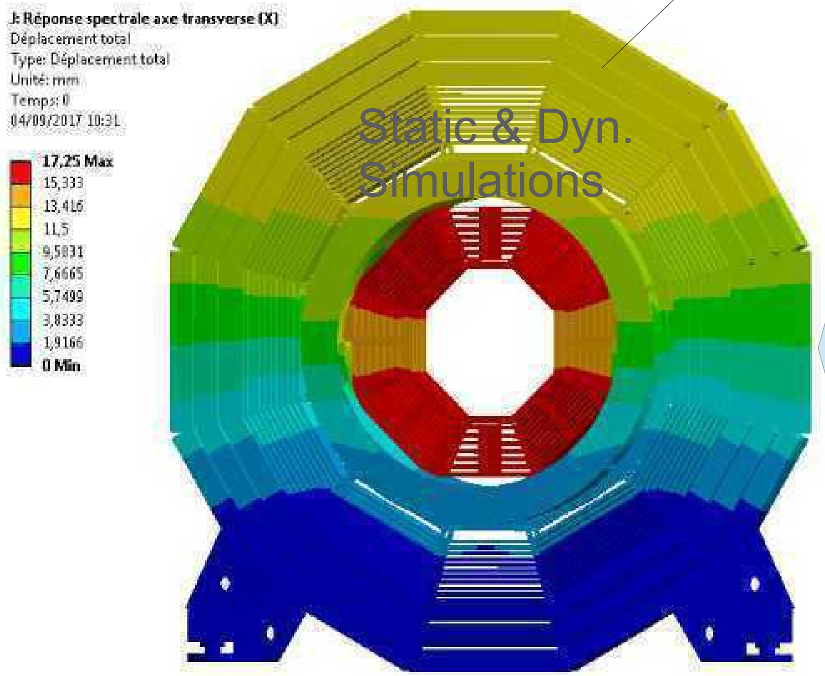


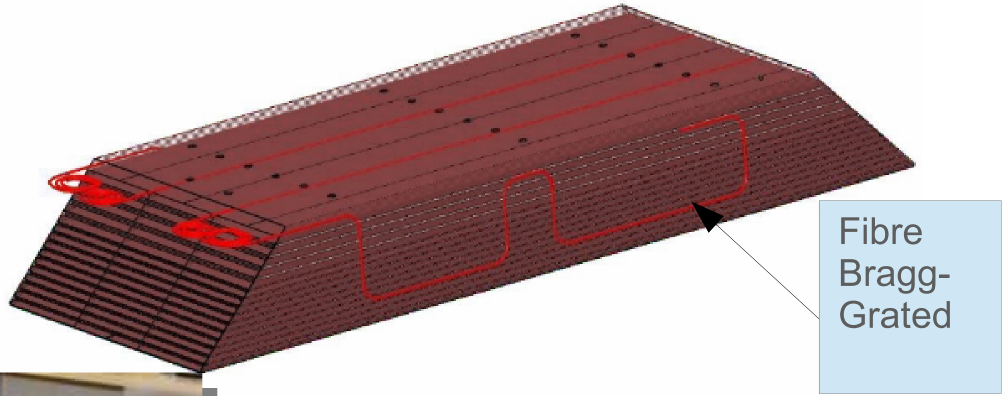


J1 = clearance between modules for the ECAL

J2 = Clearance at ECAL edges between ECAL and HCAL

h = height of the rails 30mm





measurements still to be done...

Intermediate summary

- Successful operation of a fifteen layer stack in two beam tests at DESY
  - Major milestone for technological prototype
  - Demonstration of performance of compact DAQ
  - Rich set of data to study detector performance
  - Have already precious feedback on strong points but also of weak spots
    - The inhomogeneity in the layer response is a matter of concern
    - Debugging has started

- Powerful infrastructure to conduct conclusive system tests now and in coming years

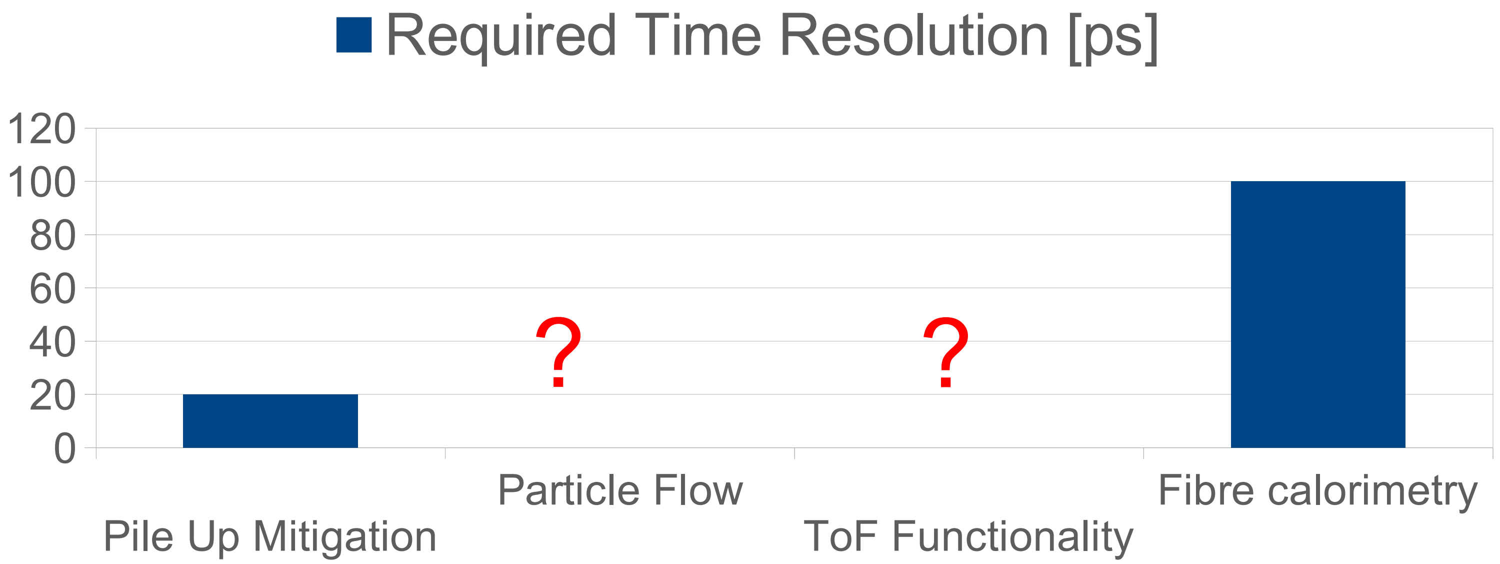
- New type of PCBs will allow for finalising the R&D needed for ILD
  and for bringing us to the “eve” of an engineering prototype in the next around two years
  - Sufficient support provided ... the team is working at the limit
  - We need in particular more people for data analysis

- Advanced engineering studies

- What else, what's next?

Timing ?

- Timing is a wide field
- A look to 2030 make resolutions between 20ps and 100ps at system level realistic assumptions
- At which level: 1 MIP or Multi-MIP?
- For which purpose ?
  - Mitigation of pile-up (basically all high rate experiments)
  - Support of PFA – unchartered territory
  - Calorimeters with ToF functionality in first layers?
    - Might be needed if no other PiD detectors are available (rate, technology or space requirements)
    - In this case 20ps (at MIP level) would be maybe not enough
  - Longitudinally unsegmented fibre calorimeters



- A topic on which calorimetry has to make up it's mind
  - Remember also that time resolution comes at a price -> High(er) power consumption and (maybe) higher noise levels

Shower development in CALICE Type Calorimeters

Shower reconstruction

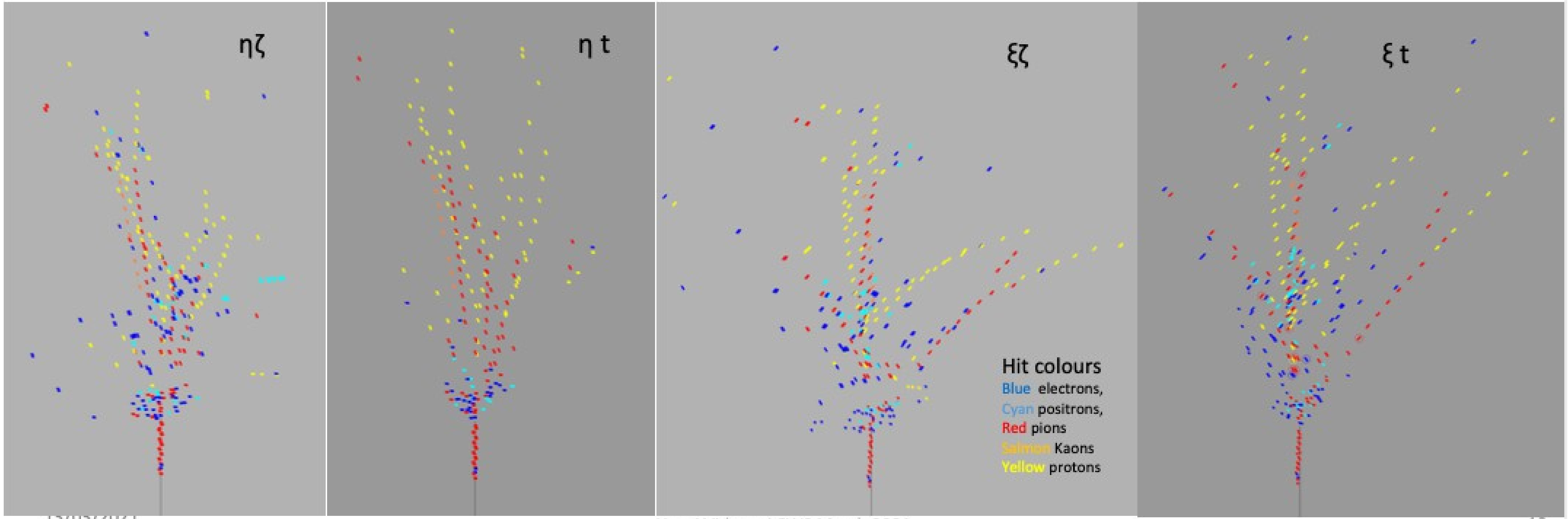
It is known that the more dimensions, the easiest to reconstruct patterns

Using the time-space

To figure out the pattern of a shower developed by a charged track or a neutral
We assume that the main direction of the shower, called ζ, is
- along the flight line from interaction to the earliest hit in the Ecal (or globally) for a neutral
- along the track direction at the position of the earliest hit for a charged track

Two perpendicular coordinates, ξ and η, are chosen to optimise the match with the detector axes, mostly for visualisation.
Then t which is much correlated to ζ.

You see immediately
the role of the β
and how the protons slow down
when the pions do not



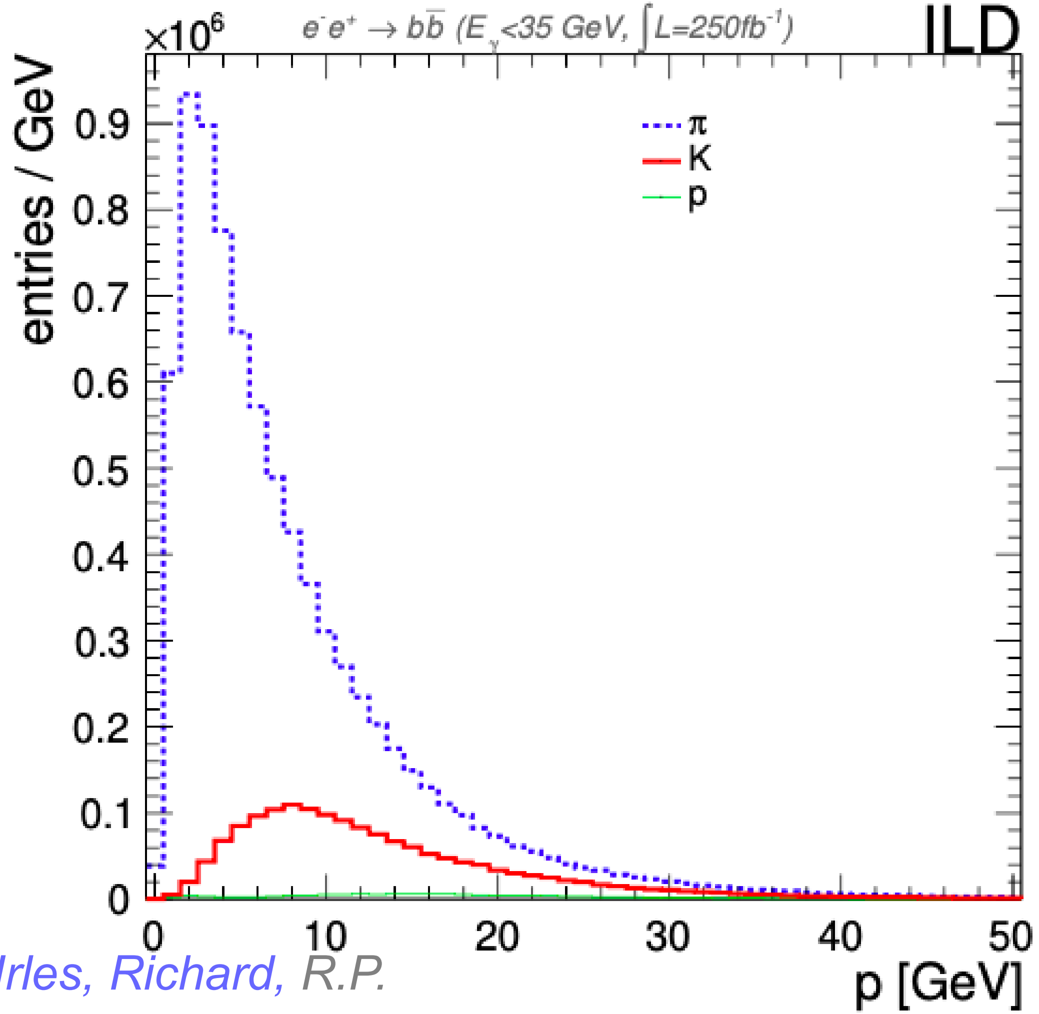
15/03/2021 Henri Videau LCWS March 2021 12

H.Videau et al., LCWS2021

arxiv:2108.10963

Calorimeters with ToF Functionality?

Momenta and abundance of pi/K/p in ee->bb @ 250 GeV



ILD: Irles, Richard, R.P.

Available time resolution with calos

Difference in ToA at ILD Calos

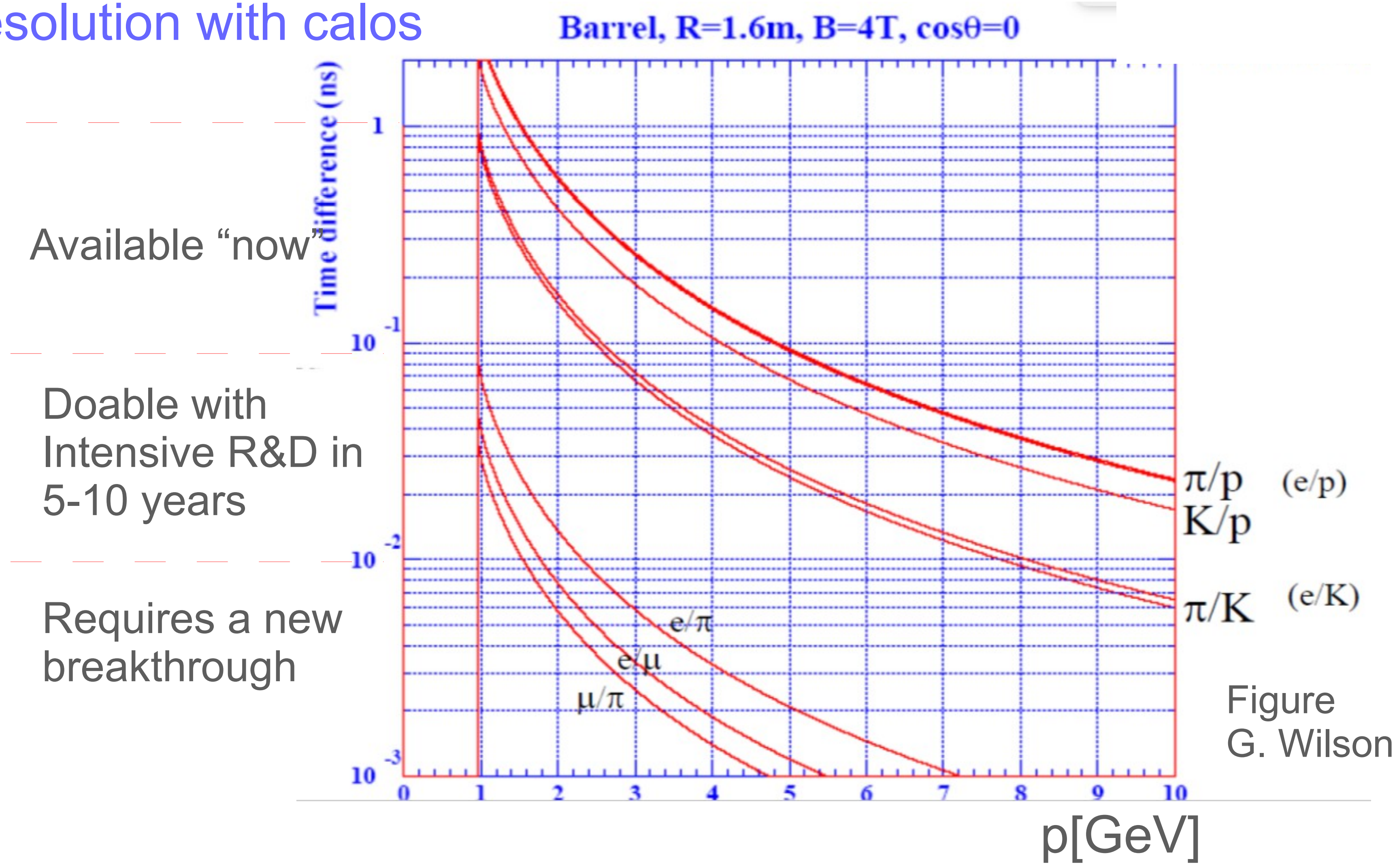


Figure G. Wilson

- Particle momenta (at 250 GeV) have peak below 10 GeV but long tail to higher energies
- Realistically ToF measurements will be (in foreseeable future) limited to particles below 10 GeV
  - Note that, apart from power consumption, in a final experiment one needs to control full system
- Momenta above 10 GeV require a real breakthrough and maybe even radically new approaches
  - Mandatory if ToF should work at and well above 250 GeV i.e. at Linear Collider energies

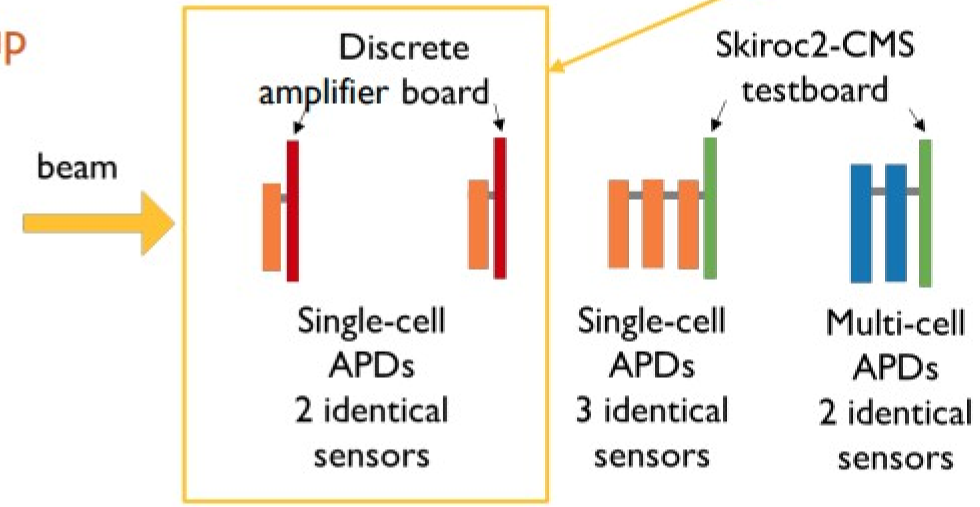
Timing devices – Hardware Studies

T. Suehara
CALICE Meeting, Valencia

6-8 Oct. 2021 at ELPH, Tohoku University

- 3 days ✕ 12 hours positron beam: ~770 MeV

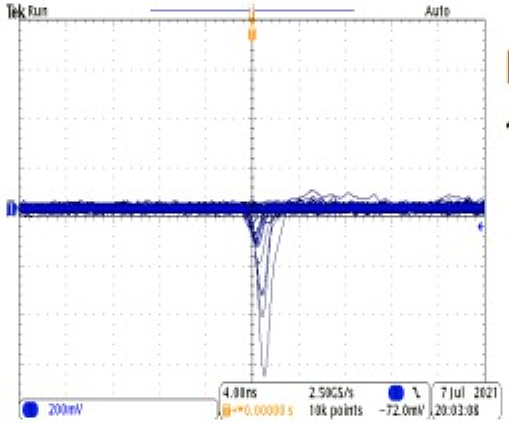
Setup



amplifier board

2 stages

Waveform output from the amp. board



Rising time ~1 nsec

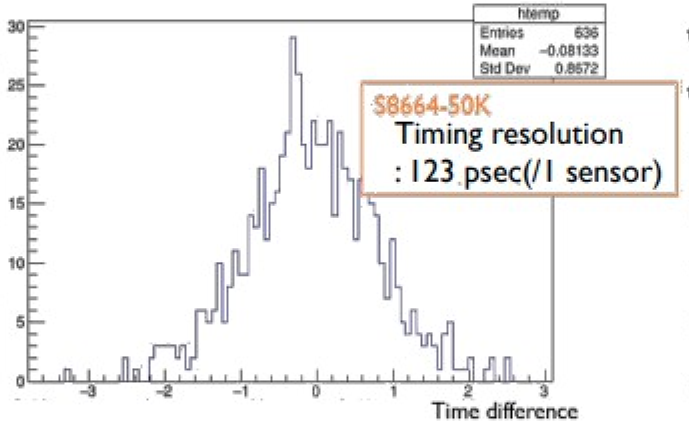
Amplifier chip

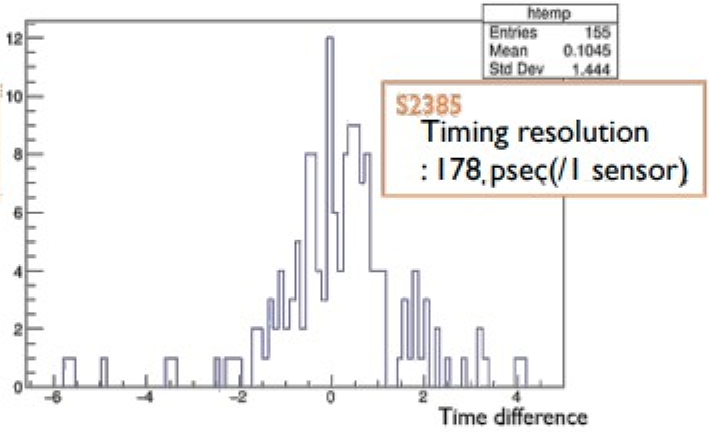
- GALI-S66+ (Mini-circuit)
- Gain: 20 dB
- Wide bandwidth 3GHz

APD

APD sensor	Cut of charge	Timing resolution
S8664-50K (Inverse type)	> 18 fC	123 ps
	> 36 fC	63 ps
S2385 (reach through type)	> 18 fC	178 ps
	> 36 fC	89 ps

Time difference between the two APDs (charge > 18 fC)





- Timing resolution of S8664-50K is better

→ Difference in capacitance related to signal rising time (S8664-50K: 55 pF S2385: 95 pF)

Final considerations: Powering needs for different running schemes

Power pulsed systems

Numbers from Vincent

All faults are mine

ILC "Standard"

T_{Bunch} ~ 1ms
f_{rep} ~ 5Hz
=> ΔT_{Bunch}=200ms

HL-ILC:

- $\mathscr{L} \times 4\,(6)$
- $N_{bunches} \times 2$: $\tau_{Train:}\ 1 \rightarrow 2$ ms
- $f_{rep}\ \times 2\,(3)$: $5 \rightarrow 15$ Hz

=> $\Delta T_{Bunch,min}$=66ms

HL-CLIC:

- $\mathscr{L} \times 2$
- $N_{bunches} \rightarrow$: $\tau_{Train:}$ 176 ns
- $f_{rep}\ \times 2$: $50 \rightarrow 100$ Hz

=> $\Delta T_{Bunch,min}$~10ms

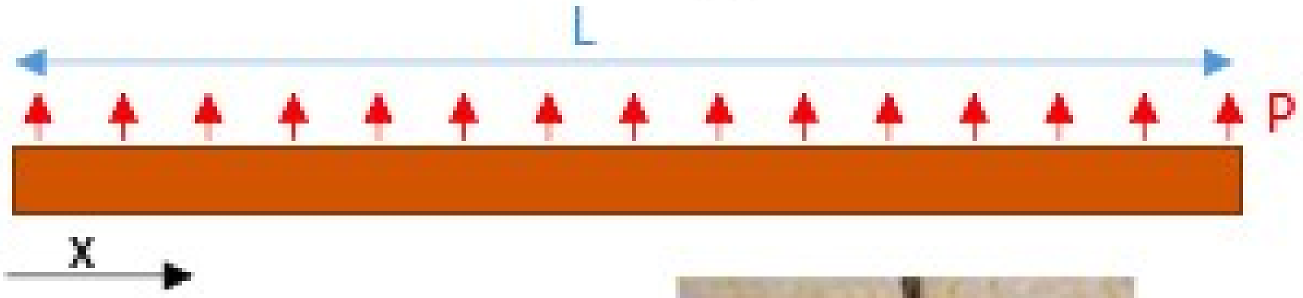
- In the (local) powering scheme the power is reloaded between the bunch trains with a small constant charging current
- As long as one manages to charge the capacitances between the bunch trains, the overall power consumption will not increase with increasing luminosity
  - The step from ILC Standard to HL-ILC doesn't look too big, CLIC may require a further look
  - Of course, the front-end electronics will still dissipate heat, passive cooling should still work

Continuously powered systems:

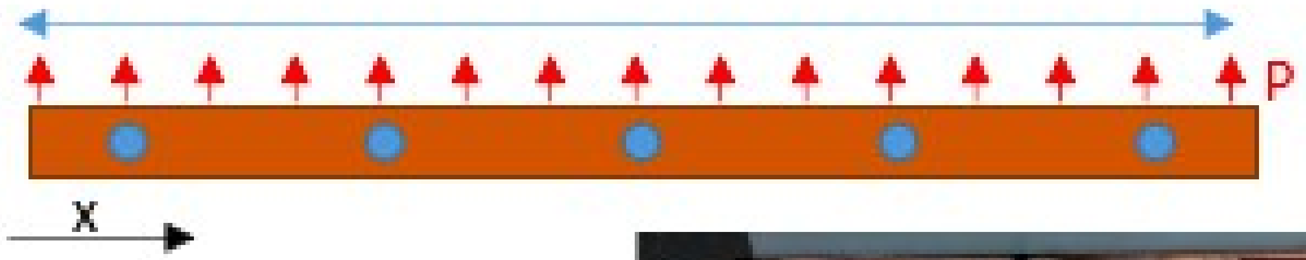
- Typical consumption of FEE (as of today) 5-10mW/channel
  - CMS HGCROC has 20mW/channel due to sophisticated digital part
- This translates directly into power consumption of detector
- 5mW: For 10^8 channels this leads to 500 kW power consumption of full detector
  - This is the pure consumption of the front-end electronics (e.g. no ohmic losses in power transfer etc. U=RI and I would be high)
  - => Active cooling

Active cooling?

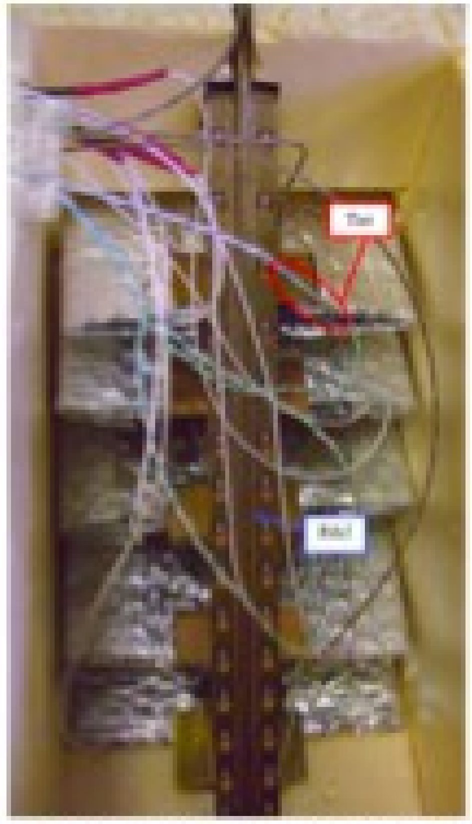
Passive cooling



Active cooling




Passive cooling ramp example


Passive cooling ramp set up test


Active cooling set up test with water at room temperature


Active cooling test layout (400mm x 300mm x 3mm thick copper plate with 1,800 pipes embedded)

Next generation ASICS?

Ch. de la Taille
CALICE Meeting, Valencia

- Dynamic gain preamp or TOT ?
- 200 ns shaping, 10 MHz ADC, several samples on the waveform
- Timing capability ? Auto-trigger and zero suppression
- Target ~1 mW power/ch and possible power pulsing
- I^2C slow control ? New readout protocol ?
- Include 2.5V LDO inside VFE ?
- Compatible with FCC LAr. SiPM/RPC tbd

	experiment	Sensor	capacitance	shaping	power	data	techno	Vdd	slow control
→ **SKIROC2**	CALICE	Si	30 pF	300 ns	5 mW/ch	5 MHz	SiGe 350n	3.3 V	SPI
HGCROC	CMS	Si	50 pF	20 ns	20 mW/ch	1.2 Gb/s	TSMC 130n	1.2 V	I^2C
FCC	LAR	Lar	50-200 pF	200 ns	<1 mW	Gb/s	TSMC 130n	1.2 V	I^2C
→ **SKIROC3**	CALICE	Si	50 pF	200 ns	<1 mW	Mb/S	TSMC 130n	1.2 V	?

CdLT CALICE meeting 20 apr 2022

(Non exhaustive) “To do list” (for LC Detector)

	Today	LC Detector
#cells*	15360	10^8
Sensor surface/m^2	0.5	2000-2500
Sensor type	9x9cm^2 based on 6” wafers	Size ? Based on 8” wafers?
Real size slabs	1 “electrical” long layer	~10000 detector slabs (5000 double layers)
Front end ASICs	SKIROC2, ns timing	SKIROC3, ps timing? Need 1.2-1.5M
Digital electronics	SL-Boardv2 (already quite close)	New versions,need 9k
DAQ	Highly performant system for prototype	Scaling to full detector
PCB	FEV2.x (already quite close)	Integration of new FE electronics, need ~75k
Slow control	Integrated in SL Board	Solution for full detector?
Mechanical Structures	1 barrel alveaola structure (EUDET 2010)	40 barrel modules + **endcaps**
Carrier Boards	Simple carbon plates	“H Boards” with wrapped W (Studies date back to 2010-2016)
Cooling	Advanced studies (AIDA-2020)	Full detector integration Continous powering woulf be anew world
Engineering (electrical and mechanics)	Advanced studies (for ILD IDR)	Require full revision and consolidation
Software	**Few** skillful people	Needs consolidation and person power

- A lot has been achieved
  - ... but the way is still long, as of today the team is too small and the funding is very (too) volatile
  - We are good in engineering but too few (young) physicists

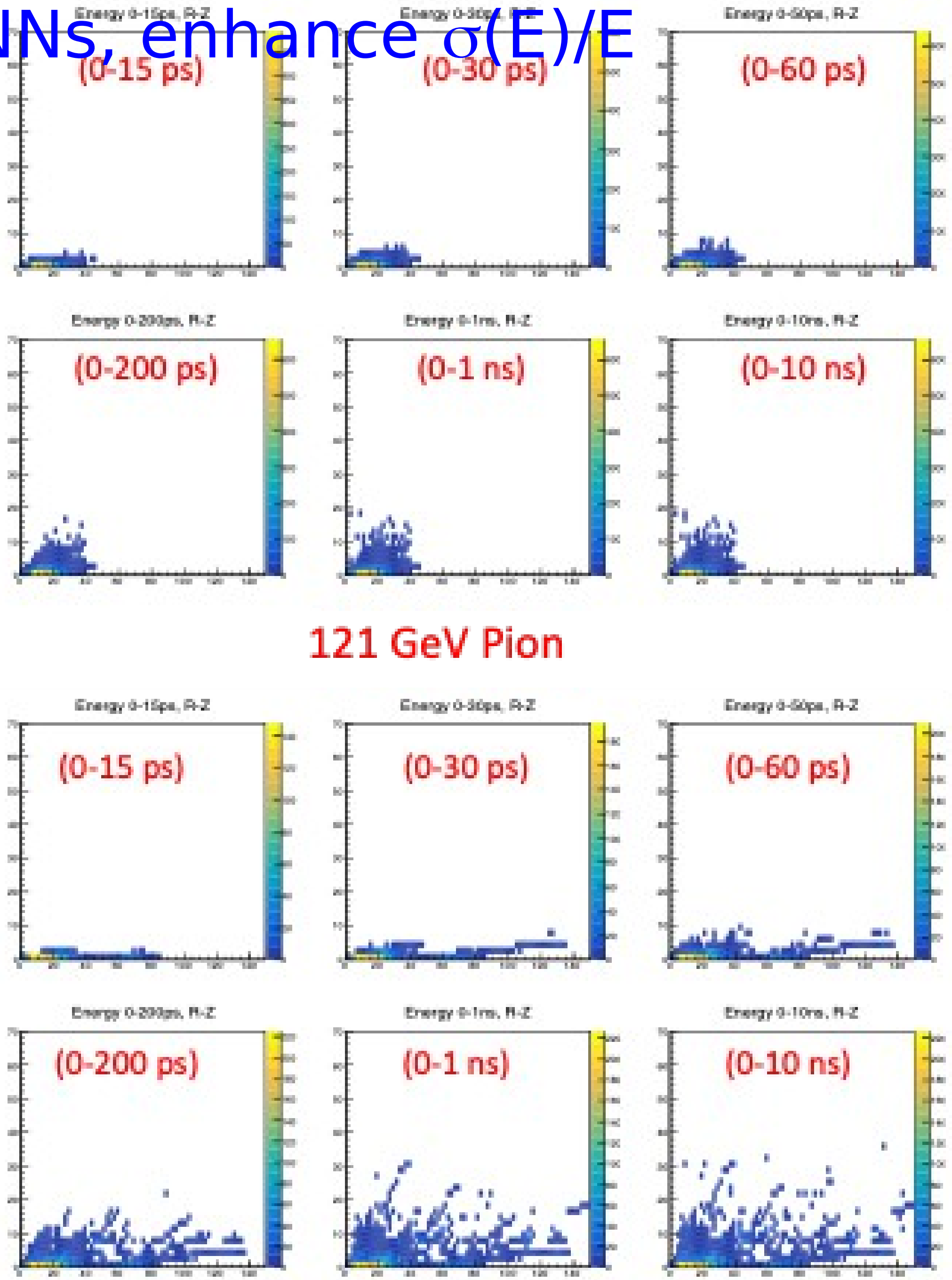
Summary and outlook

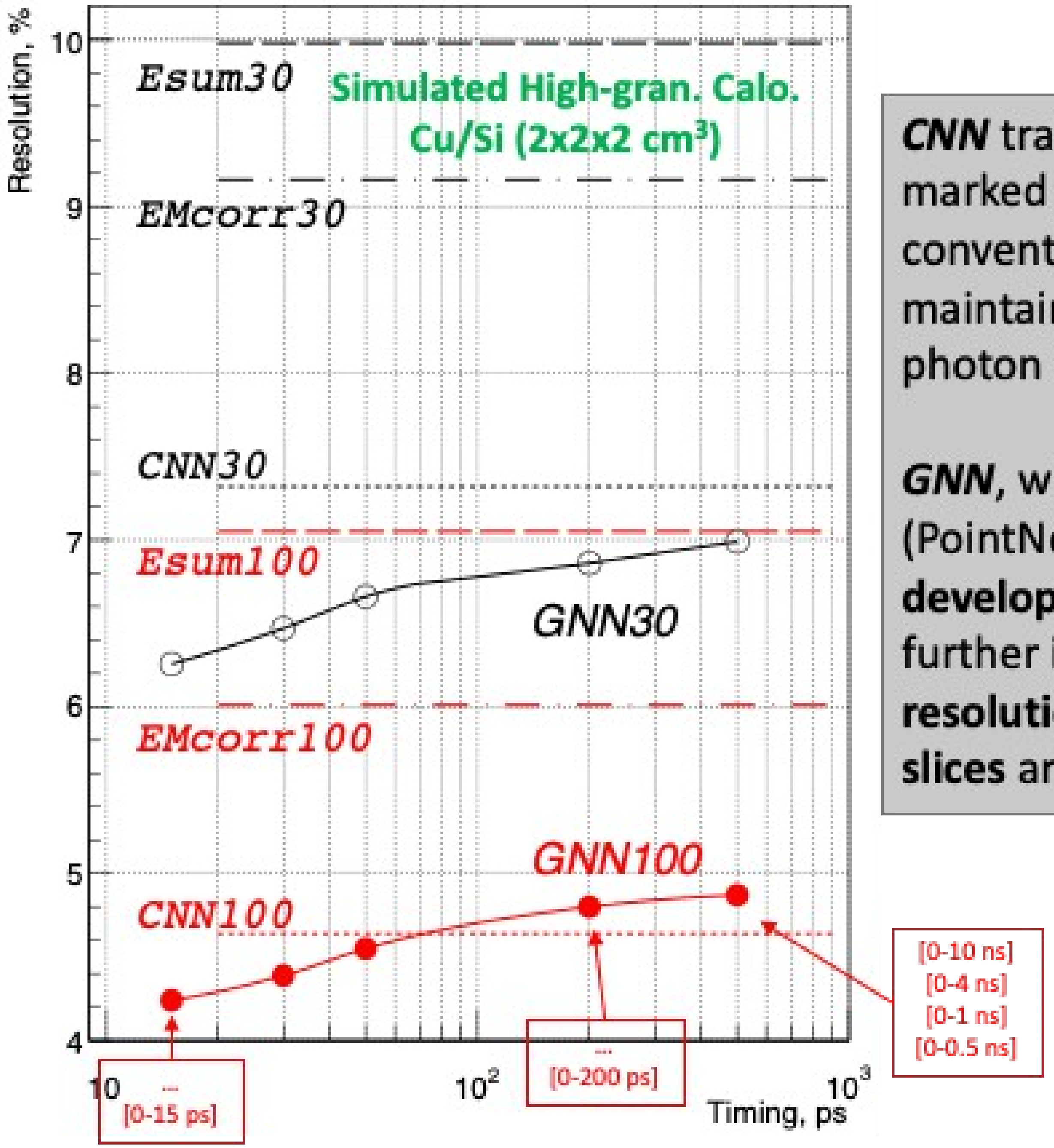
- R&D for SiW ECAL is in full swing
  - Two testbeams with prototypes
    - Important system tests
  - Strong and weak spots detected
  - The team is very (too) small, many fields uncovered, planning is difficult up to impossible since resources are a lottery
  - It's not in the "Kingdom of the Blind the One-Eye is King"
- ILD already benefits from a number of engineering studies
  - Require revision and consolidation
- Next step is consistent implementation of power pulsing
  - Power pulsing is power economic solution for detector operation (that can cope with luminosity upgrades of ILC)
  - Total consumption of 5 kW (less than three water boilers) of total ILD SiECAL seems to be in reach
- Continous powering would imply a major change
  - ... and the detector will be unavoidably much more power hungry
- What do we want from timing?
  - Requires consistent study
  - Would come at a price (higher power consumption)
- **Still a long way to go (just compare numbers on previous page)**
  - Detector construction requires an exponential increase in funding (money and manpower)

Backup

Timing in calorimeters

Features that emerge in the time domain can help distinguish particle types and, with GNNs, enhance $\sigma(E)/E$





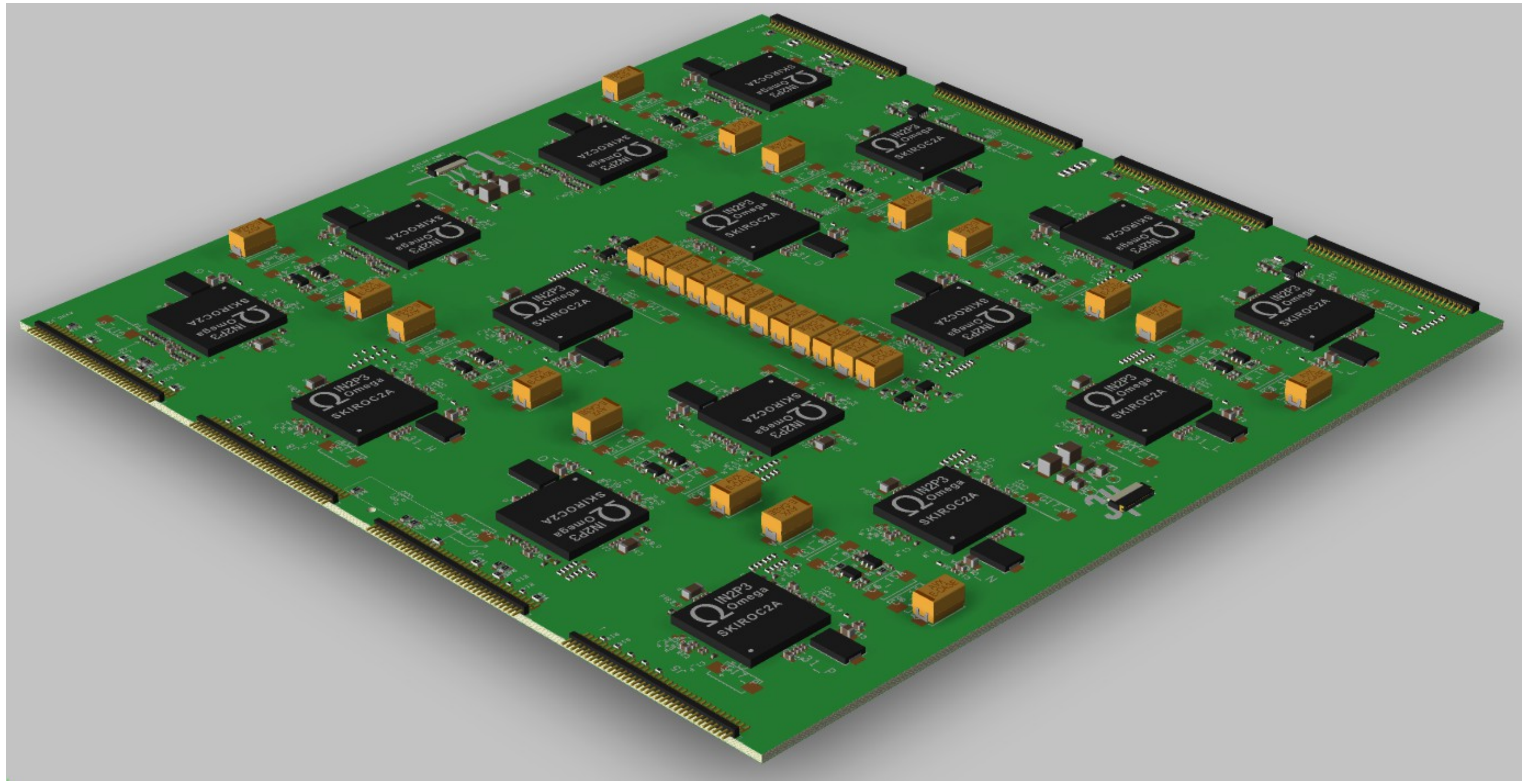
CNN trained on pions achieves marked improvement over the conventional approache while maintaining performance for photon reconstruction

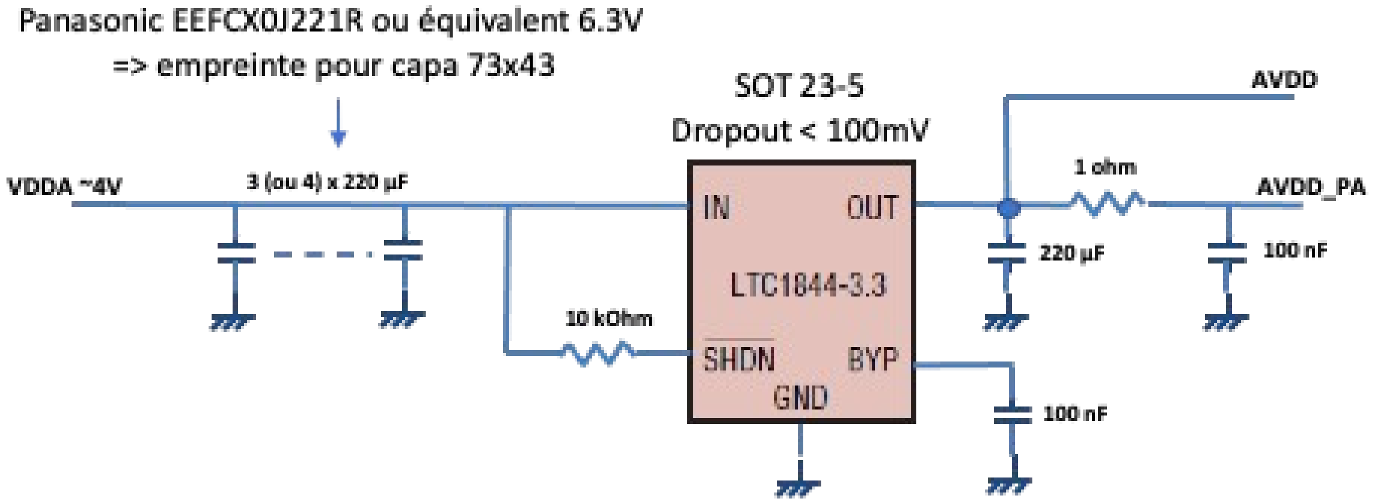
GNN, with edge convolution (PointNet), **with shower development timing information** further **improves energy resolution** when **shorter time slices** are included

arxiv:2108.10963

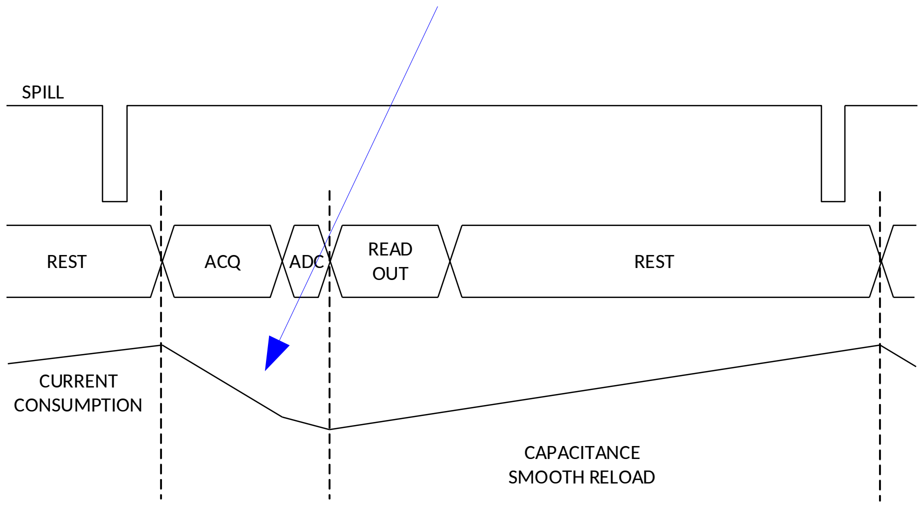
New FEV2.0 et al.

Status after regular discussions between engineers of LLR, IJCLab, LPNHE and OMEGA





With 600 µF, we ensure 100mA during 3ms with a voltage drop of 0.5V (ΔV = I.t/C).



- New board for next step of technical realisation of power pulsed Ecal layers
  - Capacitances and LDO close to ASICs
- Last month progress in design
  - Stacking of PCB
  - Choice of components
- Another important feature is that HV will be transported via connectors (i.e. On top of board
  - Wafer supply from bottom of board via plies (copper/kapton)
  - These plies are a delicate piece
  - Risk of shortcuts and wafer damage (the design of the kapton that goes below the board requires another design round)
- Expect production either shortly before or shortly after the summer break (not in a hurry, carefulness comes before speed)
- The setup will be completed by a “Termination card” that will allow for flexible chaining of cards (i.e. No soldering of terminations)
- and for flexible adding of decoupling capacitances (to study noise behaviour of COBs)