Developments and Trends in Silicon Pixel Detectors
Potentially Improving the ILD Concept Performances

M.Winter / 17 May 2022

CONTENTS:

- **How to make ILD benefit from advances & perspectives in SC detectors**
  - Hierarchy among the requirements (when antagonistic)
  - Which frameworks are anticipated to be most appropriate to ILD
- **Pixel sensors:**
  - R&D on granular, thin and low power sensors $\Rrightarrow$ CMOS sensors (65 nm, 180 nm)
  - R&D on very fast and radiation tolerant sensors $\Rrightarrow$ LGAD and similar
- **Services and detector concept:**
  - ALICE-ITS3: attractive aspects of its R&D programme and perpsectives (ALICE 3)
  - large surface, thin and bent CMOS pixel sensors
- **Summary & Outlook**

ECFA Detector R&D Roadmap for SC Devices

"Technical" Start Date of Facility (This means, where the dates are not known, the earliest technically feasible start date is indicated - such that detector R&D readiness is not the delaying factor)				< 2030					2030-2035					2035 - 2040	2040-2045		> 2045		
				Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3 [1]	ALICE 3	LHCb (≥LS4)[1]	ATLAS/CMS (≥ LS4)[1]	EIC	LHeC	ILC[2]	FCC-ee	CLIC[2]	FCC-hh	FCC-eh	Muon Collider
Vertex Detector[3]	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (μm)		$\simeq 5$		$\lesssim 5$	$\simeq 3$	$\lesssim 3$	$\lesssim 10$	$\lesssim 15$	$\lesssim 3$	$\simeq 5$	$\lesssim 3$	$\lesssim 3$	$\lesssim 3$	$\simeq 7$	$\simeq 5$	$\lesssim 5$
			X/X_0 (%/layer)	$\lesssim 0.1$	$\simeq 0.5$	$\simeq 0.5$	$\lesssim 0.1$	$\simeq 0.05$	$\simeq 0.05$	$\simeq 1$		$\simeq 0.05$	$\lesssim 0.1$	$\simeq 0.05$	$\simeq 0.05$	$\lesssim 0.2$	$\simeq 1$	$\lesssim 0.1$	$\lesssim 0.2$
			Power (mW/cm²)		$\simeq 60$			$\simeq 20$	$\simeq 20$			$\simeq 20$		$\simeq 20$	$\simeq 20$	$\simeq 50$			
			Rates (GHz/cm²)		$\simeq 0.1$	$\simeq 1$	$\lesssim 0.1$		$\lesssim 0.1$	$\simeq 6$		$\lesssim 0.1$	$\simeq 0.1$	$\simeq 0.05$	$\simeq 0.05$	$\simeq 5$	$\simeq 30$	$\simeq 0.1$	
			Wafers area (")[4]					12	12			12			12		12		12
		DRDT 3.2	Timing precision σ_t (ns)[5]	10		$\lesssim 0.05$	100		25	$\lesssim 0.05$	$\lesssim 0.05$	25	25	500	25	$\simeq 5$	$\lesssim 0.02$	25	$\lesssim 0.02$
		DRDT3.3	Radiation tolerance NIEL (x 10^{16} neq/cm²)							$\simeq 6$	$\simeq 2$						$\simeq 10^2$		
			Radiation tolerance TID (Grad)							$\simeq 1$	$\simeq 0.5$						$\simeq 30$		
Tracker[6]	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (μm)						$\simeq 6$	$\simeq 5$		$\simeq 6$	$\simeq 6$	$\simeq 6$	$\simeq 6$	$\simeq 7$	= 10	$\simeq 6$	
			X/X_0 (%/layer)						$\simeq 1$	$\simeq 1$		$\simeq 1$	$\simeq 1$	$\simeq 1$	$\simeq 1$	$\simeq 1$	$\lesssim 2$	$\simeq 1$	
			Power (mW/cm²)						$\lesssim 100$	$\simeq 100$		$\lesssim 100$		$\lesssim 100$	$\lesssim 100$	$\lesssim 150$			
			Rates (GHz/cm²)							$\simeq 0.16$									
			Wafers area (")[4]						12			12		12	12	12	12		12
		DRDT 3.2	Timing precision σ_t (ns)[5]						25	$\lesssim 25$		25	25	$\lesssim 0.1$	$\lesssim 0.1$	$\lesssim 0.1$	$\lesssim 0.02$	25	$\lesssim 0.02$
		DRDT3.3	Radiation tolerance NIEL (x 10^{16} neq/cm²)							$\simeq 0.3$							$\lesssim 1$		
			Radiation tolerance TID (Grad)							$\simeq 0.25$							$\lesssim 1$		
Calorimeter[7]	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.2	Timing precision σ_t (ns)[5]											$\lesssim 0.05$	$\lesssim 0.05$	$\lesssim 0.05$	$\lesssim 0.02$		$\lesssim 0.02$
		DRDT 3.3	Radiation tolerance NIEL (x 10^{16} neq/cm²)														$\gtrsim 10^2$		
			Radiation tolerance TID (Grad)														$\simeq 50$		
Time of Flight[8]	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.2	Timing precision σ_t (ns)[5]				$\simeq 0.02$		$\simeq 0.02$		$\lesssim 0.03$	$\simeq 0.02$	$\simeq 0.02$		$\lesssim 0.01$		$\lesssim 0.01$	$\simeq 0.02$	
		DRDT 3.3	Radiation tolerance NIEL (x 10^{16} neq/cm²)														$\simeq 10^2$		
			Radiation tolerance TID (Grad)														$\simeq 30$		

Tracking Devices: Pixel Sensors (1/3)

- **Why are semi-conductor detectors attractive ?**
  - ⋇ they can be very precise: 0(1) μm
  - ⋇ they can be very fast: O(10) ps
- **However:**
  - ⋇ they cannot be simultaneously very precise and very fast
  - ⋇ power consumption of very fast sensors tends to be very high ($\gtrsim$ 1-10 W/cm^2)
  - ⋇ need of hierarchy among requirements driven by physics and those imposed by running conditions
  - ⋇ priorities are different for HL-LHC, CLIC, FCCee (CEPC ?), ILC due to different running conditions

    $\Rrightarrow$ Sensor R&D goals are different
- **They can be very thin:**
  - ⋇ very low material budget: $\lesssim$ 50 μm (0.05% X$_0$ / hit) $\simeq$ twice larger average material/TPC hit

    IF one neglects the material budget of SC sub-system services !
  - ⋇ possibility to bent and shape like ”roman tiles”

    $\Rrightarrow$ minimise impact of overlap between neighbouring modules and of mechanical support

Tracking Devices: Pixel Sensors (2/3)

- **Single point resolution:** σ_{sp}
  - $\sigma_{sp} \simeq$ few μm achievable, with some overhead below $\sim$ 5 μm
  - $\sigma_{sp} \lesssim$ 5 μm x 5 μm (typically $\lesssim$ 25-30 μm pitch), tends to limit in-pixel circuitry (VFE data processing)

    $\Rightarrow$ time resolution and hit rate handling capacity impacted
  - Alternative approaches for σ_{sp}:
    - small pixels with binary charge encoding ($\equiv$ discri. threshold YES/NO)
    - larger pixels with VFE charge determination μ-circuitry (TOT, ADC)

- **Time stamping:** Δ_t
  - $\Delta_t \lesssim$ 100 ps achievable with complex VFE circuitry
  - Several drawbacks:
    - power consumption can be very high ($\gtrsim$ 1-10 W/cm^2)
    - in-pixel circuitry (TDC) requires sizeable (e.g. thick) pixels
    - possibly: dead time, fill factor $<$ 100 % (LGAD, SiPM)

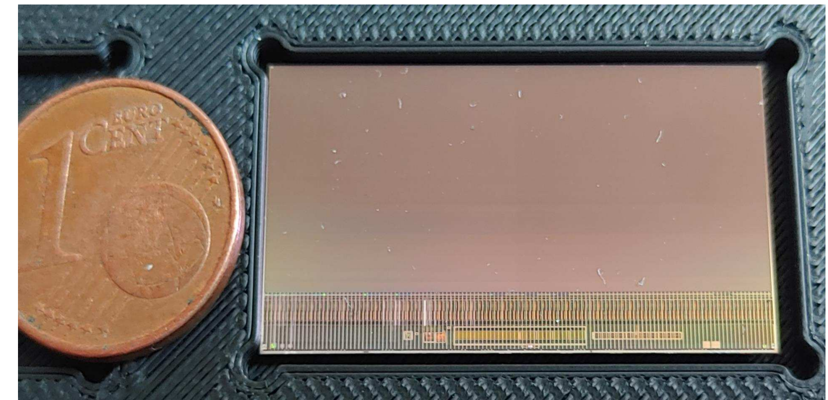
- **Two classes of Semi-Conducting pixel sensors (incl. strixels):**
  - privileging spatial resolution: CMOS pixel sensors, SoI sensors, FPCCD, DEPFET, ...

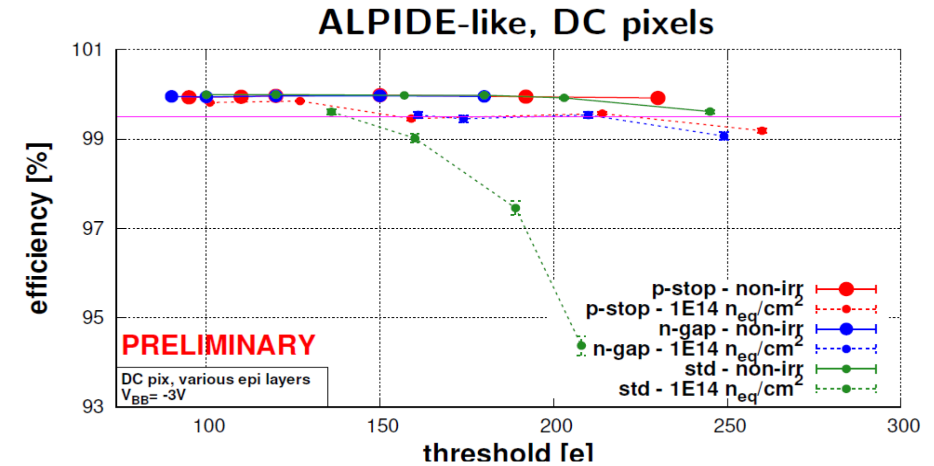
    AND aiming at improved time resolution (& sometimes radiation tolerance)
  - privileging time resolution & radiation hardness: LGAD, CMOS, SiGe, Hybrid, ...

    AND aiming at improved spatial resolution (smaller pixels) & power saving

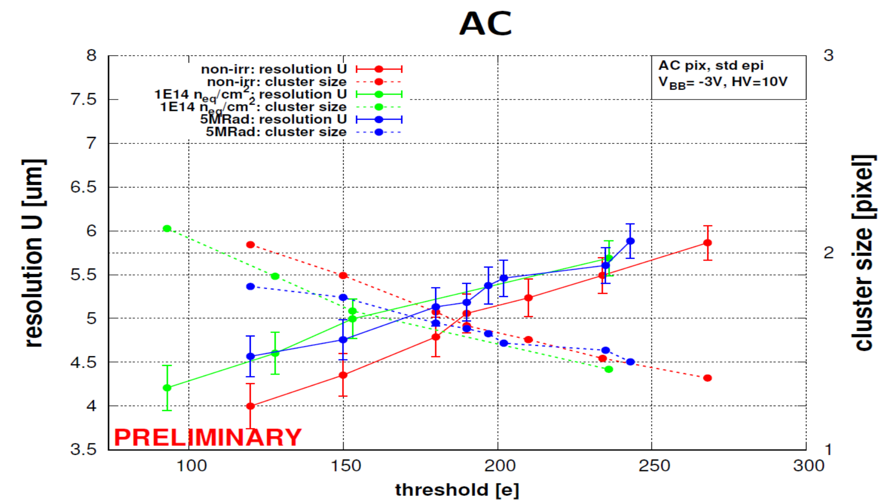
Example of Trade-Off: MIMOSIS

- **MIMOSIS Pixel Sensor (180 nm CMOS process):**
  - 1024x504 pixels (27x30 μm^2) covering 4.2 cm^2
  - VFE $\equiv$ ALPIDE, adapted to O(10^2) MHz/cm^2 hit density
  - introduction of AC-coupled pixels (sensing node bias)
  - 2 Gbits/s data transmission frequency
  - read-out in 5 μs with $\lesssim$ 70 mW/cm^2 power density
  - tested (2021-22) on beam at DESY & CERN-SPS





- **Extension to PSIRA:**
  - VFE μ-circuits of MIMOSIS allow for $\sim$ 0.5 μs r.o.
  - Anticipated power density $\sim$ 50–100 mW/cm^2
  - 50μm thick EPI instead of 25 μm $\Rrightarrow$ expect $\sigma_{sp} \simeq 4\ \mu m$
  - Proto. of 32x504 pixels will be submitted to foundry in June together with final full size MIMOSIS prototype



Tracking Devices: Pixel Sensors (3/3)

- **Capacity of pixel sensors to provide PID:**
  - ⋇ if thinned to a few tens of μm, they cannot provide PID based on dE/dX
  - ⋇ once pushed to their ultimate time resolution, they may provide TOF info allowing for PID, BUT:
    - PID is restricted to low momentum particles (few GeV/c)
    - fast sensors require complex circuitry $\Rrightarrow$ pixel dimensions $\Rrightarrow$ insufficient spatial resolution
    - sizeable power consumption $\Rrightarrow$ active cooling required $\Rrightarrow$ extra material budget
      & geometrical acceptance restriction due to services (cooling system, cable ducts)

- **Guidance for ILD accounting for recent progress in SC sensors:**
  - ⋇ SC sub-systems should complement tracking of TPC (essential for K/Pi separation)
  - ⋇ focus on spatial resolution and material budget (including power saving);
    timing is not a critical issue: O(500 ns) within reach with $<$ 100 mW/cm^2 (power pulsing ?)
  - ⋇ very fast sensors may be more valuable in end-caps (outside of TPC geom. acc.)
  - ⋇ if desired, introduce fast layers in minimal fraction of tracking sub-systems, typically in 2 layers:
    $\hookrightarrow$ outskirt of vertex detector and front of forward tracking and at large radius and end of forward tracking

Fast to Very Fast Pixel Devices

- Typical goals for speedy read-outs: event separation or PID

  1) Beam related constraints: HL-LHC pile-up interactions, CLIC BX separation,
  signal/beam BG separation, ... $\Rrightarrow$ O(0.1–1) ns

  2) PID based on TOF $\Rrightarrow$ $<$ 50 ps required

- Contemporary detectors in construction:

  ⋇ NA-62 Gigatracker: upgrade $\rightarrowtail$ 2023

  - hybrid pixels (300x300 μm^2) composing 3 stations of 6x3 cm^2 (0.5% X_0, μchannel cooling)
  - time stamping: 200 ps with 10 TDCpix r.o. chips for 18,000 pixels

  ⋇ CMS timing layer: End-gap disk of $\sim$ 4 m^2

  - time stamping goal: 30-50 ps/track based on LGAD pixels
  - End-cap Timing Layer (ETL): LGAD pixels (1.3x1.3 mm^2) with $\simeq$ 90% fill factor
  - 16x16 LGAD pads read out with one bump-bonded ETROC chip: 40 ps jitter, 1 W dissipation

- Where does fast timing serve ILD performances

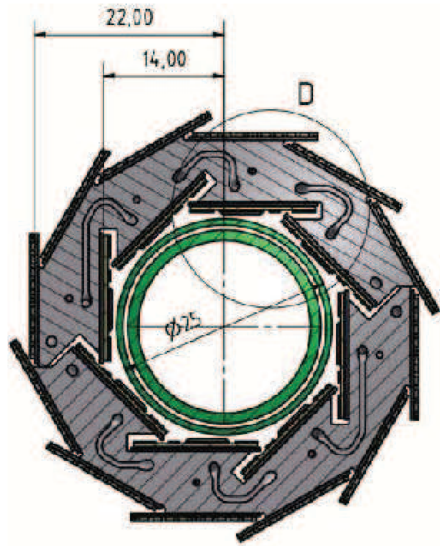
⋇ against beam BG overlap with physics final states: few 100 ns

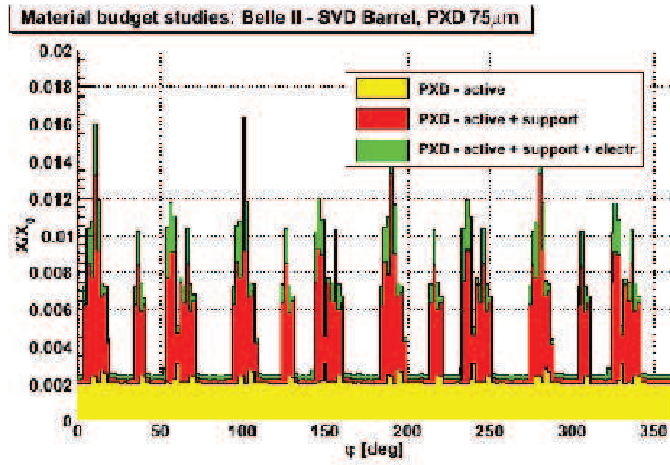
⋇ reduction of beam related back-scattered background: $<$ 20 ns

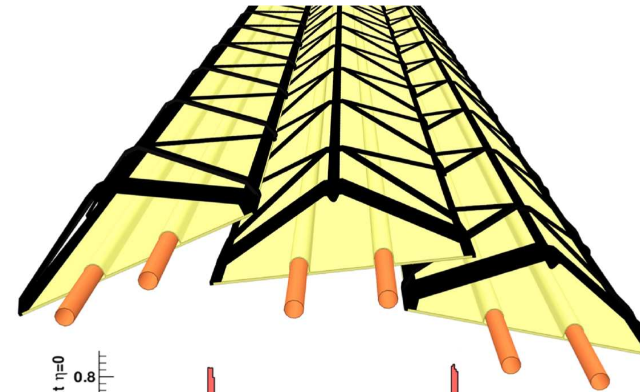
⋇ TOF (end-caps): few tens of ps !!!

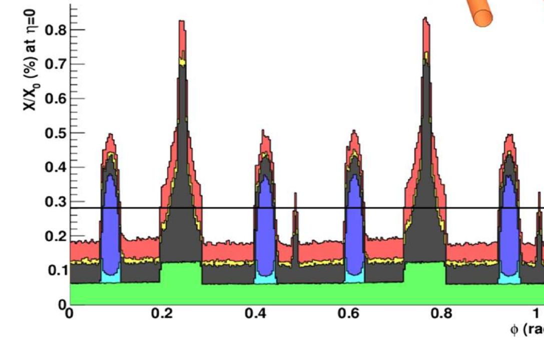
Tracking Devices: Material Budget

- Physics perfo. limited by material budget of **services & overlaps** of neighbouring modules/ladders







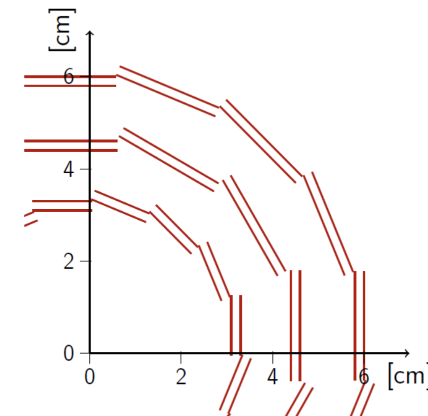


Flex Printed Circuit (22%)
Glue (5%)
Carbon Structure (33%)
Water(13%)
Cooling pipes wall (2%)
Pixel Chip (26%)
Mean X/X0 = 0.282%

BELLE-II PXD **ALICE-ITS**

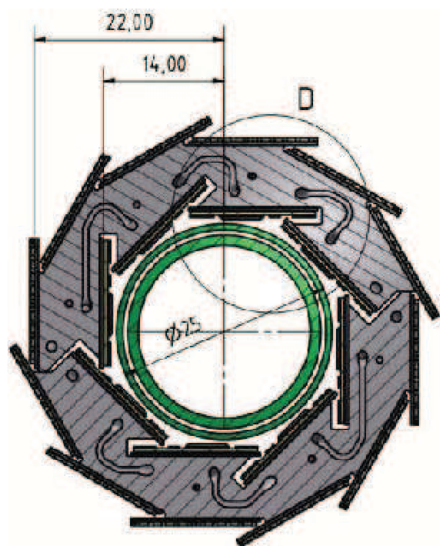
- Contribution of sensors to total material budget of vertex detector layer is modest: 15 - 30%

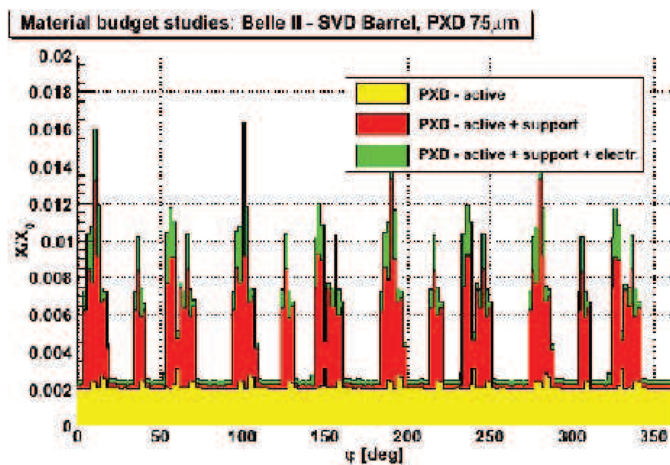
- **Additionnal complications:**
  - double-sided layers: OK for innermost layer ?
  - insensitive (side) part of ladders ⇛ overlapped ?
  - high magnetic field, etc.

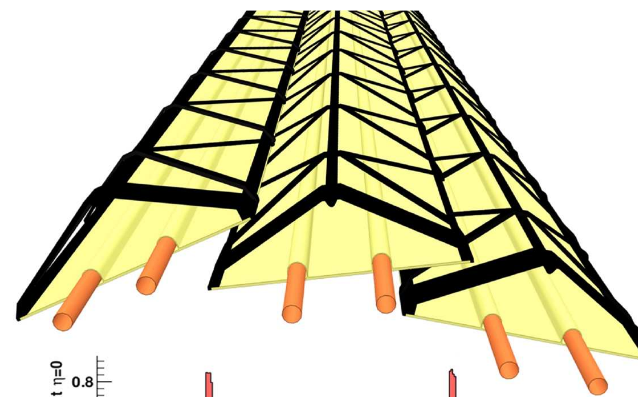


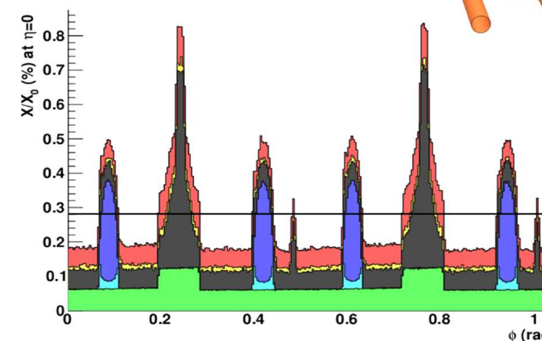
Major R&D Goal in Coming Years: Material Budget Reduction

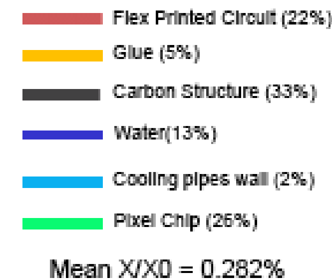
- Physics perfo. limited by material budget of **services & overlaps** of neighbouring modules/ladders





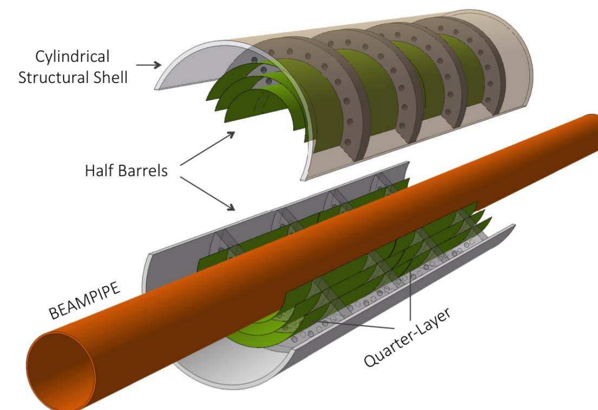






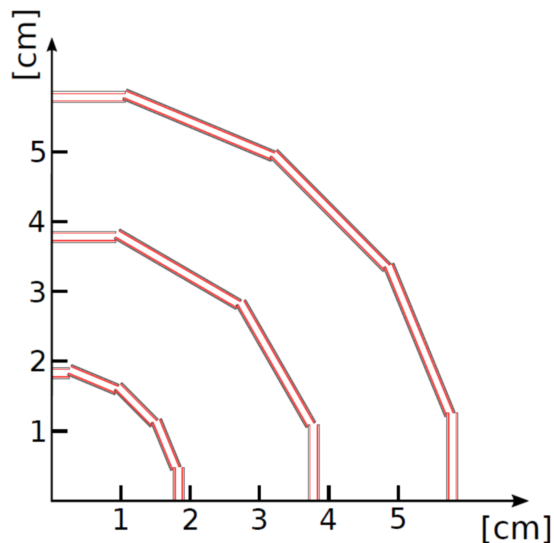
BELLE-II PXD **ALICE-ITS**

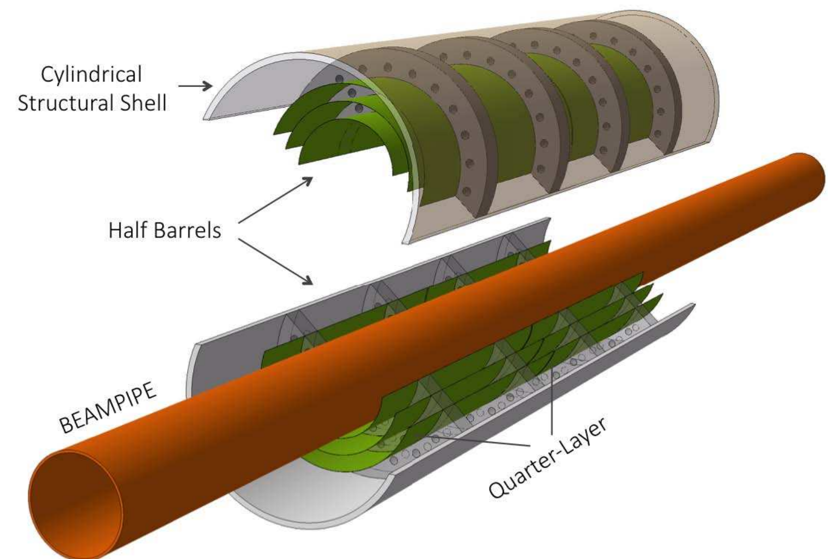
- Contribution of sensors to total material budget of vertex detector layer is modest: 15 - 30%
- **R&D objective beyond "classical" concepts:**
  - Innermost layer: try stitched & curved CPS along goals of ALICE-ITS3, possibly with 65 nm process
  - Concept with minimised mechanical support (e.g. using beam pipe) See Talk of M. Mager at Vertex-19, Lopud Island, Oct.'19



Aiming at Improved Physics Performances w.r.t. State-of-the-Art

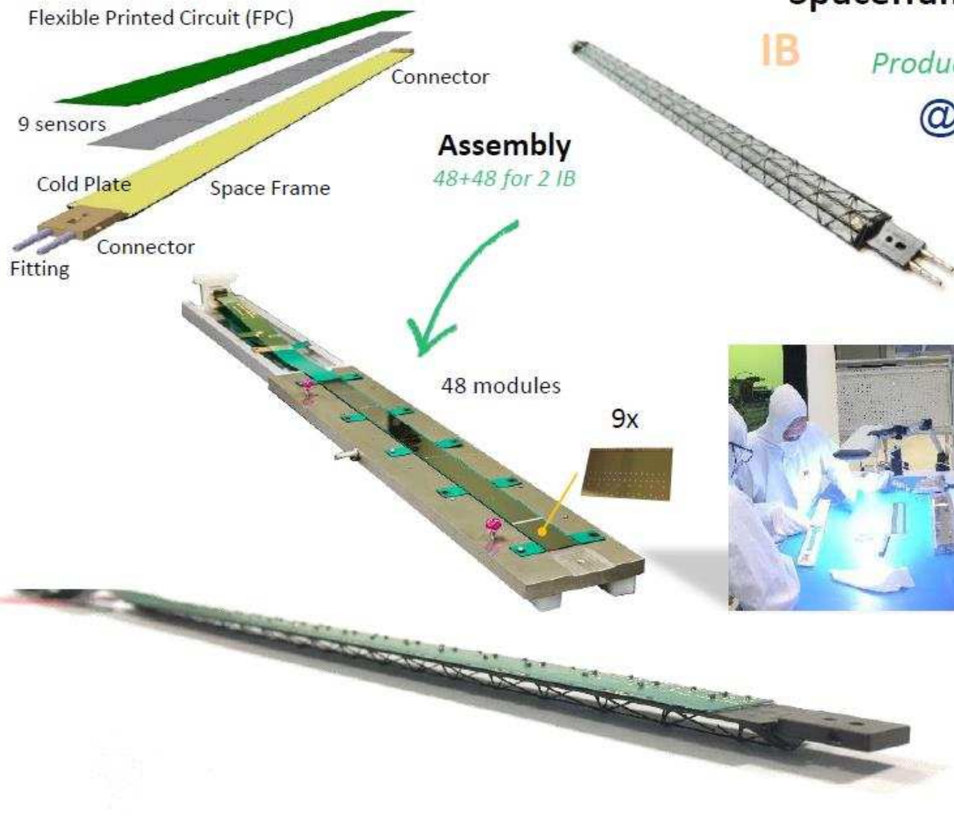
- Revisit globally usual vertex detector concepts in ordre to suppress its material budget
  and improve the spatial resolution toward the ambitionned 3 μm
- **Join R&D effort of ALICE-ITS3 project**, associated to W.P.-1.2 of CERN-EP R&D programme
  (despite some modest ambitioned performances: 5 μm and 10 μs)
- Unique occasion to develop stitched (curved) pixel sensors in a 65 nm technology (cost !)
  and a novel integration concept optimised for material budget suppression

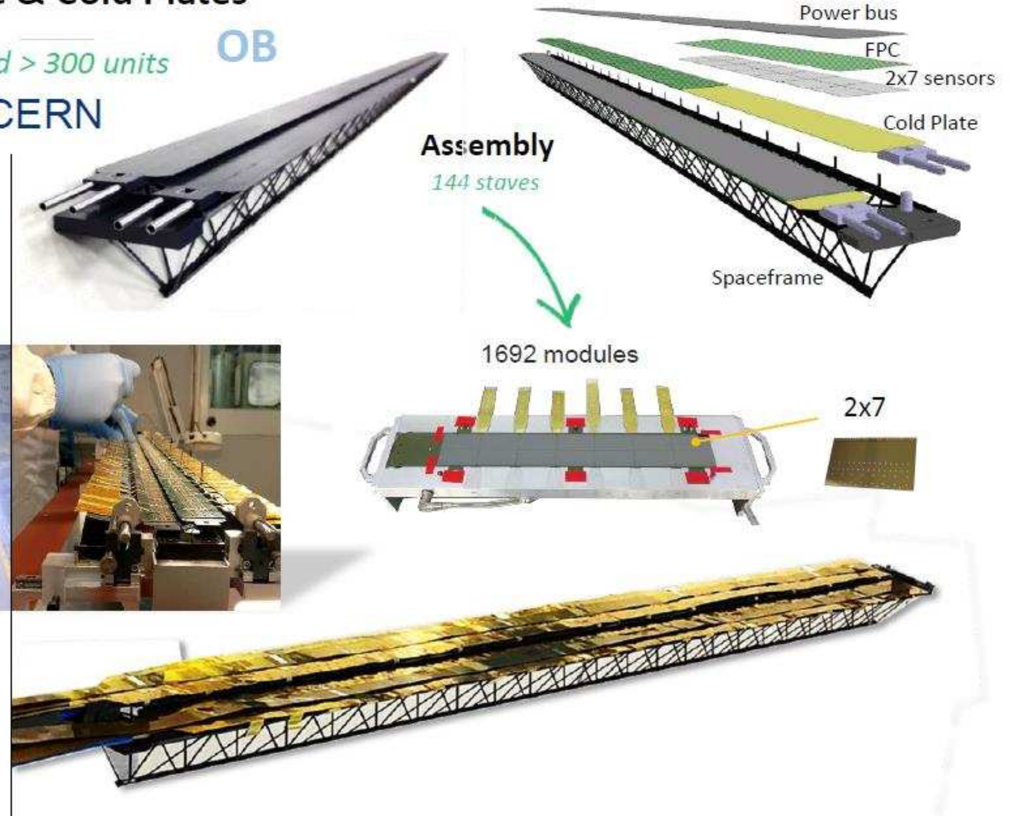




ALICE: ITS2

Forum on Tracking Detector Mechanics 2021





- → Chips are glued onto cold plates with embedded Kapton that provide leakless water cooling.
- → The cold plates are stiffened by a spaceframe that provides stiffness and position stability
- → To achieve the target precision all gluing stages are done in specially developed jigs

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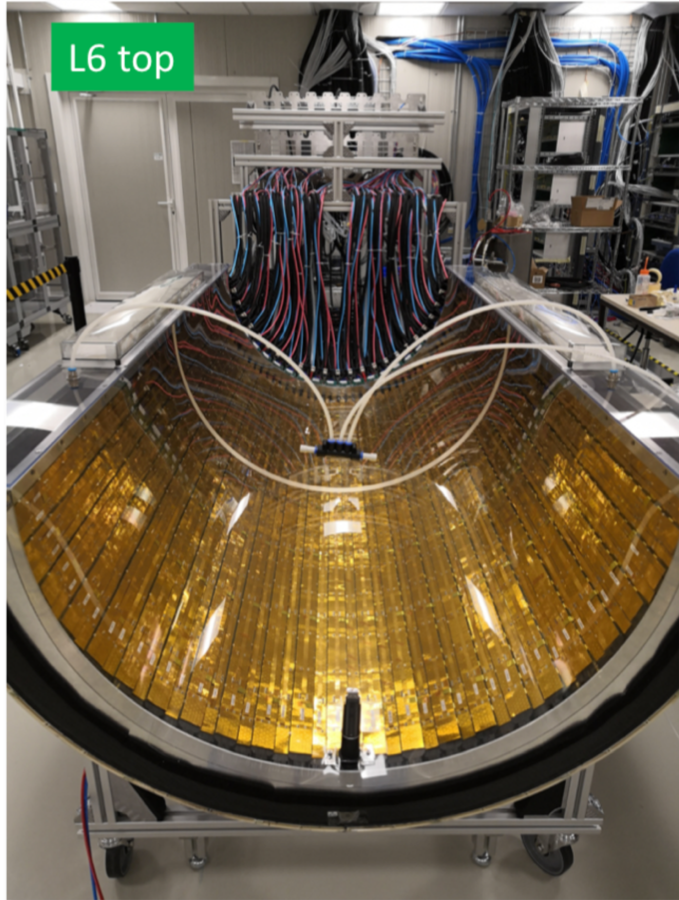
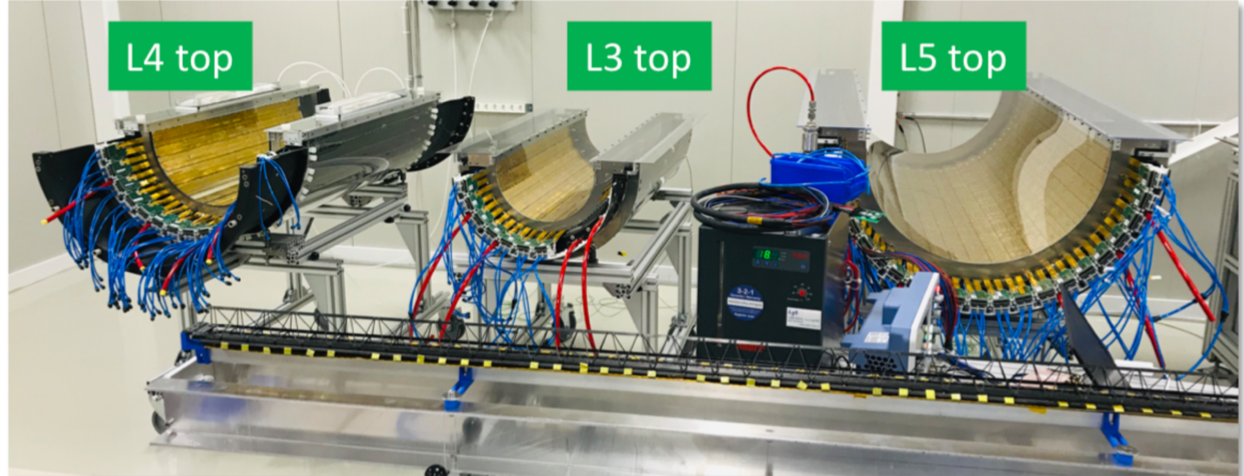
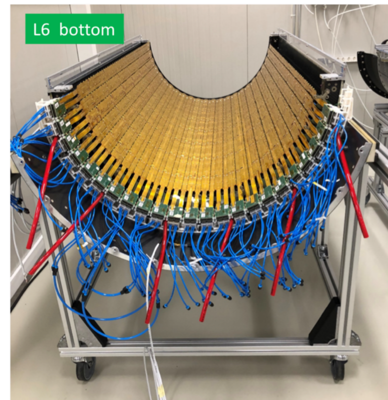
from C. Caruglio - 2021

WATCH THE CABLES ...

Outer Barrel Half Layers







ITS and its Supply and Readout Systems are **completed** at date

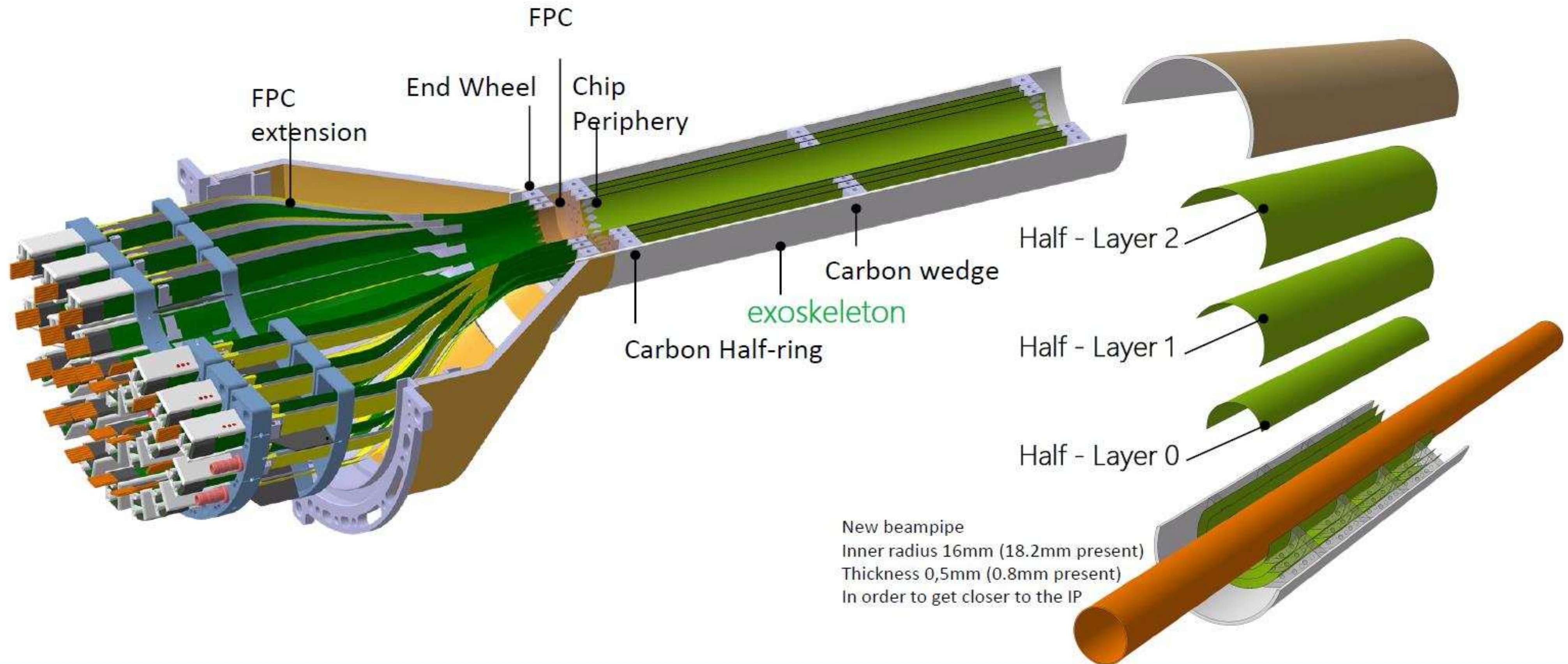
Undergoing **commissioning** (in the clean room)

Transfer to the cavern over June, July and August 2020

from G. Aglieri - 2020

ITS3 Layout

Forum on Tracking Detector Mechanics 2021



→ novel vertex detector consisting of curved wafer-scale ultra-thin silicon sensors arranged in perfectly cylindrical layers, featuring an unprecedented low material budget per layer, with the innermost layer positioned at only 18 mm radial distance from the interaction point

from C. Caruglio - 2021

ITS3 CARBON FOAM

Forum [illegible]ng Detector Mechanics 2021

R&D

Liquid Cooling

Graphite foam used as conductive media between Titanium pipe and sensor

Air Flow

Graphite foam used as heat radiators in Gas cooling solution

wedge (structural)

half-ring (thermal)

Periphery (where most of the heat is dissipated

Convective heat transfer enhancement allowing air to flow across the foam bonded to the chip sensor

Low density

ERG DUOCEL_AR

0.06 kg/dm^3

0.033 W/m·K

Used as support (wedge)

~710 cm X0

High thermal conduction

ALLCOMP_HD

0.45-0.68 kg/dm^3

85-170 W/m·K

Used as heat radiator (half-ring)

Several carbon foam have been considered, here shown foams at the extremes (lighter/ better thermal conductivity)

→ **R&D in HEP Carbon foam used as radiator in detector GAS cooling applications.**
Best compromise between thermal properties and low density. Radiator geometries optimisation to reduce pressure drop

→ **In Industry Carbon Lighter foams available from Aerospace.**

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NEXT First step toward working large sensor: Super-ALPIDE

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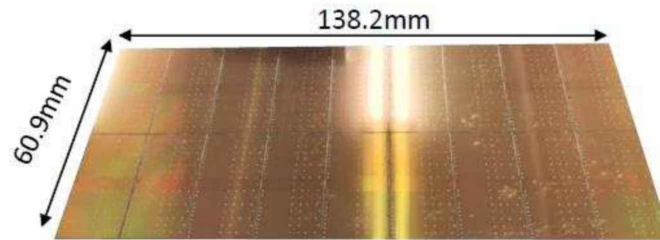
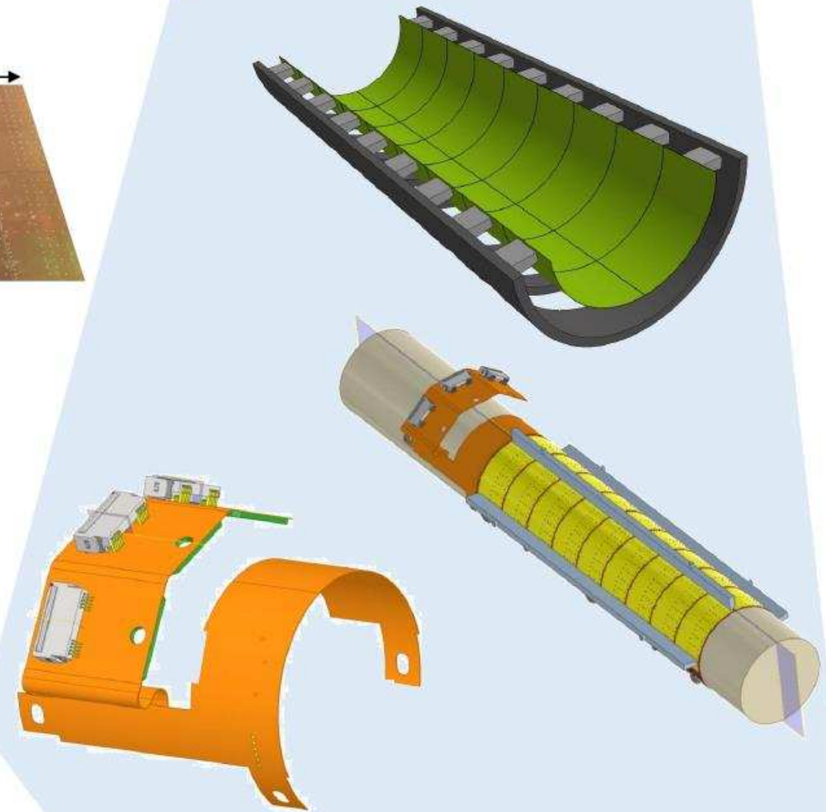
FPC (temporary approach)



Super-ALPIDE
Non stitched, it will require an FPC that will envelope the sensor and will be connected through wire bonds



CAD scheme with super-ALPIDE chip

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→ **R&D in HEP Material reduction in front of sensors will be pursued by investigating new sensors technologies and air cooling.**

from C. Caruglio - 2021

CURVED SENSOR DEVELOPMENT BASED ON ASSEMBLY OF ALPIDE SENSORS

A Large Ion Collider Experiment

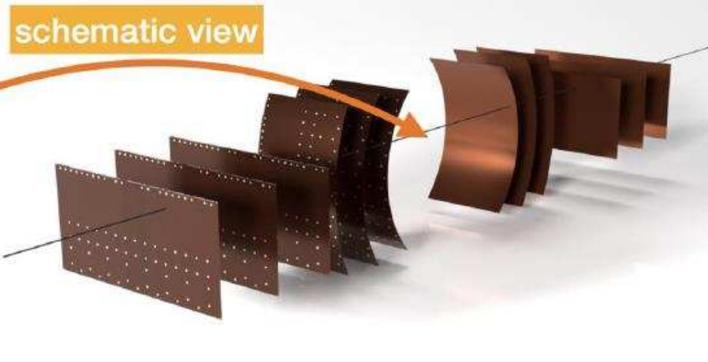
Super-ALPIDE mockup assembly - V2
Wire-bonding through exoskeleton

from ALICE-ITS3 - internal $\Rrightarrow$ **NOT TO COPY**

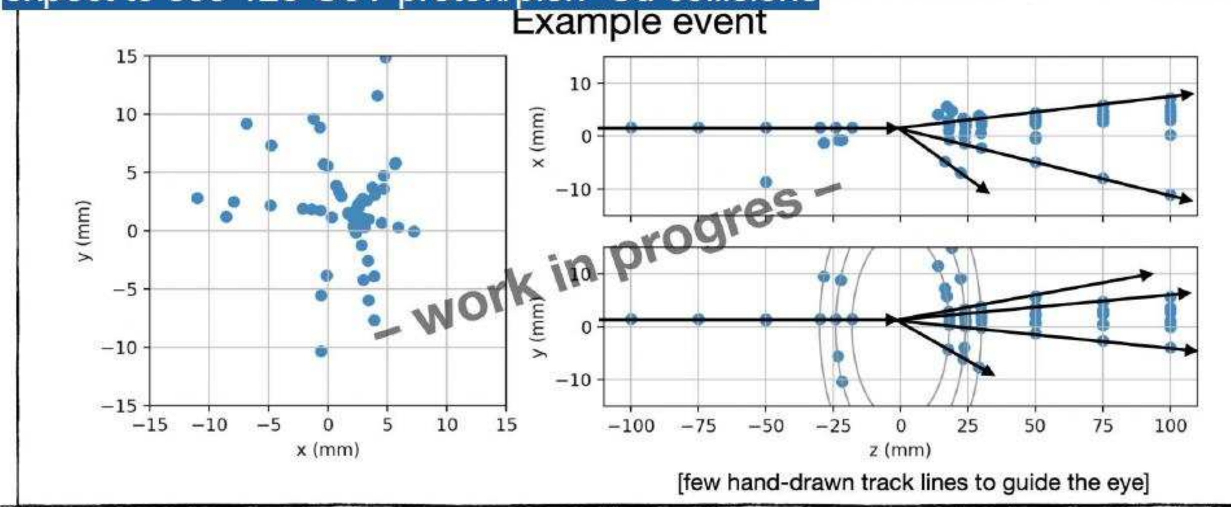
ALICE | WP4 meeting | 14 April 2022 | Domenico Colella 16

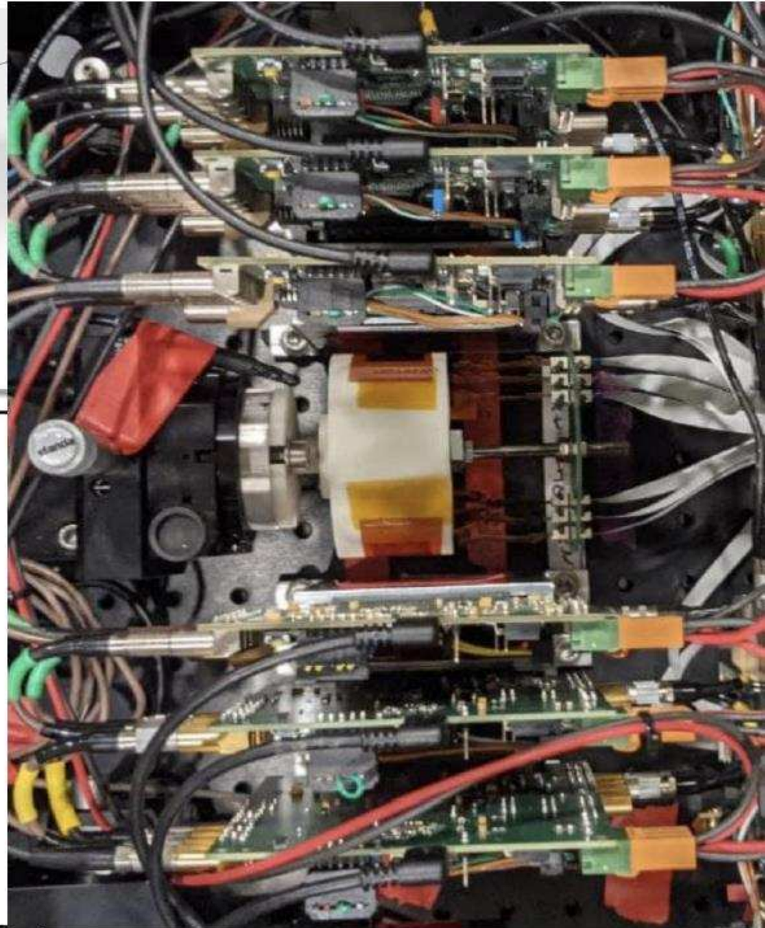
▷ **Extendable to MIMOSIS+ : $\lesssim$ 5 μm – O(1 μs) – 2 Gbits/s**

µITS3



Cu target in the center
expect to see 120 GeV proton/pion–Cu collisions

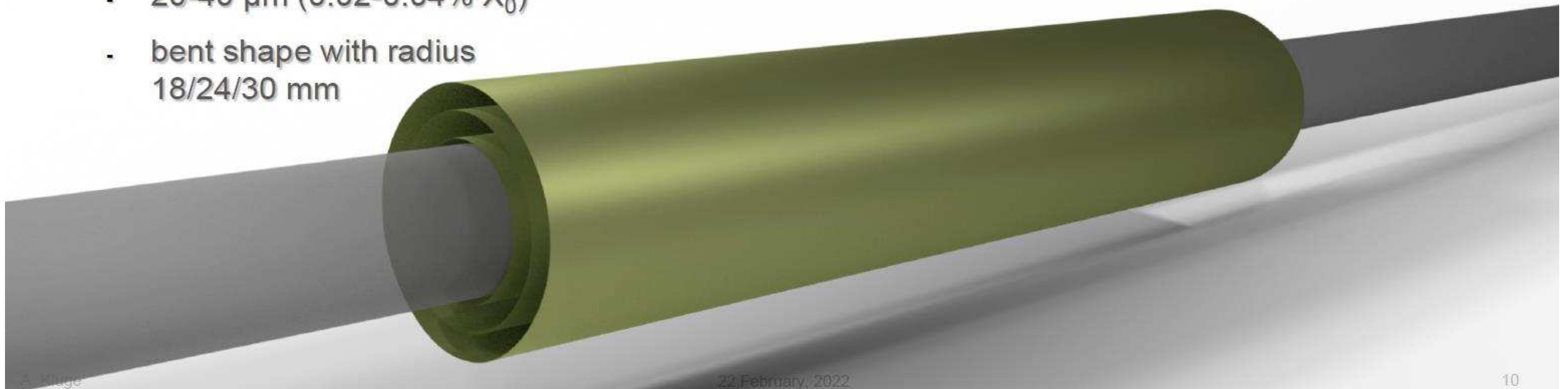




from A. Kluge - VCI 2022

ITS3 specifications & layout

- **Concept**
  - **replace inner 3 layers of ITS2 with ITS3**
  - 280 mm long sensor ASICs
  - out of 300 mm long stitched wafers
  - 20-40 μm (0.02-0.04% X_0)
  - bent shape with radius 18/24/30 mm
  - carbon foam rib to hold ASICs in place
  - air cooling
  - homogenous material distribution
- **6 sensor ASICs**
  - **2 halves * 3 layers**



from A. Kluge - VCI 2022

Which questions need to be answered?

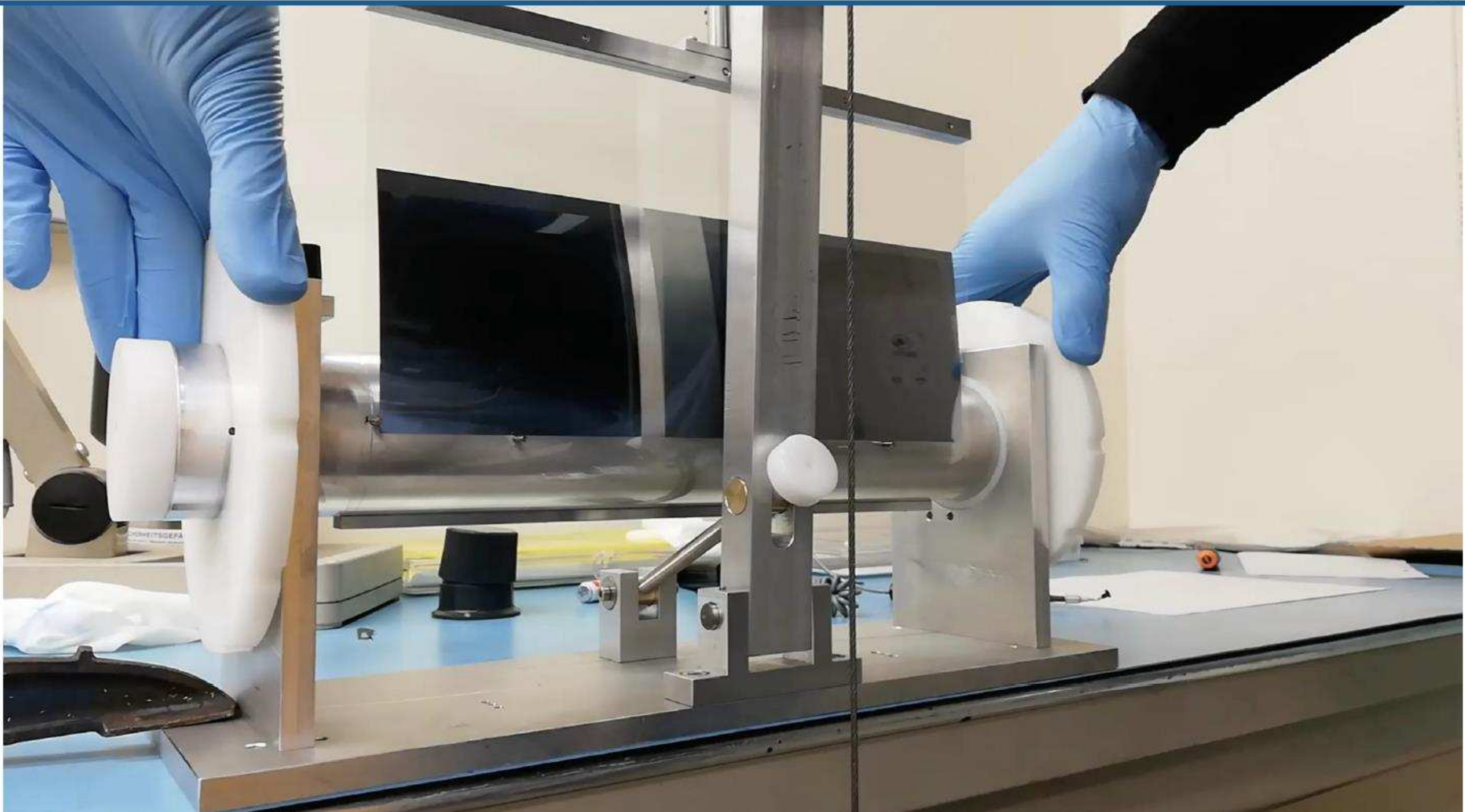
- **Idea**
  - remove all but the silicon sensor ASIC and
  - bend it around beam pipe

    for increased performance and mechanical stability
- **Questions**
  - Can thin silicon be bent without breaking?
  - Are bent silicon sensor ASICs functional?
  - Can long, thinned silicon sensors be integrated without a heavy CF structure?
  - Can the sensor be cooled with air only efficiently?
  - Can a 280 mm long silicon sensor ASIC be produced?
  - Can the sensors be connected without additional HDI?

A. Kluge 22 February, 2022 13

from A. Kluge - VCI 2022

Bending wafer scale silicon



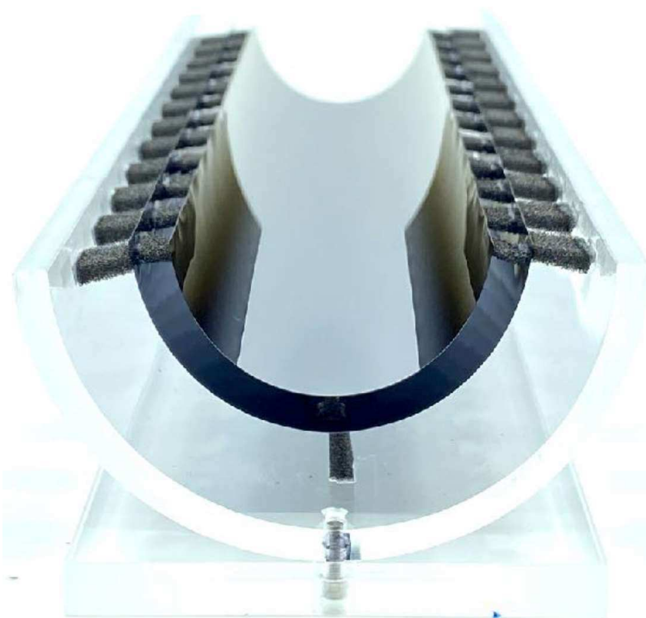
A. Kluge

from A. Kluge - VCI 2022

Layer assembly

Layer 2

Layers 2+1



Layers 2+1+0

3-layer integration successful!

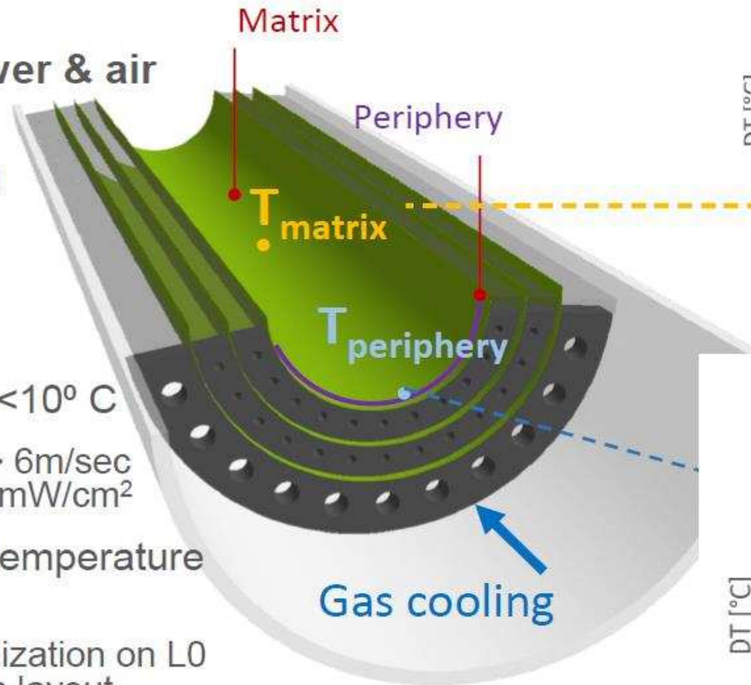
from ALICE-ITS3 - internal ⇛ **NOT TO COPY**

Wind tunnel cooling studies

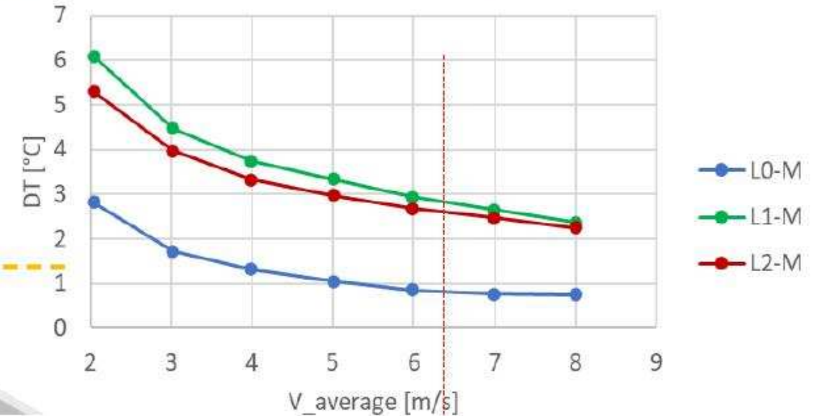
- **Tests with model and heaters**
  - **Different power & air speed**
  - **Carbon foam radiator are key for heat removal at periphery**
  - L1 and L2 DT <10º C

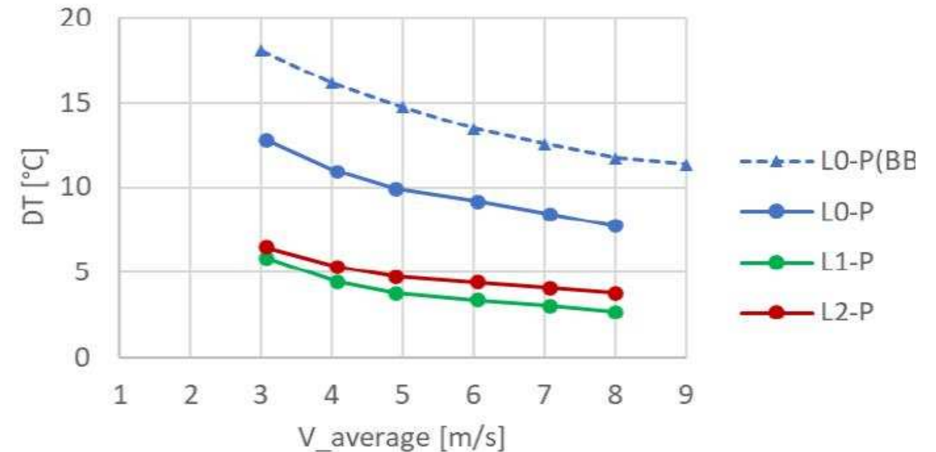
    for gas flow> 6m/sec and PW 900mW/cm²
  - L0 has larger temperature DT to air

    further optimization on L0 Carbon foam layout
  - Power density concentrated on 2.5 mm periphery



$DT = T_{periphery} - T_{air_in}$ Vs Airspeed





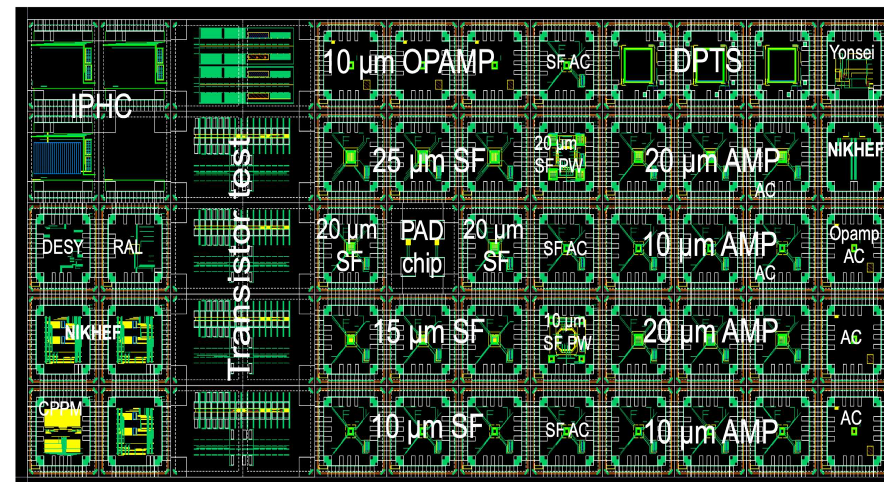
A. Kluge

22 February, 2022

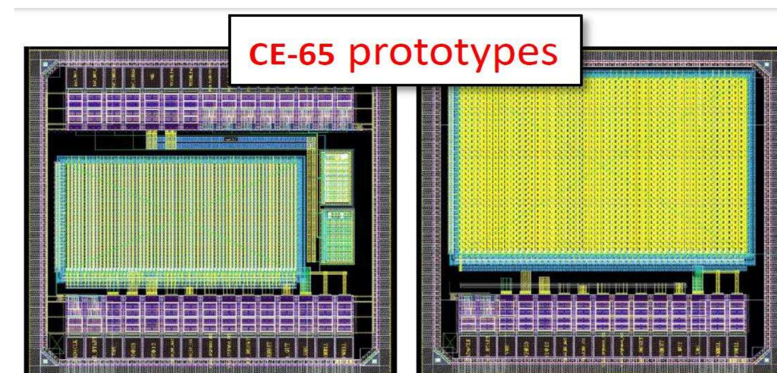
from A. Kluge - VCI 2022

Exploration of a 65 nm Imaging Technology

- **Motivations of the R&D:**
  - Smaller feature size than 180 nm technology used for MIMOSIS
    $\Rrightarrow$ smaller pixels, more in-pixel functionnalities,
    less power consumption, faster readout, ...
  - Imaging technology available since $\sim$ Spring 2020:
    includes stiching $\Rrightarrow$ multireticle sensors
  - R&D coordinated at CERN (ALICE-ITS3 & EP-div)
  - ITS3 goals: small pixels and very low material budget
    exploiting stitching for "supportless" detector layer



- **Prototyping at IPHC for MLR1 (2020):**
  - Design of "elementary" test structures with CERN
  - Design of 2 chips featuring arrays of 15x15 & 25x25μm^2 pixels
    with rolling shutter readout & analog output
  - Grouped submission (MLR1) submitted to TowerJazz
    for fabrication during Winter-Spring 2020-21
  - Tests under way: detection performances are promising

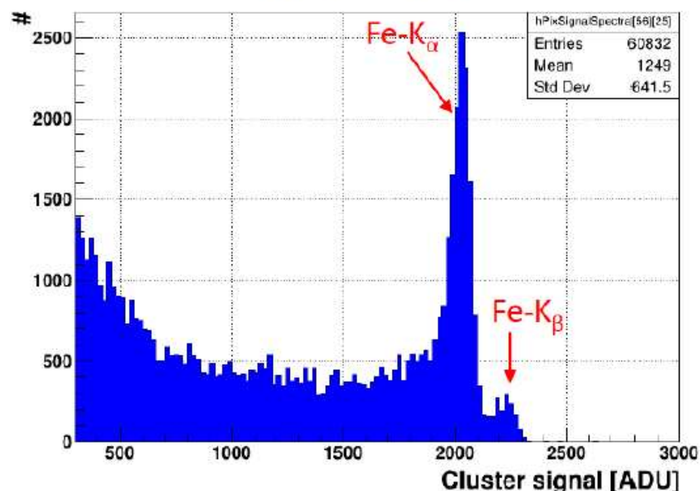


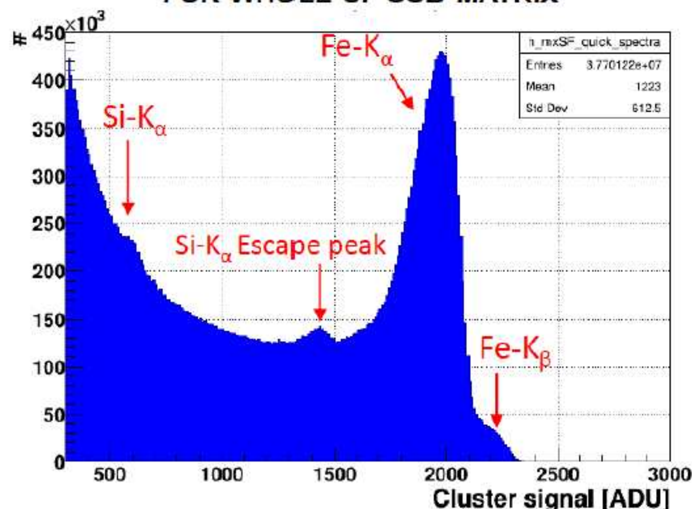
Variants A/B/C	Variant D
64 × 32 15 µm pitch	48 × 32 25 µm pitch

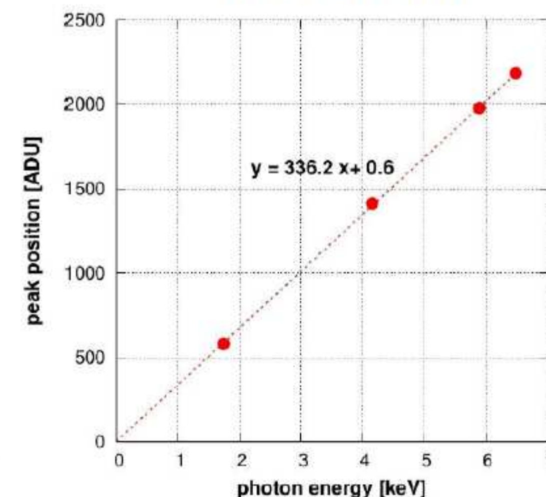
MLR1: CE-65 Proto. Testing Charge Collection with 15 μm Pitch

CE65 (IPHC): Exemplary ^{55}Fe spectra

Source follower sub matrix, optimised diode



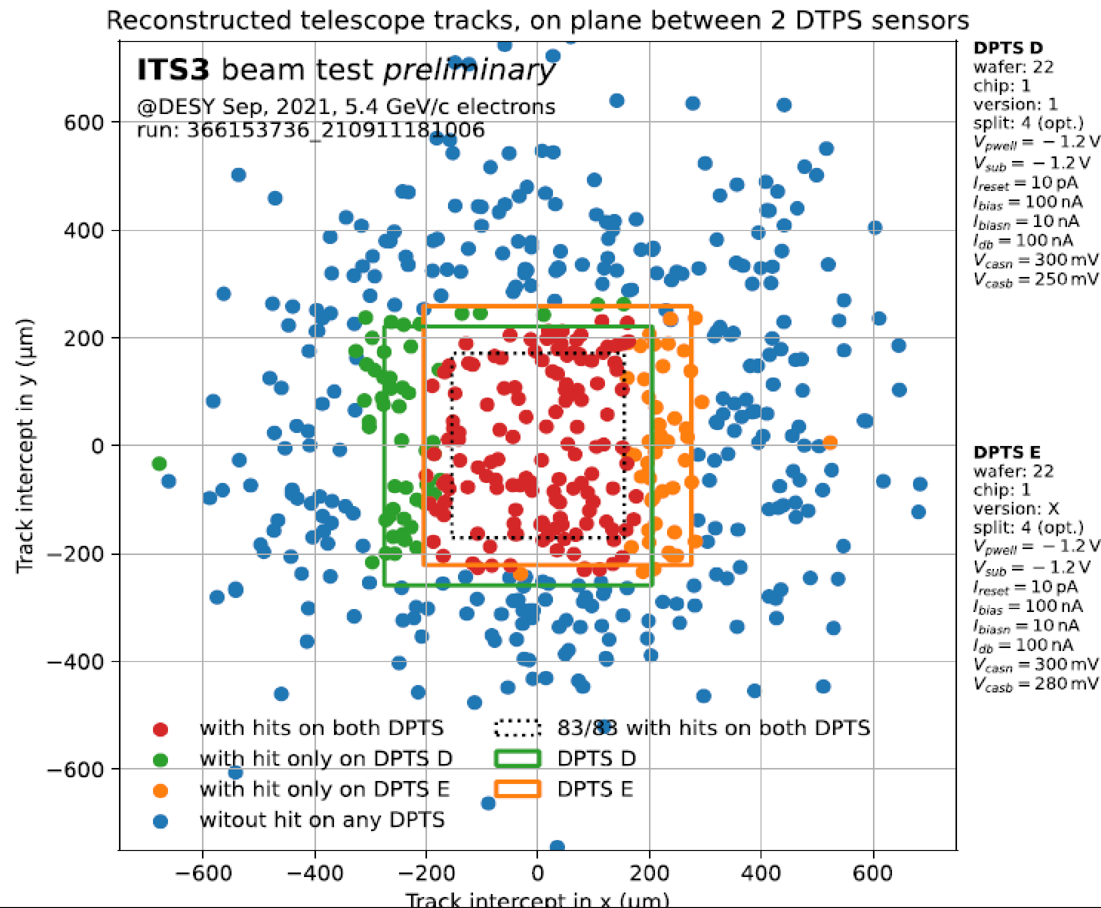




See S. Bugiel, A. Dorokhov et al, VCI

from VCI-2022 - S. Bugiel et al.

Beam test with Telescope with DPTS



- **Tracks without hit in the DPTS**
  - **have 100% shadow over DPTS**
- **166/166 tracks in DPTS1**
- **162/162 tracks in DPTS2**
- **and even for both in coincidence 83/83 tracks**
- **100% efficiency**
- **Excellent sensor/front-end performance already from first 65 nm prototype**

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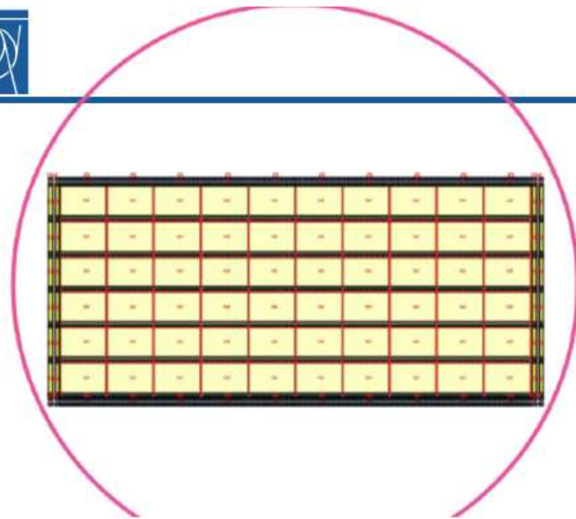
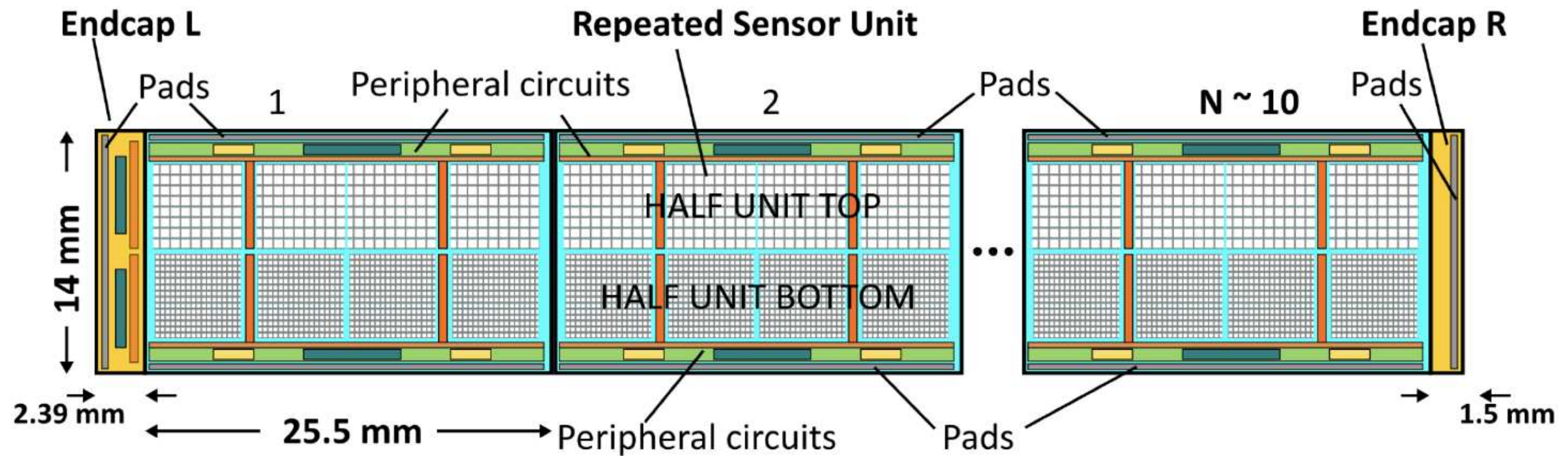
from A. Kluge - VCI 2022

Stitched sensor ASICs



- **Next big milestone in sensor design: stitching**
- **Design activity in full swing**
  - Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**



A. Kluge 22 February, 2022 40

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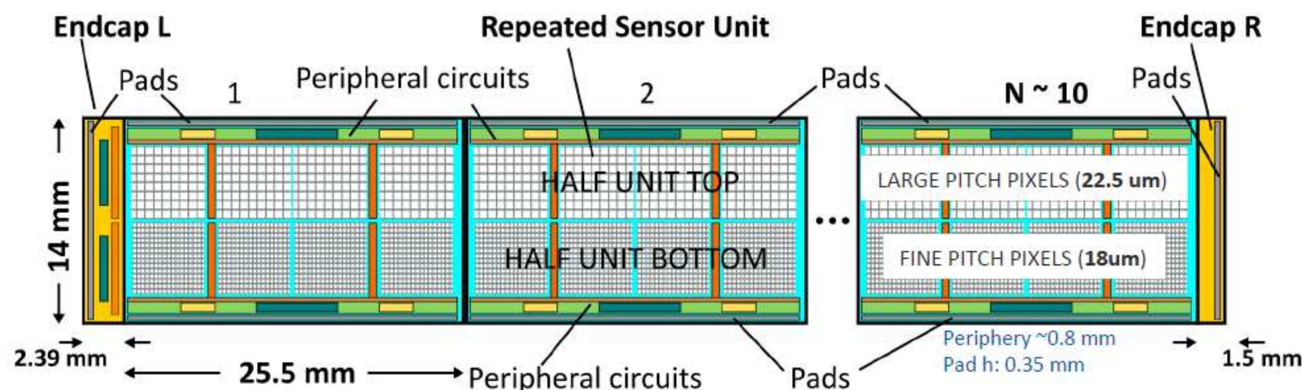
Next Step: ER1 including 25 x 1.5 cm large sensor in 65 nm Technology

MOSS Monolithic Stitched Sensor Prototype



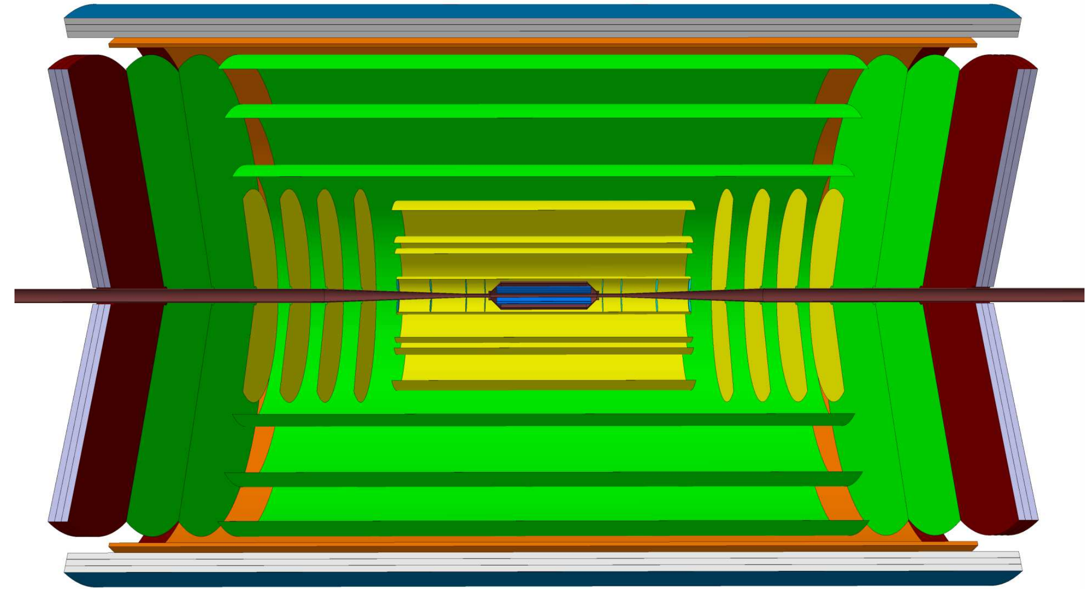
Primary Goals
Learn Stitching to make a particle detector
Interconnect power and signals on wafer scale design
Learn about yield and DFM
Study power, leakage, spread, noise, speed

- Large sensor abutting identical but functionally independent sub-units
  - Repeated Sensor Unit, Endcap Left, Endcap Right
  - Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

On behalf of MOSS team

ALICE-3 Concept: Which Guidance for ILD-2030 ?

- **Full Si tracking concept based on large (stitched) bent CMOS sensors in TPSCo 65 nm technology to be installed during LHC-LS4 (2033-34)**



- **Sensor thickness $\sim$ 30 μm (VD) - 100 μm (tracker)**
- **Epitaxial layer thickness $\gtrsim$ 8 μm (signal $\sim$ 500 e$^-$)**
- **Pixel pitch $\simeq$ 10 μm (VD) $\Rrightarrow$ $\sigma_{sp} \simeq$ 2.5 μm**
  (tracker: 50 μm pitch)
- **$\Delta_t \gtrsim$ 100 ns in nearly all layers**
- **Power $\simeq$ 70–100 mW/cm^2 (for 100 ns)**
- **Active cooling, e.g. μ-channel or polyimide pipes**
  $\hookrightarrow$ synergies with LHCb, CERN-EP R&D, ECFA R&D)
- **Mat. budget/layer $\gtrsim$ 0.1% (VD) to 1% (tracker) X$_0$**
- **20 ps TOF layers (CMOS sensors, e.g. FASTPIX like),**
  outside tracker (R=85 cm, beyond FW/BW disks) and outside VD (R=20 cm, after front BW/FW disks)
- **PID (TOF): $p_t(e^-) \lesssim$ 0.5 GeV/c, $p_t(\pi/K/p) \lesssim$ 2 GeV/c**
- Not considered here: VD (3 layers) inside BP (R=5mm) & RICH for PID

MAPS FOIL: Embedded thin CMOS Pixel Sensors

Chip embedding

ALICE

- The idea is to embed chips into flexible printed circuit boards
- Interconnection is done by metallisation (like via plating in ordinary PCBs)
- The idea is not new, but:
  - it was not followed up much
  - we made some important progress recently

[Dulinski, FEE-2014] [Di Mauro, ITS2 WP4] [SERVIETTE]

IPHC FEE-2014, Argonne, USA

Novel approach for ultra thin sensor packaging:

use of a "standard" flex PCB process for chip embedding in plastic foils

The goal: < 0.1 % of X_0 per sensor layer (large area ladder, all included)

Embedding principle

- Gluing between two kapton foils
- Opening vias using lithography
- Metallization: Al (5-10 μm)
- Lithography to pattern metal
- Gluing of another kapton foil for deposition of second metal layer

No wire bonding, excellent mechanical chip protection

Chips embedding

- Option proposed by R. De Oliveira
- No soldering needed, contacts are implemented by the standard metallization process
- Flex and chips are kept flat by a thick (1-2 mm) Cu support plate (not shown here) removed at the end after mounting on C-fiber
- Single chip test OK, first 9 chips assembly on-going (metrology after step 1)

3 SERWIETE project

bump bonding; metal traces 1 μm thick; 1 analogue MIMOSA-18 sensor; ~13 mm; ~43 mm; sketch of metal traces 14 μm thick; 3 binary MIMOSA-26 sensors; ~14 mm; ~120 mm

Figure 6: Sketch of the two SERWIETE prototypes. On the left, the 2010 prototype equipped with 1 analogue output MIMOSA-18 sensor. On the right, the 2011 prototype with 3 binary output MIMOSA-26 sensors with indication of some metal traces.

LCWS/ILC2010

CONCLUSIONS

- ILD DESIGN MAY INTEGRATE PROGRESS ON SC SENSORS & THEIR SERVICES (INCL. GEOMETRY)

- SCIENTIFIC PRIORITIES FOR ILD (ALL E_{CM}):

  1) few μm spatial resolution & suppressed mat. budget (power !) rather than r.o. speed

     $\Rrightarrow$ services are of prime importance & deserve substantial R&D $\Rrightarrow$ priority !

  2) very fast (few tens of ps) sensors may be added ”soberly”,

     e.g. 1 layer behind VD or FW/BW disks & 1 layer outside trackers

     $\Rrightarrow$ evaluate added value (PID, BG rejection, ...) versus overhead in services resulting from syst. integration

- PRIVILEGED ENVIRONMENT FOR THE VXD R&D:

  ⋇ ALICE-ITS3 W.P.-3 & W.P.-4 (together with CERN-EP R&D W.P.-1.2)

  ⋇ Development of stitched (multi-reticle) CMOS pixel sensors $\Rrightarrow$ drastic mat. budget reduction expected

  ⋇ Exploration of 65 nm TPSCo process $\Rrightarrow$ low power, thin (bending), small pixels

  ⋇ Should end up with a novel vertex detector taking data in $\gtrsim$ 5 yrs

- PRIVILEGED FRAMEWORK FOR LARGE TRACKERS: ALICE 3 PROJECT $\rightarrowtail$ LHC-LS4 (2033-34)

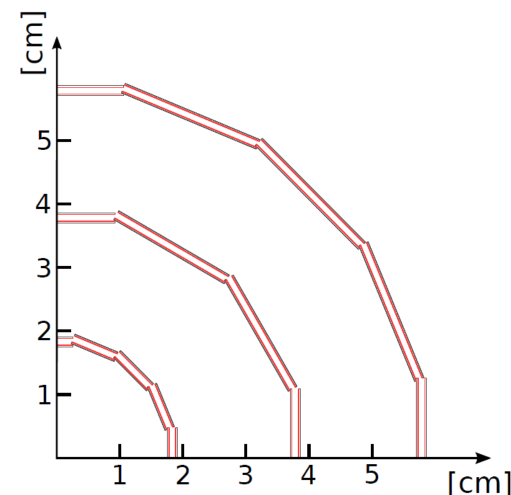
  ⋇ Requirements for tracking sub-systems overlap those of ILD

  ⋇ Lettre of Intent: CERN-LHCC-2022-009 / LHCC-I-6038

Vertex Detector Requirements: Spatial Resolution

- **Vertexing goal at FCCee:**
  - ⋇ $\sigma_{\Delta} d_0 \leq 5 \oplus 10 - 15/p \cdot sin^{3/2}\theta \;\; \mu m$
  - ⋇ assume 3 double layers (R ranging from 17.5 to 60 mm)
  - ⋇ $\sigma^{sp}_{R\phi,Z}$ = 3 μm
  - ⋇ 3 dble-layers with water cooling ($\equiv$ ALICE-ITS2)

    $\Rrightarrow$ 0.6 - 0.7 % X_0/dble-layer

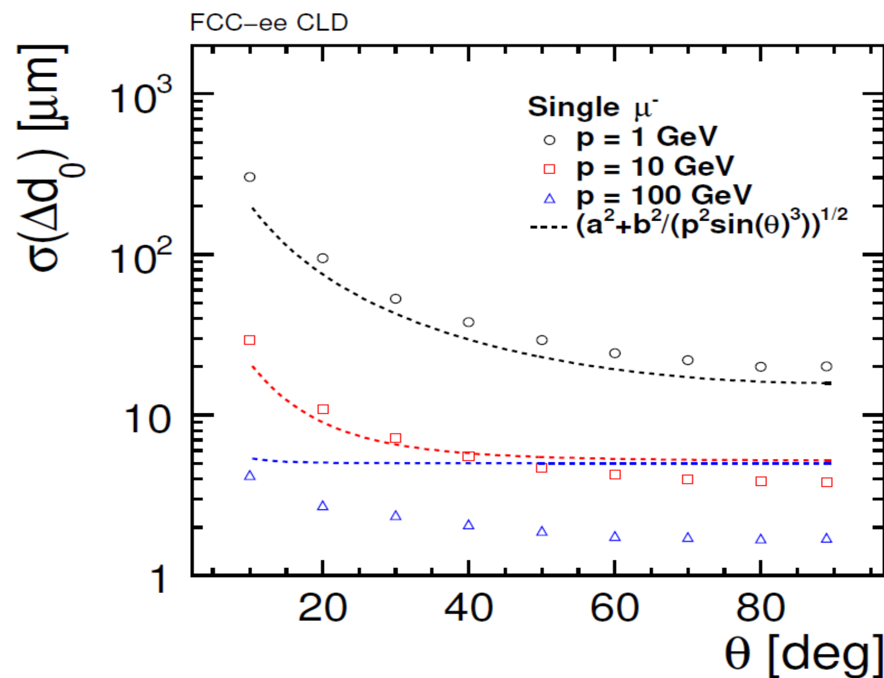


- **Beam pipe of FCCee:**
  - ⋇ dble-shell of Be with water cooling $\equiv$ 0.34 % X_0
  - ⋇ gold coting (5 μm) $\equiv$ 0.15 % X_0

- **ILD VXD & beam pipe material budget:**
  - ⋇ VXD: 0.3 % X_0/dble-layer with air cooling

    (possibility of power pulsing)
  - ⋇ BP: sgle-shell of Be with no cooling $\equiv$ 0.14 % X_0

  $\Rrightarrow$ b $\simeq$ 10 GeV$\cdot\mu m$ instead of 15 GeV$\cdot\mu m$



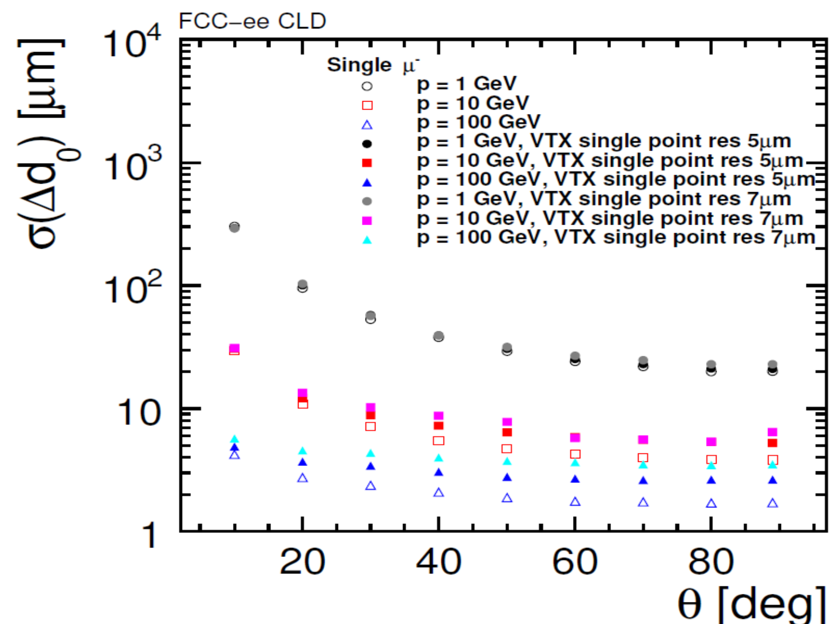
(a) d_0 resolution

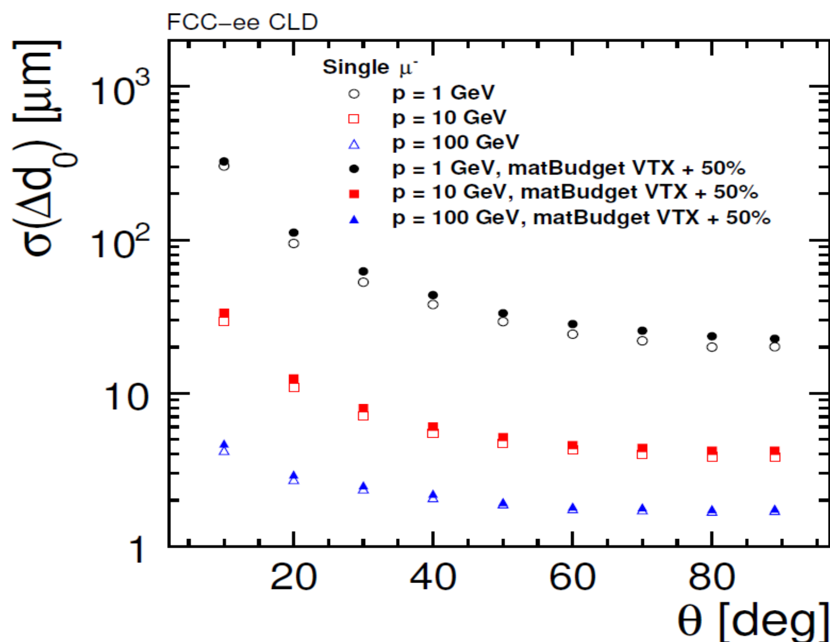
Vertex Detector Requirements: Single Point Resolution (2/2)

- **Impact of relaxed constraint on single point resolution:**
  - $\sigma^{sp}_{R\phi,Z}$ = 3 μm $\longrightarrow$ 5 and 7 μm
  - dilutes $\sigma(\Delta d_0)$ by up to factor 2

- **Impact of increased dble-layer material budget:**
  - add 50 % to dble-layer material budget
  - impact is nearly marginal $\Rrightarrow$ impact $<$ 1 GeV/c ?

    What if mat. budget would be twice less ?





(a) d_0 resolution

ALPIDE: Single point resolution and Cluster multiplicity

ALPIDE Position resolution and cluster size

V_{BB}=-3V

Resolution (μm)

Average Cluster Size (Pixel)

Threshold (e^-)

Resolution | Cluster Size @ V_{BB}=-3V

W7-R10 Non Irradiated
W7-R7 Non Irradiated
W7-R17 TID Irradiated, 206 krad
W7-R5 TID Irradiated, 205 krad
W7-R38 TID Irradiated, 462 krad
W7-R41 TID Irradiated, 509 krad
W8-R5 NIEL, 1.7e+13 1MeV n_{eq} / cm^3
W8-R7 NIEL, 1.7e+13 1MeV n_{eq} / cm^3

VXD Upgrade -Requirements

Radius range: R	14 – 135 mm (**)
Tracking & Vertexing performance at least as good as current VXD	
Single point resolution(*)	< 15 um
Total material budget	< (2x 0.2% + 4x 0.7%) X_0
Robustness against radiation environment	
Hit rate(*)	~ 120 MHz/cm^2
Total Ionizing Dose(*)	~ 10 Mrad/year
NIEL fluence(*)	~ 5.0×10^{13} n_{eq}/cm^2/year

(*) requirement for the innermost layer (R=14mm)
(**) Optionally, we may include also the CDC inner region (135<R<240mm)

- Be prepared for a major interaction region redesign
  - Allow large safety factors against backgrounds
- Take advantage of technology development
- Possible performance improvements
  - Impact parameter and vertexing resolution
  - Tracking performance for low pT tracks
  - Lower trigger latency
  - L1 trigger capabilities

Feb 23, 2022 F.Forti - Belle II Upgrades

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- Little overlap in sensor requirements: $< (15\ \mu m,\ 100$ ns, 200 mW/cm^2)
- **But:** cooling system possibly relevant for FCCee vertex detector