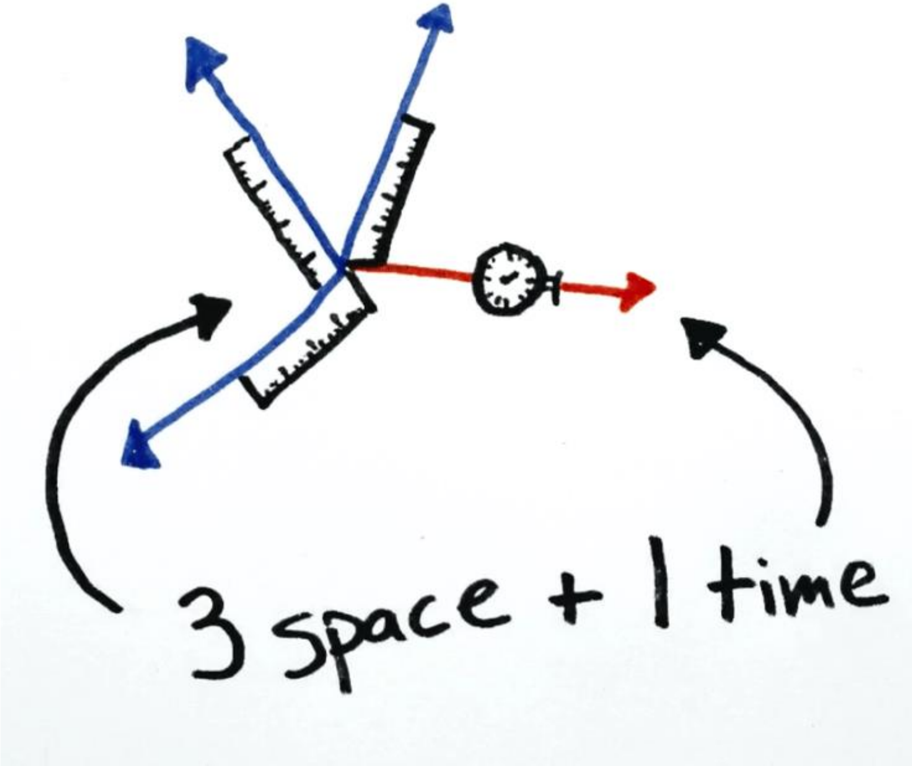
Review of LGAD-based enabling sensors for a low-material 4D tracker system

ILD strategy meeting

May 17th, 2022



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EXCELENCIA MARÍA DE MAEZTU

IFCA Instituto de Física de Cantabria

CSIC Consejo Superior de Investigaciones Científicas

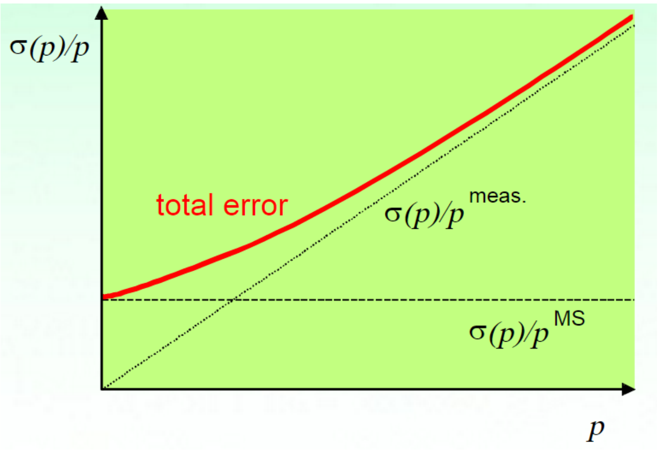
UC Universidad de Cantabria

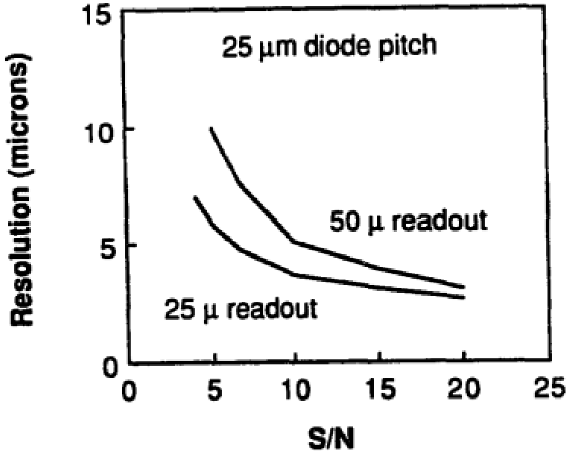
Outline

- Precision timing basics
  - Jitter, time-walk and limit time resolution
- Low Gain Avalanche Detectors for timing.
  - LGAD vs PIN and SiPM
- LGAD architectures for 4D tracking.
- Summary

Motivation… not just timing

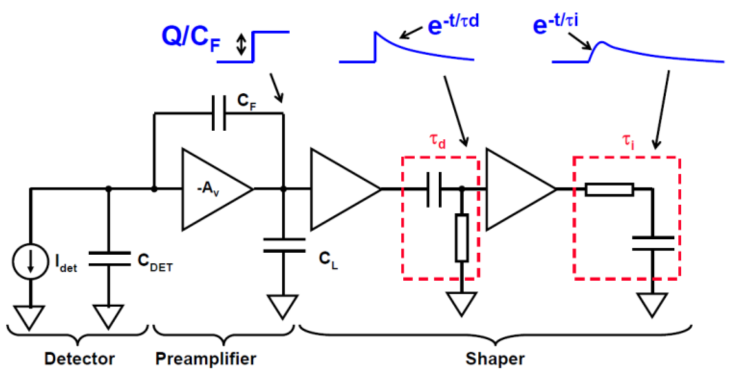
– Sensors with large SNR and small material budget to enable few tens of picoseconds time stamping of MIP particles (high precision ToF).
– Integrated signal amplification increases the Signal-to-Noise ratio increasing the tracking resolution:
  - Thinner detectors (reduction of the **multiple scattering**)
  - Improved **intrinsic hit resolution**.



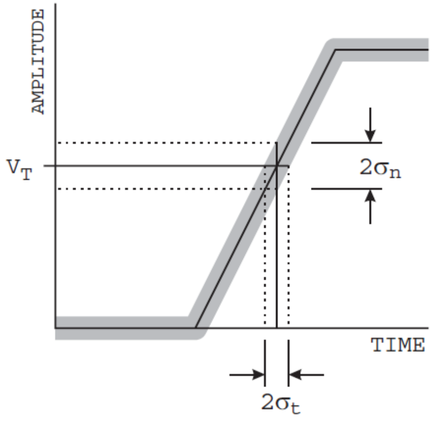


Precision timing: basics

Timing 101: Timing resolution contributions - Jitter



Leading Edge Timing



Ideally, for a constant amplitude pulse, the time resolution is given by the jitter which depends on:

- **Noise** (dominated by the **amplifier** noise)

$$v_n \propto \sqrt{f_u} \propto \sqrt{\frac{1}{t_{ra}}}$$

- **Signal amplitude** (dominated by **sensor's** response)
- **Rise time** (dominated by **amplifier** risetime)

$$t_r = \sqrt{t_{rs}^2 + t_{ra}^2}$$

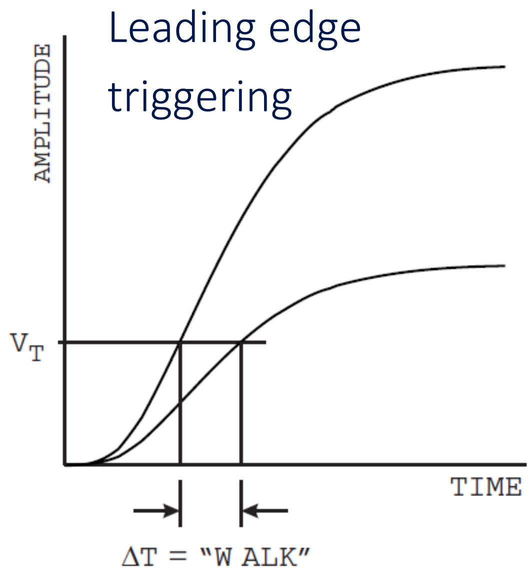
$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} \qquad \frac{dV}{dt} \approx \frac{V}{t_r} \rightarrow \sigma_t = \frac{t_r}{SNR}$$

$$\sigma_t \propto \frac{1}{V_0} \frac{1}{\sqrt{t_{ra}}} \sqrt{t_{rs}^2 + t_{ra}^2}$$

Typical bandwidth of HL-LHC timing layer preamplifier of around 400 MHz $\rightarrow t_r \sim t_{ra} \sim$ 1ns then a (modest) SNR of about 30 should provide a timing resolution of about 30 ps

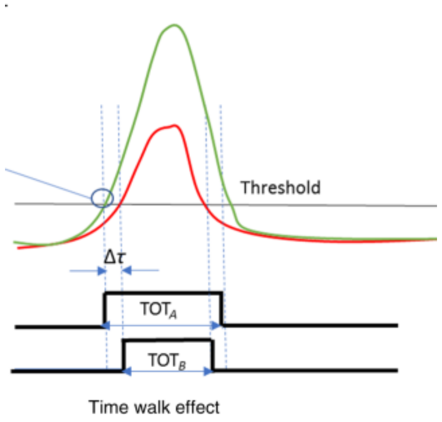
Timing 101: Time resolution contributions – Time walk

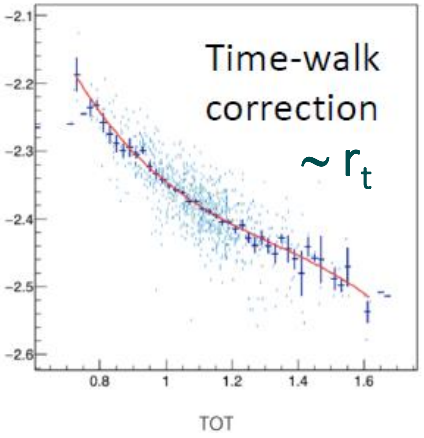
In real conditions, the pulse amplitude is not always constant.



Option 1

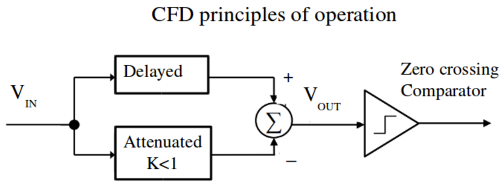
Correct the time shift using the pulse amplitude

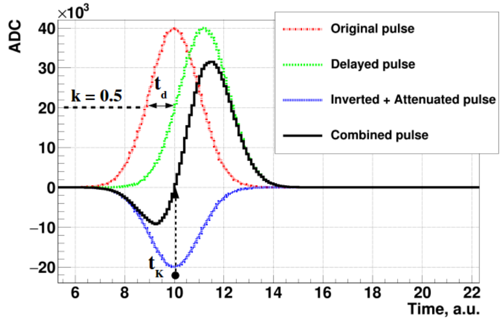




Option 2

Constant Fraction Triggering





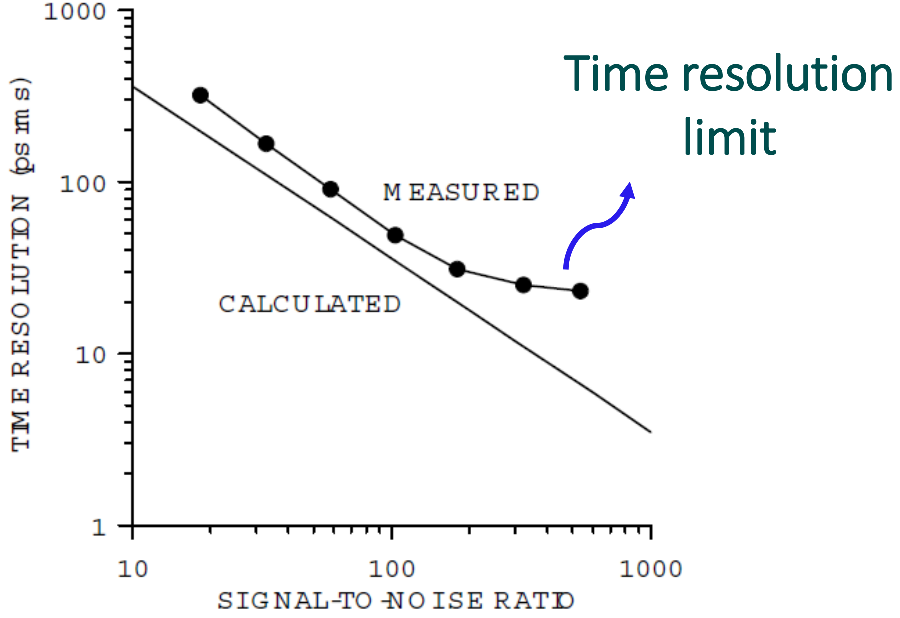
Both methods: Amplitude-corrected LET and CFT have a similar performance as long as THE SHAPE OF THE PULSE'S LEADING EDGE IS CONSTANT.

Caveat: ToT correction is a off-line method while CDF is a real-time correction.

Timing 101: Time resolution contributions – limiting systematics

Jitter induced by pulse shape changes

- Changes on the leading edge shape (i.e., different rise times or its distortions) translate into additional jitter



System aspects:

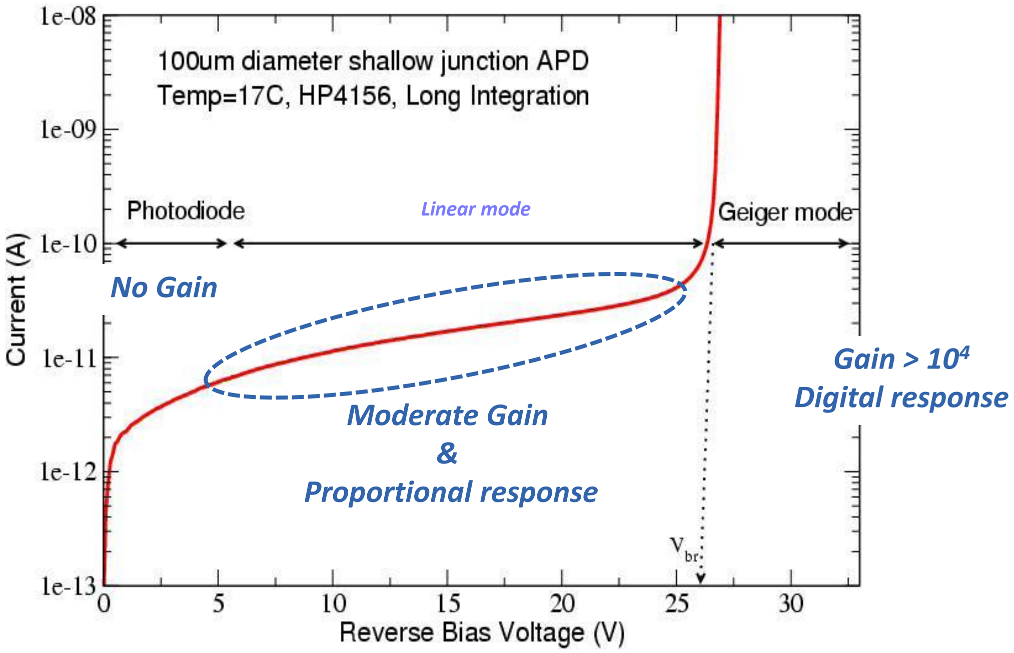
- TDC resolution.
- ADC (ToT) resolution limits time-walk correction.
- Clock distribution (jitter, slew and thermal drifts).

These are the limiting factors and off-line data-based corrections are needed.

Enabling Technology: Low Gain Avalanche Sensor

Silicon sensors as enabling sensing technology for 4D tracking ?

- Silicon-based diodes provide both **fast rise time and relatively large signal/noise ratio**.
- Well **stablished high-precision tracking technology** (electrode patterning)
- Three operating modes: no signal gain (**PIN**), proportional (**APD**) and Geiger mode (**SiPMT**).



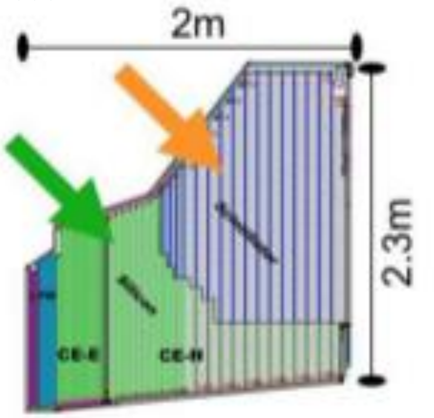
[1] A.G. Stewart et al. in Proc. of SPIE, Vol. 6119, 2006

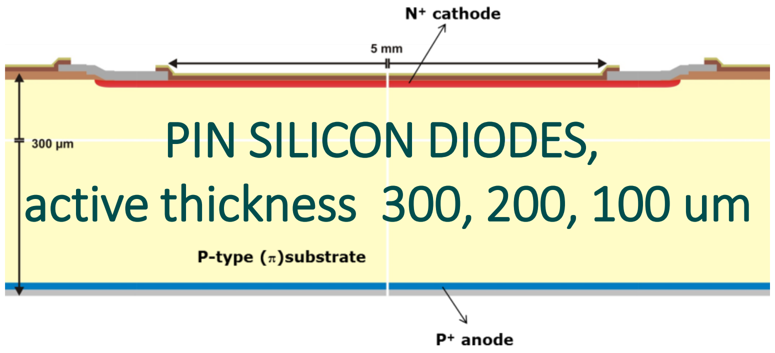
Timing with PIN diodes : CMS HGCAL as case of use

- Very reliable and mature mass production technology
- Main limitation: low SNR

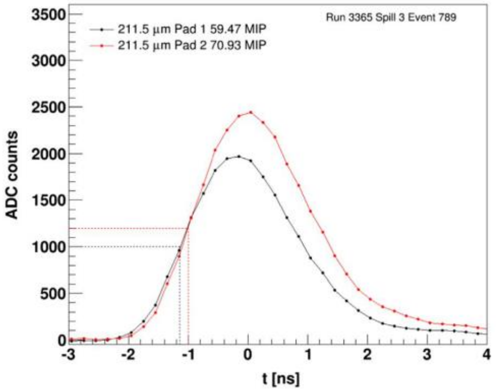
Scintillator + SiPM

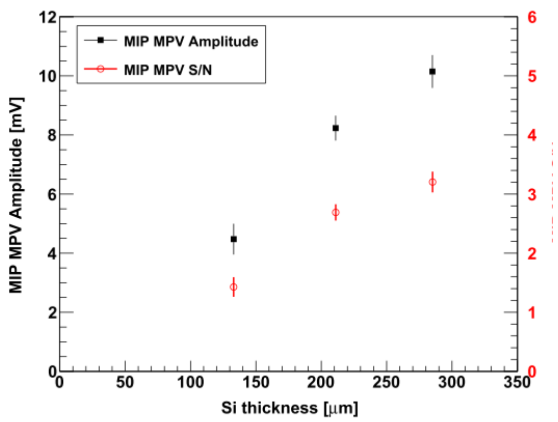
Pin diode

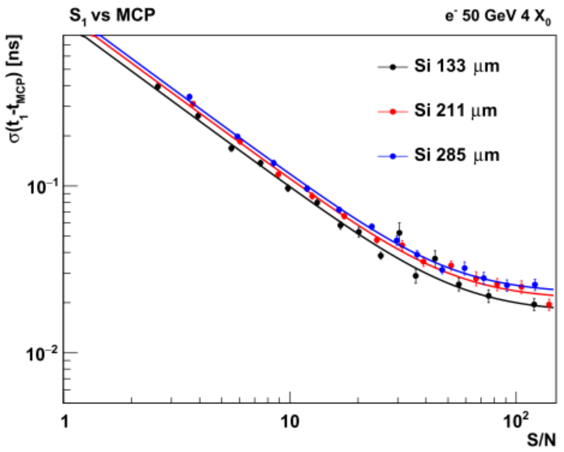




PIN SILICON DIODES,
active thickness 300, 200, 100 um



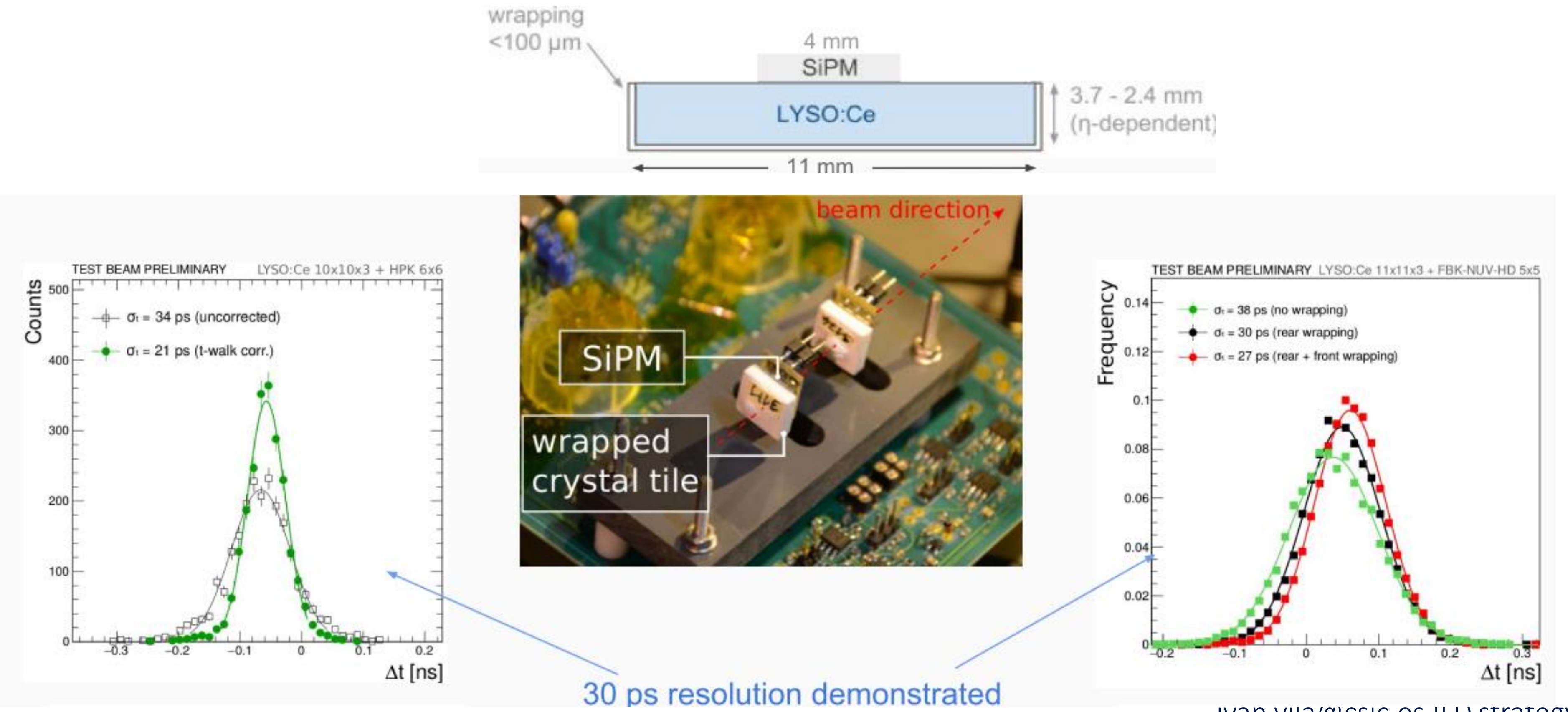




E. Currás, Nucl.Instrum.Meth. A859 (2017) 31-36

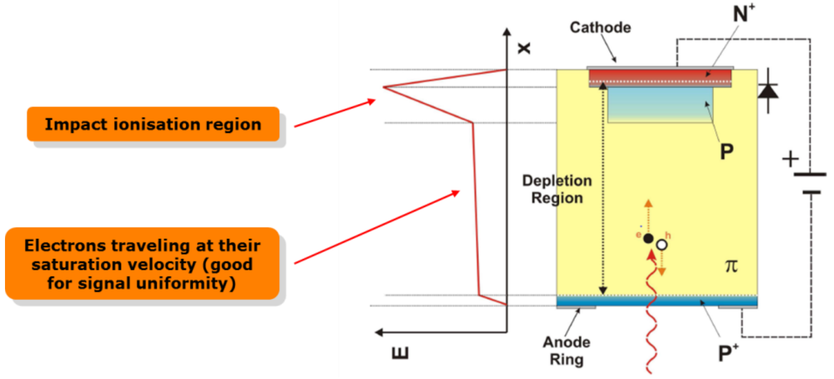
Silicon Photomultipliers: (Geiger-mode APD)
Case of use BTL detector at CMS

- Mature technology, mass produced and cheap sensing element.
- Main limitations: moderate radiation tolerance < 2×10^{14} n_{eq}/cm2 and concept with intrinsic poor spatial resolution, high fake pulse rate

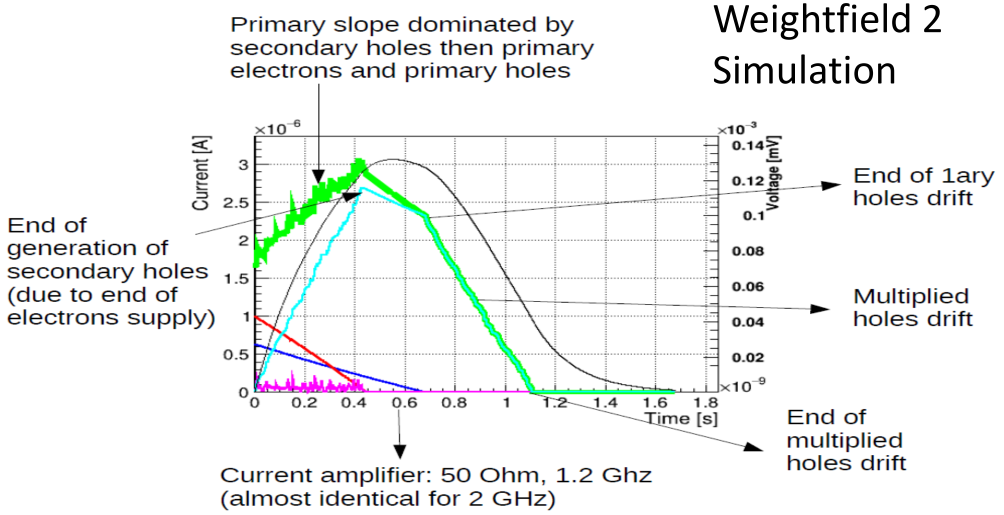


Avalanche mode diode (Low Gain Avalanche Detector LGAD) :

- Proportional multiplication mode (impact ionization of primary carriers)
- Main advantage: custom SNR for optimal for timing and tracking (introduced by IMB-CNM)



Weightfield 2 Simulation



LGAD have a much larger **rise-time** (collecting time of primary electrons) than PIN (all carriers ballistic movement).

⇨ Go thinner to reduce the collecting time of the primary electrons and make $t_{rs} << t_{ra}$

LGAD **SNR** better than PIN due to gain

⇨ Taylor the gain for optimal jitter wrt limit time resolution

LGAD for HL-LHC timing layers (status report in nutshell)

- Provide about 30ps MIP time stamping for disentangling between the different interaction vertices.
- LGAD is the baseline technology of the endcap MIP timing detector for the HL upgrade of Atlas and CMS experiments
- Main challenges (and solutions)
  - **Radiation tolerance to (mostly) neutrons and protons:**

    Damage Mechanisms: primary carriers trapping, acceptor deactivation, mean-free-path reduced, electric field modification,

    Solutions: Thin bulk (higher electric field), co-doping with Carbon (suppression of the acceptor removal mechanism), deep multiplication layer.

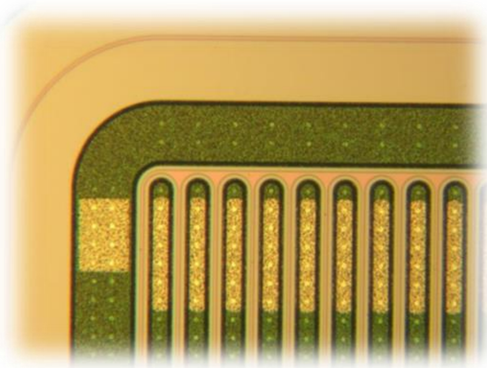
    Current status: radiation tolerance up to 1.5 e15 n/cm2 achieved (conservative bound).
  - **Long-term reliability:**

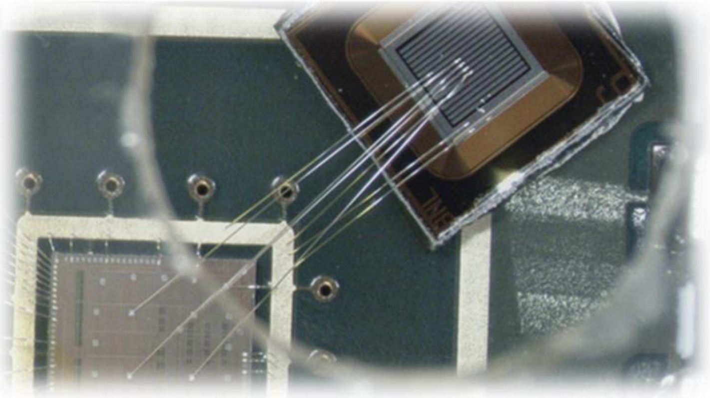
    Damage mechanism: very rare highly ionizing events induce fatal diode breakdown (also in PINs @ very high HV)

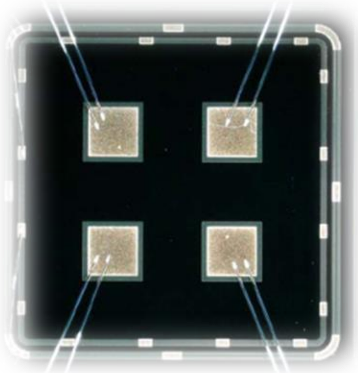
    Solution: limited average E field (< 11V/um).

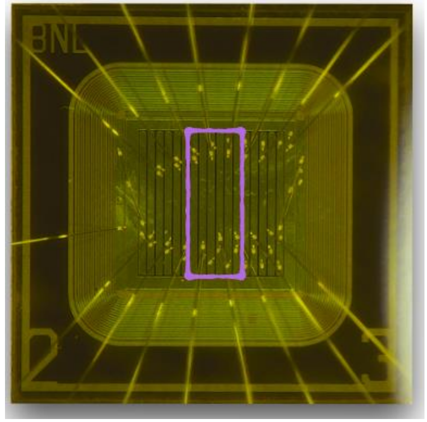
    Current status: fatal damage mechanism understood and implementation of maximum voltage bias.
  - Large scale **manufacturing yield (99.8% of good pad achieved by HPK in recent manufacturing runs).**
  - Increase **fill-factor and increase the granularity** ← Next of the talk

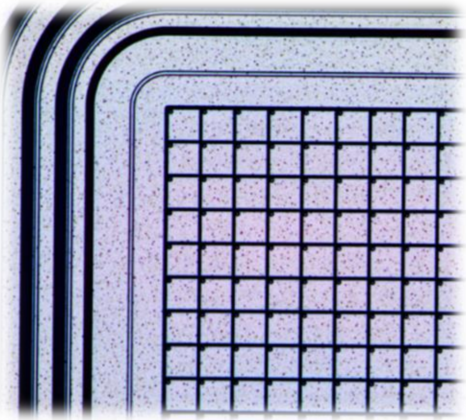
Panorama of LGAD technologies for 4D tracking

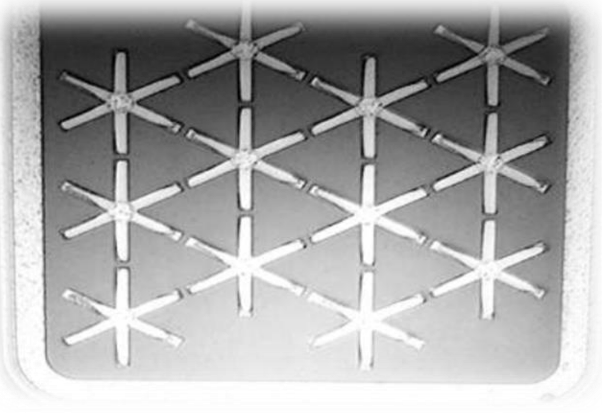










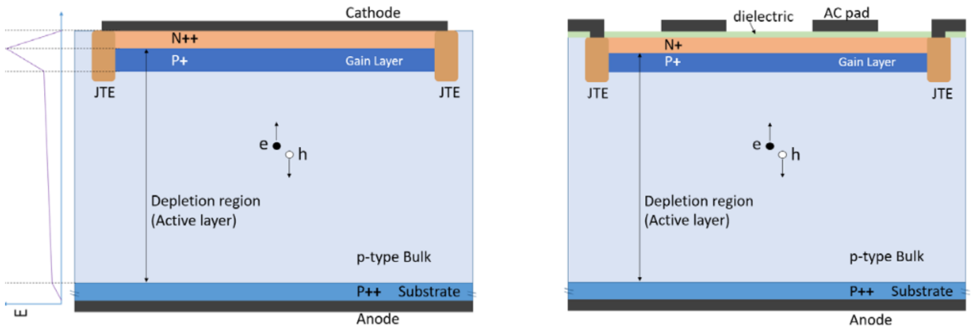


Towards a LGAD-based 4D tracking enabling sensor

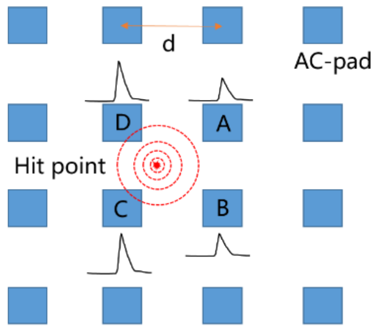
- Several technologies for improving the spatial resolution and increased fill factor:
  - Resistive AC-Coupled LGADs (**AC-LGADs**)
    (First manufacturing run from FBK; new foundries joining IHEP, BNL, HPK, etc.)
  - Trench-isolated LGADs (**TI-LGAD**)
    (first manufacturing run from FBK)
  - Thin Inverse Low Gain Avalanche detectors (**iLGAD**)
    (Design completed at IMB-CNM, first production run ready to start)
  - Deep Junction Low Gain Avalanche detectors (**DJ-LGAD**)
    (first manufacturing from BNL)

Resistive AC-Coupled Silicon Detectors

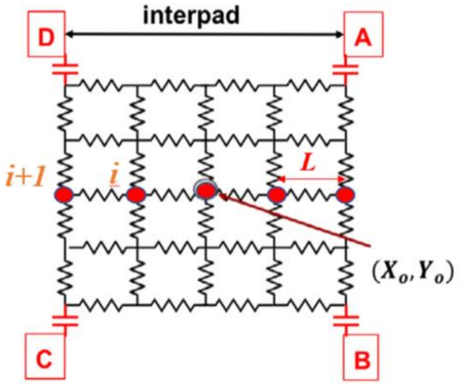
- Resistive readout of Si strip detectors first proposed by Radeka in 1974 (IEEE Transaction on Nuclear Science NS-21 (1974) 51)
- Feasibility studies on the Resistive DC readout for a **linear collider** tracker were carried out by J. K. Carman, et al in 2011 (NIM A 646 (2011) 118)
- 1D Resistive AC coupled microstrip as tracking sensors for the **linear collider** were introduced by IMB-CNM (D. Bassignana et al., 2012 JINST 7 P02005)
- 2D Resistive AC coupled readout in LGAD introduced by FBK (M. Mandurrino et al., IEEE Electron Device Lett. 40(11) (2019) pp.1780-1783.):
  - Non-segmented LGAD gain layer; segmented electrode on top of a dielectric layer .



LGAD (Low-Gain Avalanche Diode) AC-LGAD (AC-coupled LGAD)



AC-pad layout scheme

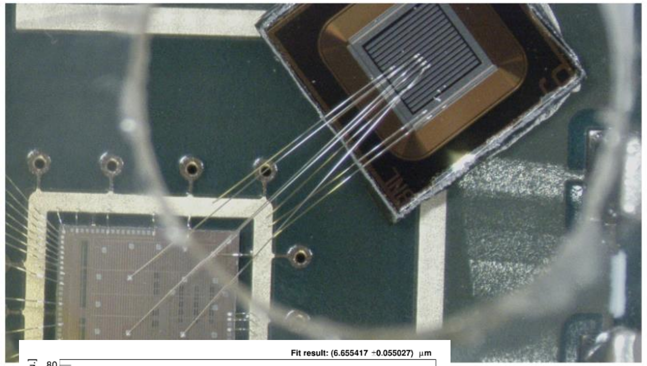


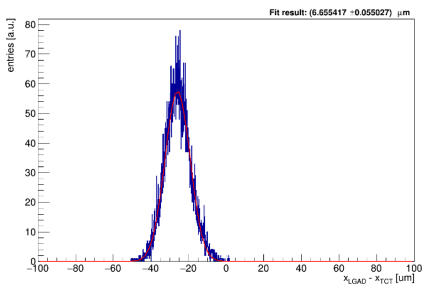
Mengzhao Li, 39th RD50 Workshop, Nov 2021

- Hit position reconstruction algorithm based on charge sharing among the electrodes (Smarter ML algorithms possible) achieve sub-pitch hit resolution figures.
- Timing resolution improved by multiple electron readout. Not as simple as sqrt of # of electrodes improvement due to correlations)
- Advantages:
  - 100% fill factor
  - high spatial resolution for large pitch devices.
- Limitations:
  - Hits on top of the electrode with do not have charge sharing (resolution degraded to the electrode size).
  - Maximum hit occupancy one hit / electrode pitch.

Resistive AC-Coupled Silicon Detectors (2)

- Beyond the proof-of-concept limitations.
- 16 strips, pitch 100 µm, gap 44 µm
- Central and neighbouring strips wire bonded to the four input channels on the ALTIROC ASIC (Atlas HGTD ROC)
- Strips chosen to be far from the device guard-ring to minimize border effects Lateral strips on their left and right are wire-bonded to the same ground as the ASIC
- Second prototype bonded to dedicated discrete front-end amplifier board from Fermilab + fast digitizer.
- **Test beam studies** of second prototype

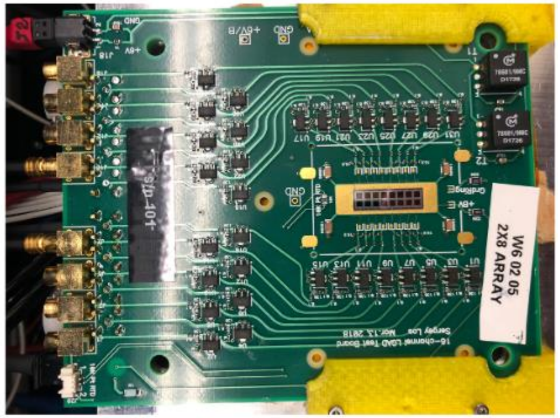




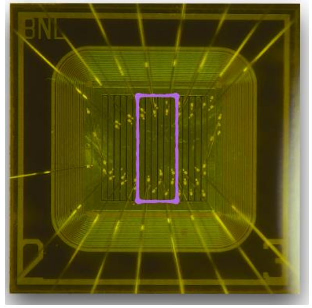
RD50

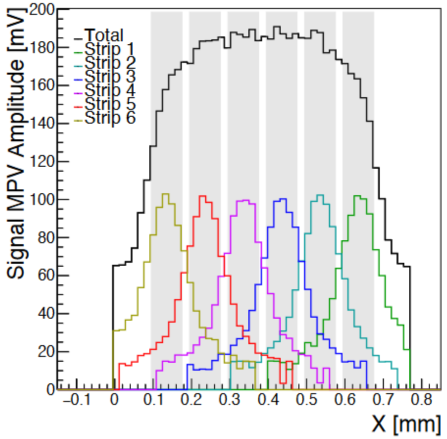
G. D'Amen, C. Madrid, 39th RD50 Workshop, Nov 2021

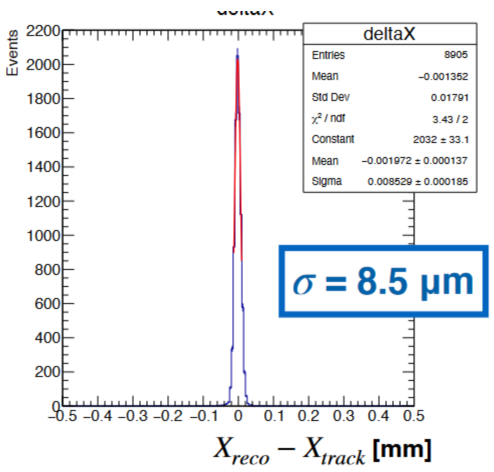
Interstrip spatial resolution estimated with laser TCT setup. Estimated resolution of 6 um.



16-ch sensor LGAD on Fermilab readout board







Timing resolution between 30 and 40 ps

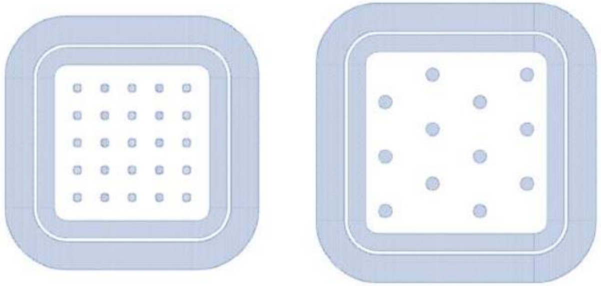
Discontinuities are observed where the relative fraction is large or when we get direct hits to the strip

Resistive AC-Coupled Silicon Detectors (3)

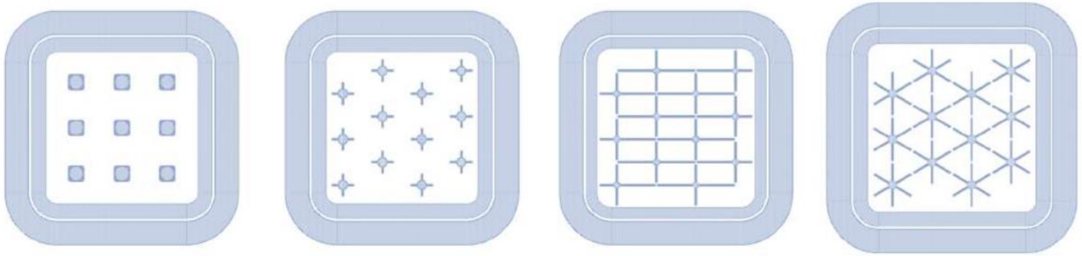
- Moving beyond the current technology limitations: trade off between signal detection efficiency and electrode area.

M. Mandurrino, 39th RD50 Workshop, Nov 2021

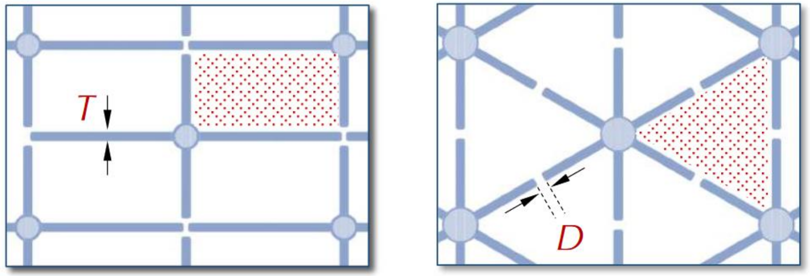
- Two different **array configurations**: *regular* and *staggered*



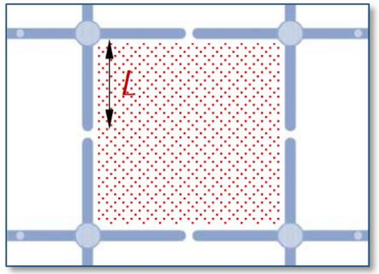
- Several **pad geometries**: *squares*, *circles*, *crosses*, *stars*, etc...



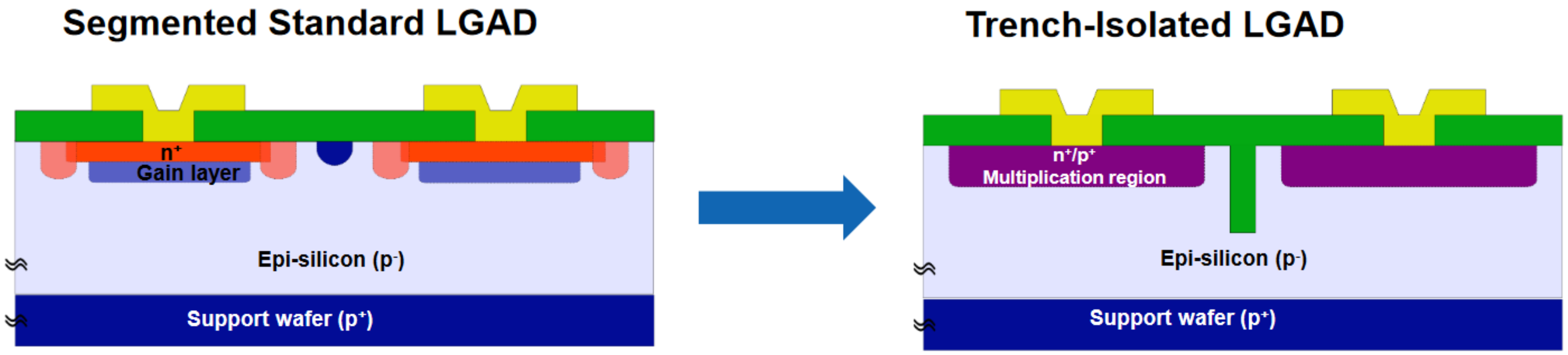
- **Signal confinement** with *cross* or *star* AC-pads in the **staggered arrays**:

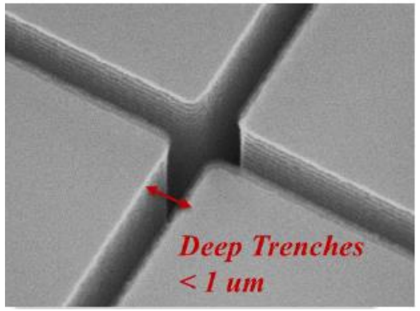


- and in the **regular arrays**:



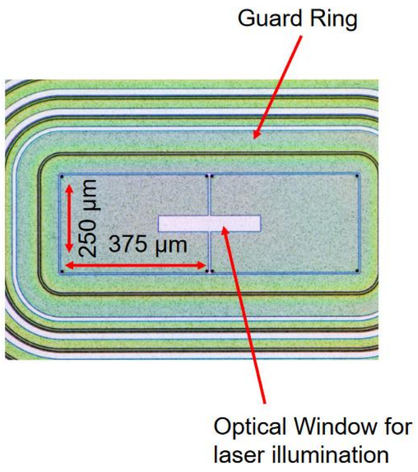
Trench-isolated Low Gain Avalanche detectors (**TI-LGAD**)

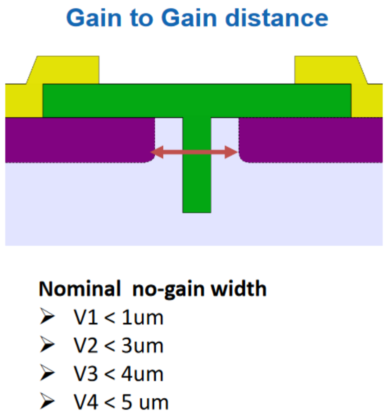


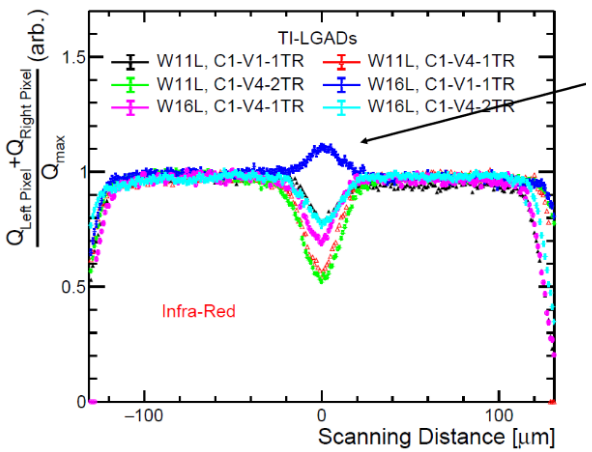


G. Paternoster, 39th RD50 Workshop, Nov 2021

- Pixel border region hosts structures to control E field (JTE, p-stop, etc..)
- Trench isolation could drastically reduce inter-pixel border region down to few μm
  - Typical trench width < 1 μm (max aspect ratio: 1:20)
  - Trench filling with: SiO2, Si3N4, Polysilicon



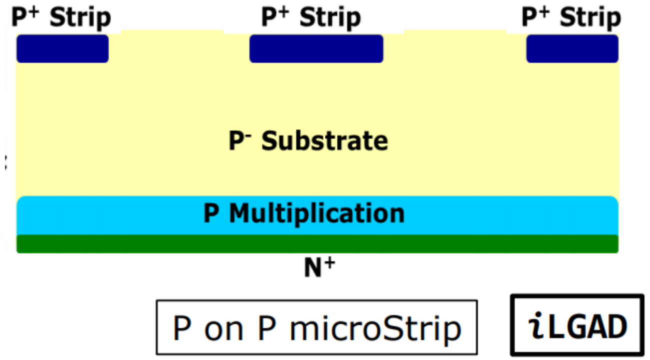


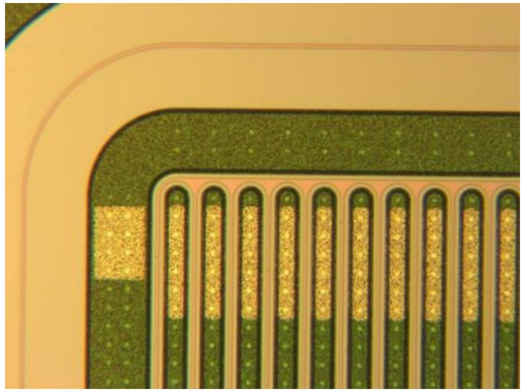


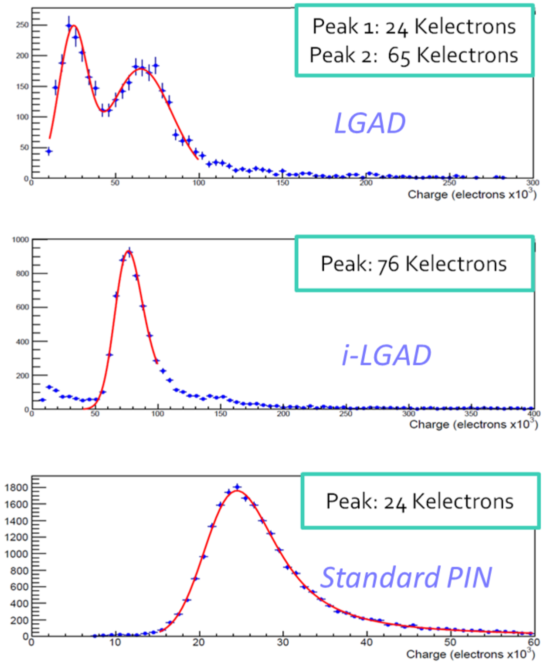
(Thin) Inverse LGAD (iLGAD)

I. Vila, 13th Trento Workshop, February 2018

- Continuous multiplication layer, segmented hole readout.
- Proof-of-concept from IMB-CNM prototype demostrated at test beam (300um thick and no time readout.).

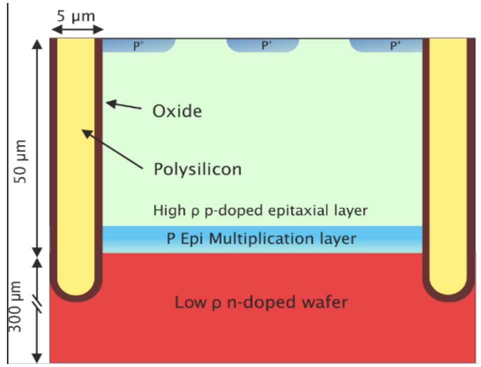


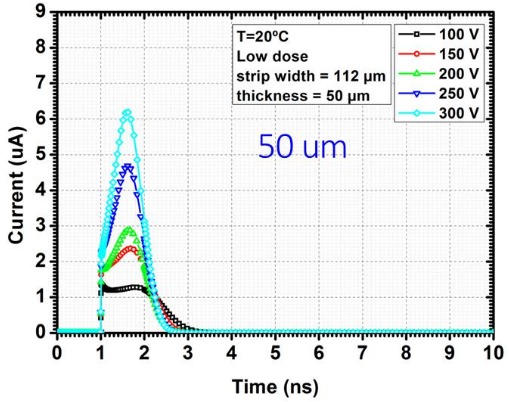




Gain Spatial Uniformity: Collected Charge

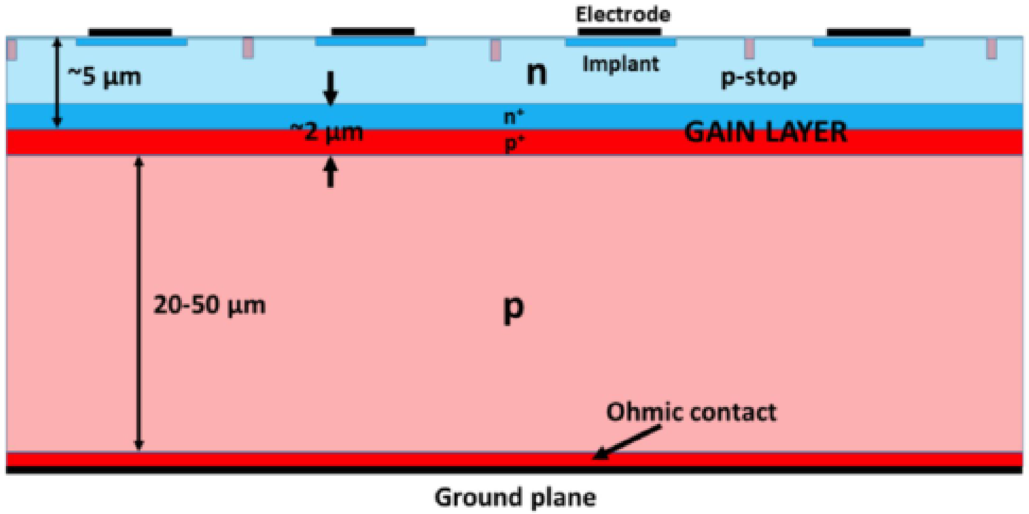
- Thin Single-sided design being manufactured at IMB-CNM



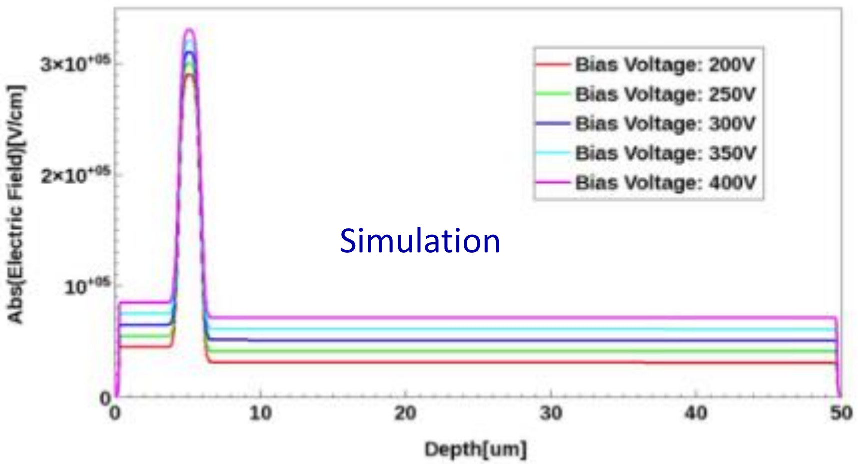


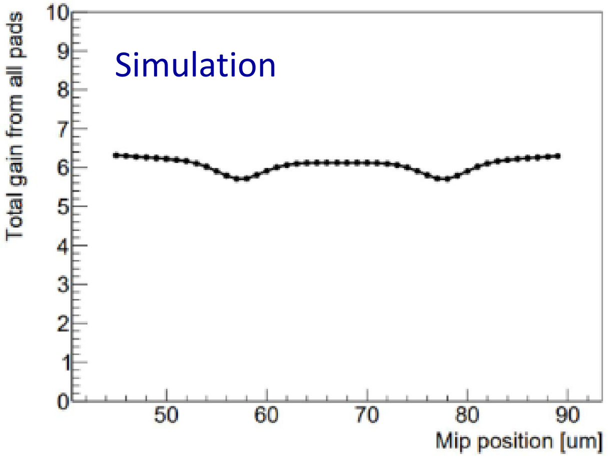
Deep Junction - LGAD

C. Gee, 39th RD50 Workshop, Nov 2021



- Advantageous to bury high p-n junction several um below the surface of the sensor so fields low at surface, allowing conventional granularization
- Electric field in p-n junction is high enough to maintain drift-velocity saturation
- Maintains fine granularity on order of tens of microns
- Preserves direct coupling of signal charge to readout electrodes
- Initial prototype manufacturing at BNL





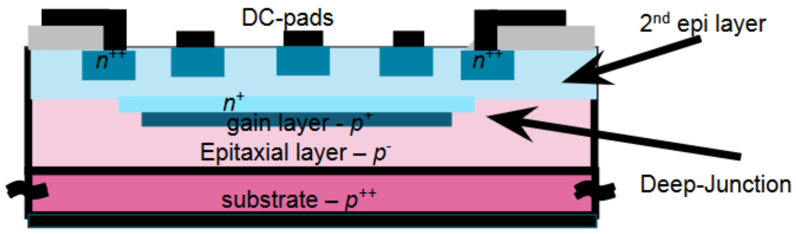


Diagram credit: BNL

Take home messages

- LGAD (HEP jargon for an APD with moderate gain) is the solution towards:
  - larger SNR (decoupled from the material) for O(10ps) hit resolution
  - O(10um) spatial resolution with fine electrode segmentation and AC coupling
- Many 4D LGAD architectures are under intense R&D.
- The next stepping stone in the development of a true 4D tracking sensor will be based on a hybrid sensor design with LGAD interconnected to timepix4 ASIC (AIDAInnova WP6)
- The technology is maturing and attracting the interest of major manufacturing companies BUT still a long way to go:
  - Complete proof-of-concept studies.
  - Reliability (long term stability, noise and destructive breakdown)
  - Manufacturing yield?
  - Scalability (larger area sensors) ?
  - Uniformity ?
  - Radiation tolerance fine pitch devices?
- Other strategies for the implementation of a 4D tracking should be also considered: PIN diodes with special junction geometries (TimeSPOT project) or monolithic CMOS based.

Final (personal) remark: The elephant in the room

- I do not see any technical showstopper for the LGAD sensors as true 4D sensing technology.
- Quite confident that LGAD sensor can become the baseline technology for the next generation of large 4D tracker systems.
- But LGAD are hybrid sensors interconnected to a dedicated readout ASIC:

The feasibilty of a front-end readout electronics with a relatively high density of readout channels is still to be proven; the power consumption and the corresponding heat disipation could become the showstopper.

THANK YOU FOR YOUR ATTENTION