Impact of non-ILC collider option on Power Management of the detector

Some material for helping/triggering the discussion

ILD meeting – 4 October 2022

Few considerations about the powering

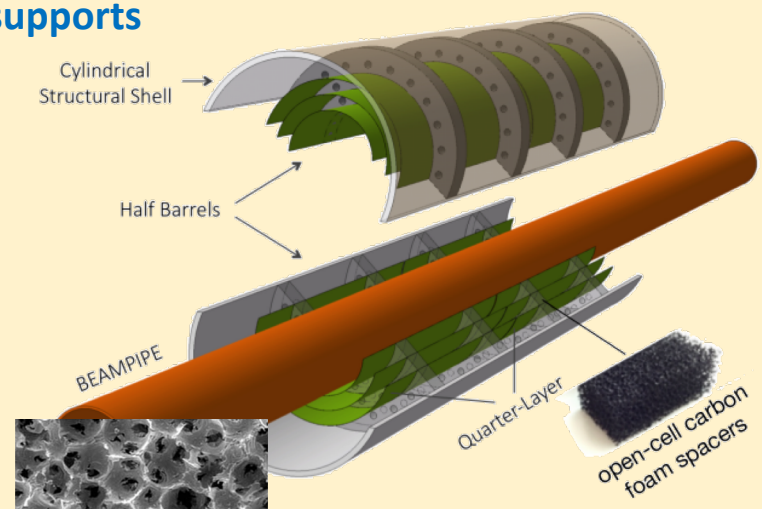
Material budget on the tracking part is an issue

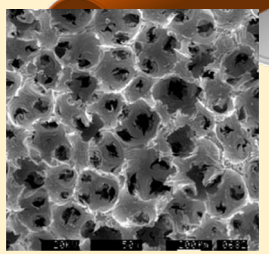
Air flow cooling to not increase the material budget in vertex (up to 20 mW/cm2) could work

Example of ALICE LS3 Upgrade:

Curved wafer-scale ultra-thin CMOS Active Pixel sensors

Using air flow cooling through low density **graphite foam supports**





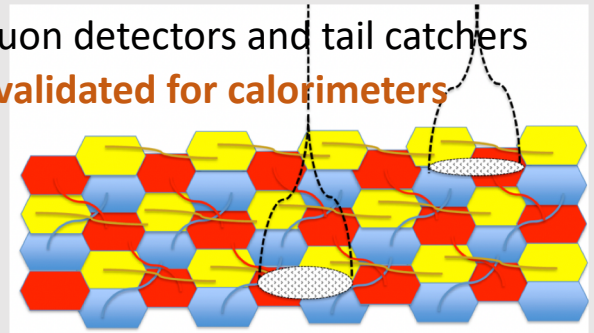
Scanning electron micrograph of the carbon foam surface

The huge number of **calorimeter** channels (and with higher occupancy than for the ILC) **will probably impose the need of cooling.**

This impacts in the design a could affect the overall performance (sampling fraction, extra dead spaces…) and homogeneity

But, is it possible to ***reduce the readout channels without decreasing the granularity***? (lower powering but also cheaper devices)

New scheme ***(woven strips)*** developed by Lyon group for RPC readout with a factor 30 reduction for muon detectors and tail catchers but **need to be validated for calorimeters**



With four PCBs

In addition, the impact of the different conditions as B, dimensions or low energy, etc… on the calorimetry goes forward than cooling and other things will need to be reevaluated/studied

Some thoughts from Felix

No power-pulsing means that

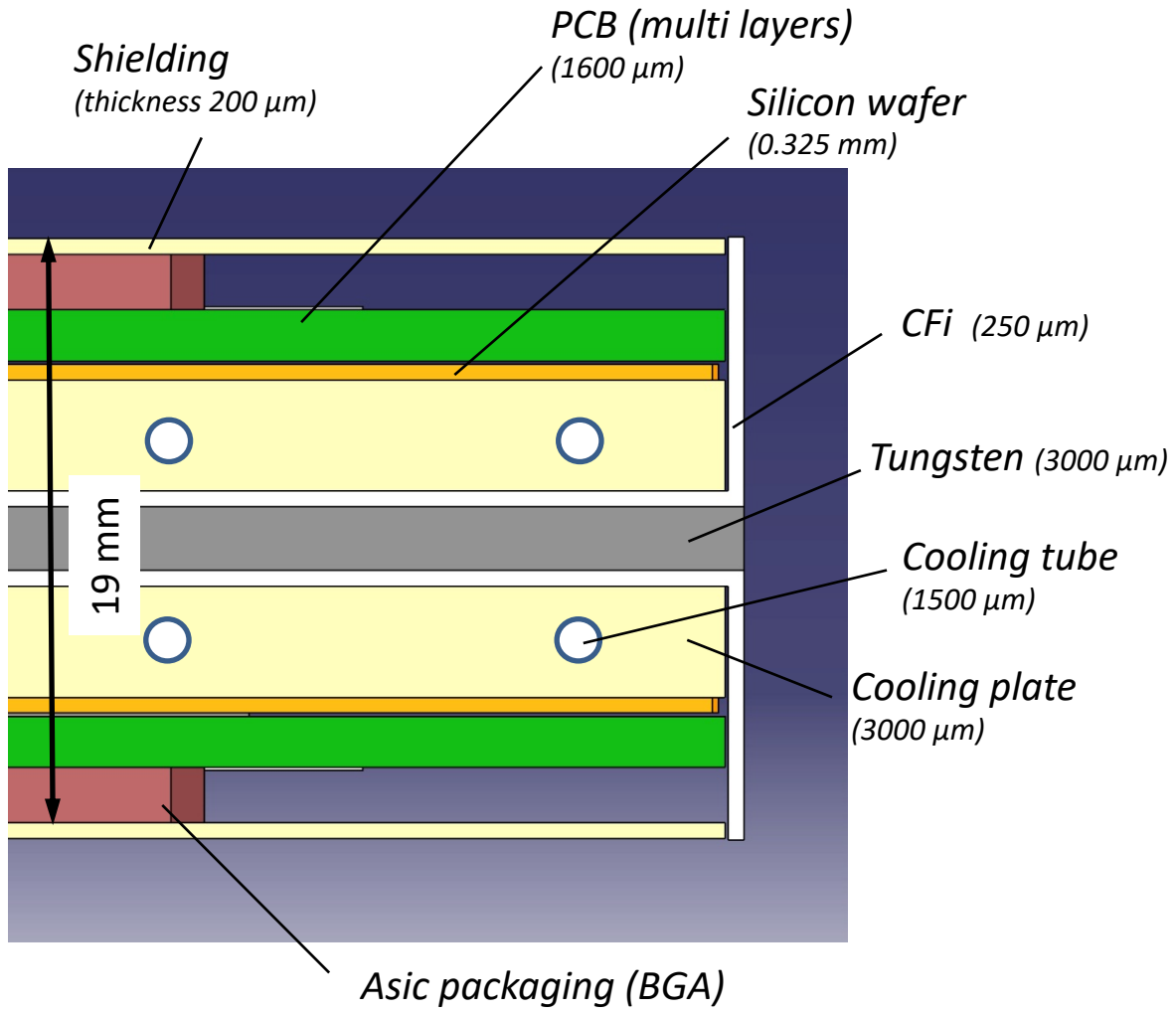
- The need for active cooling in the read-out gap needs to be evaluated
- most likely some cooling will be needed, and this will require some re-optimisation of the sampling structure
- the data rates are much higher than at the ILC, so bandwidth needs must be re-evaluated
- a realistic specification on powering and cooling requirements at the concentrator level need to be formulated
- the impact on services for powering and cooling in the gap and at the concentrator level needs to be estimated

The role of the calorimeter in the trigger needs to be discussed, and implications on electronics (and powering) be studied.

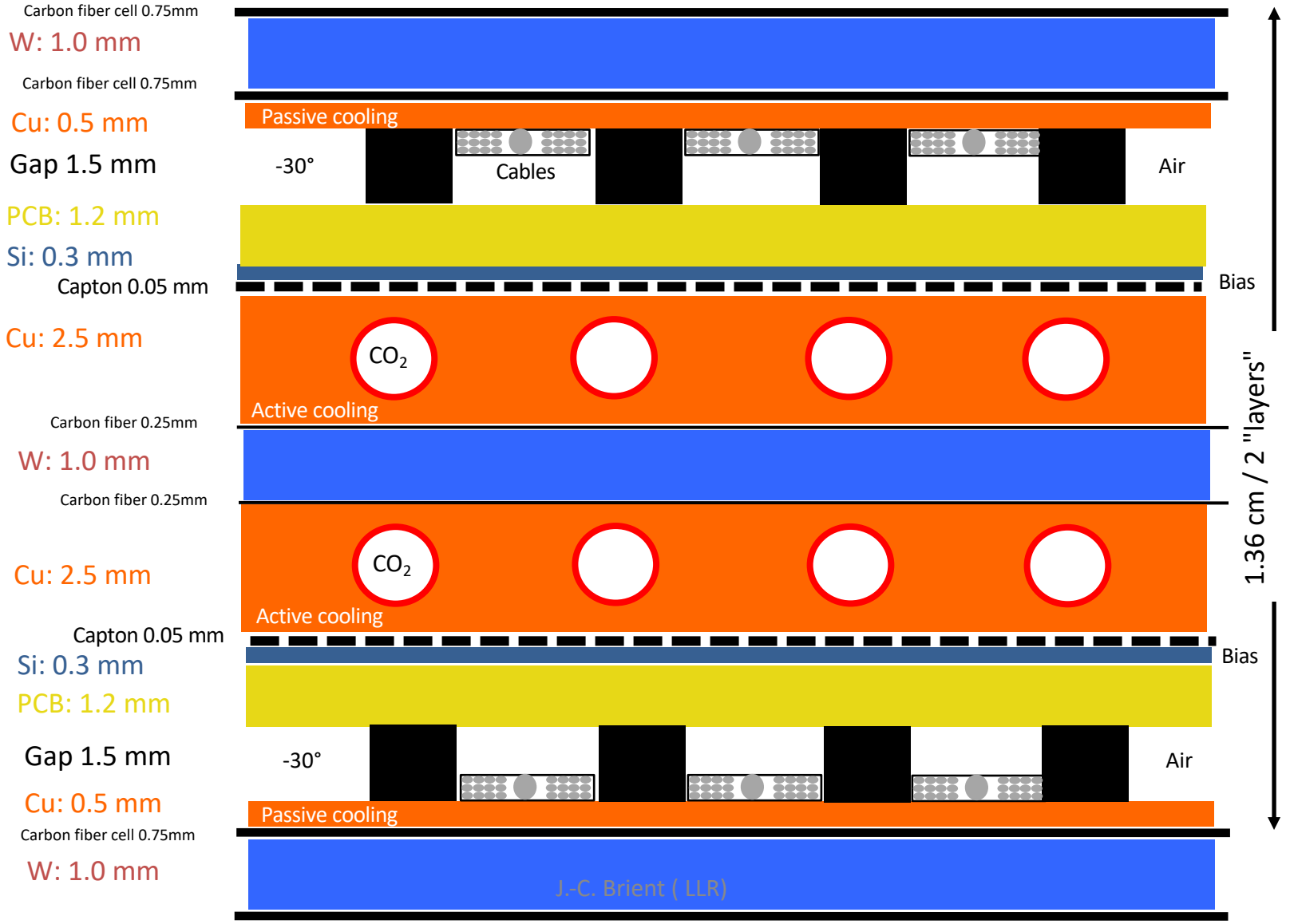
Possible cross section of the ECAL with active cooling (based on CMS study for HGCAL)

About 8.7 mm/layer

R_M^{eff}= 2.4 cm(2cm in CALICE-ILD)
Total thickness for 23 X0, 30 layers is 26 cm.



Front of ECAL – Shower start



COMMENT

Example R&D engineering on the cooling for a circular accelerator

This ECAL for CIRCULAR ACCELERATOR

But which level of granularity can be afforded without powerpulsing ?

- For physics, the smaller is the best (it continue to improve largely even for S_{Pixel}<<Rm)
  BUT for the electronics cost and cooling , … there is some limits

- Readout every 25 ns; no power pulsing
  readout frequency versus ILC x **14** (350 ns to 25 ns)
  conso/cell = 2.8 mW (Analogic part SKIROC2 without PP) +
  2,1 mW (=0,15 x**14** for digital part with readout every 25ns)

  = 5mW …. Propose to use 10 mW/channel (including a safety factor of 2)

- From CMS upgrade project-**HGCAL** , active cooling system can be stabilized in temperature
  for about 100W/layer, with fluid running in tube inside cooper plate (Rm not so good than ILC… but)

Taking into account the choosen layer size (= 150x20 cm²) and the 100W/layer (given by CMS engineers)
The cooling can afford pixel size of about 0.6x0.6 cm² !!! We have it

COMMENT

Donc, partons de l'hypothèse
que c'est bien un calo optimisant les performances PFA
C'est à dire un calo ultragranulaire : **CONSEQUENCES**

a) Calibration of O(100) millions channels and signal stability (we want same response for same collision)

b) Capability to make zero suppress "on site" (we don't want to read empty pixel)

c) Keep S/N ≥ 10 at MIP level and coherent noise under control (noise , radio/TV , telephone, ground loop, etc…)

d) Multiplexing for the quantity of signal line out (we don't want to have 100M cables)

e) Power management due to large number of channels (we don't want to burn our electronics readout)

f) KEEP the COST UNDER CONTROL (we want an affordable cost)

A set of answers to be verified by demonstrator

a) Choose stable device (silicon) or control & monitor the signal stability (Scintillator)

b) ADC& digital memory in readout chip, close to active layer. Read memories at each end of bunch train

c) i.e. Silicon PIN diodes …. AC/DC coupling , ground loop …

d) Large number of Channels/VFE ASIC… (KPIX, SKIROC), but only few readout line

e) Power pulsing (thanks to machine structure) → reduced the power to dissipate… no cooling inside

f) Reduce the overall surface or use lower cost active device (scintillator)

BUT warning versus point a) and c) . 10 years contacts with producers, defining wafers design which reduce the cost

Scintillator or silicon ?

- Stability
- Capability to go down to 0.5x0.5 cm²
- Good S/N at MIP level
- VERY good uniformity (guarding vs uniformity in strip or tile)
- Cost …

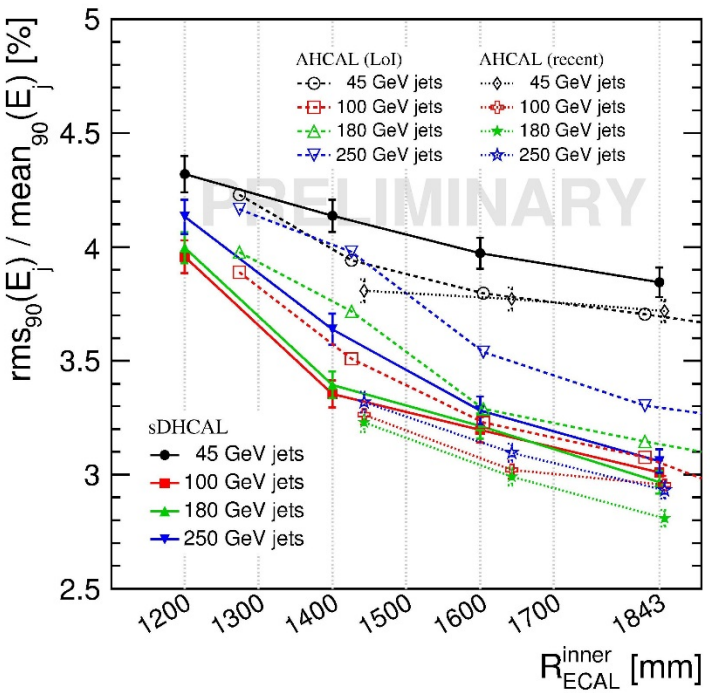
Today price is about **2.0-3.0 €/cm²** for silicon PIN diodes
If you include the scintillator, fibers, monitoring system and SiPM the price is marginally different from silicon PIN

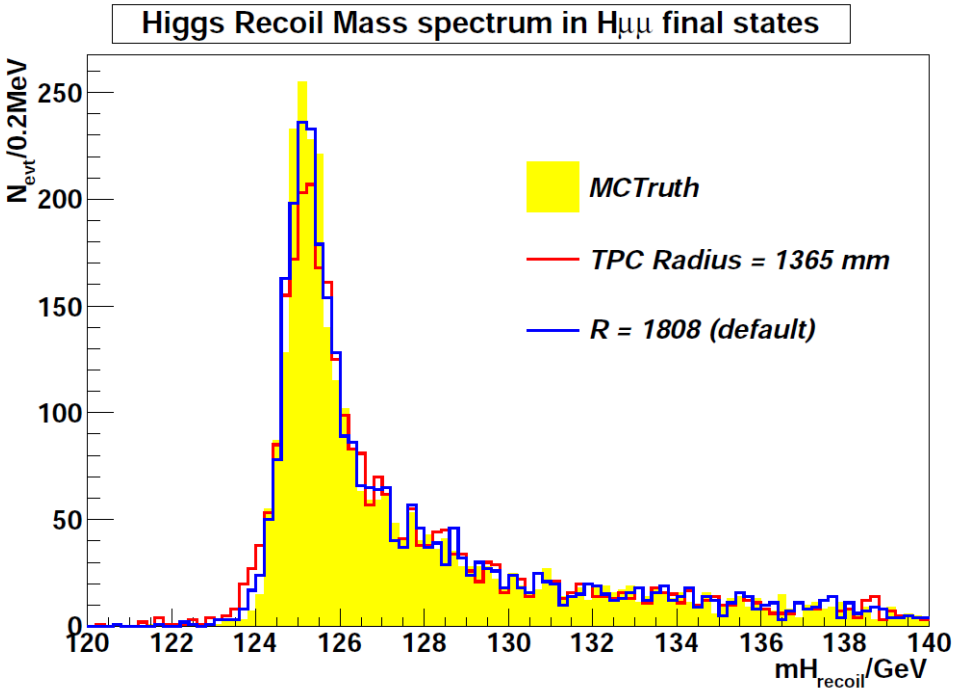
HOWEVER, about the overall detector cost
It depends of the ECAL barrel radius and length.
For the same physics(jet, tau, etc..) performances, a smaller detector with smaller pixel could do the job

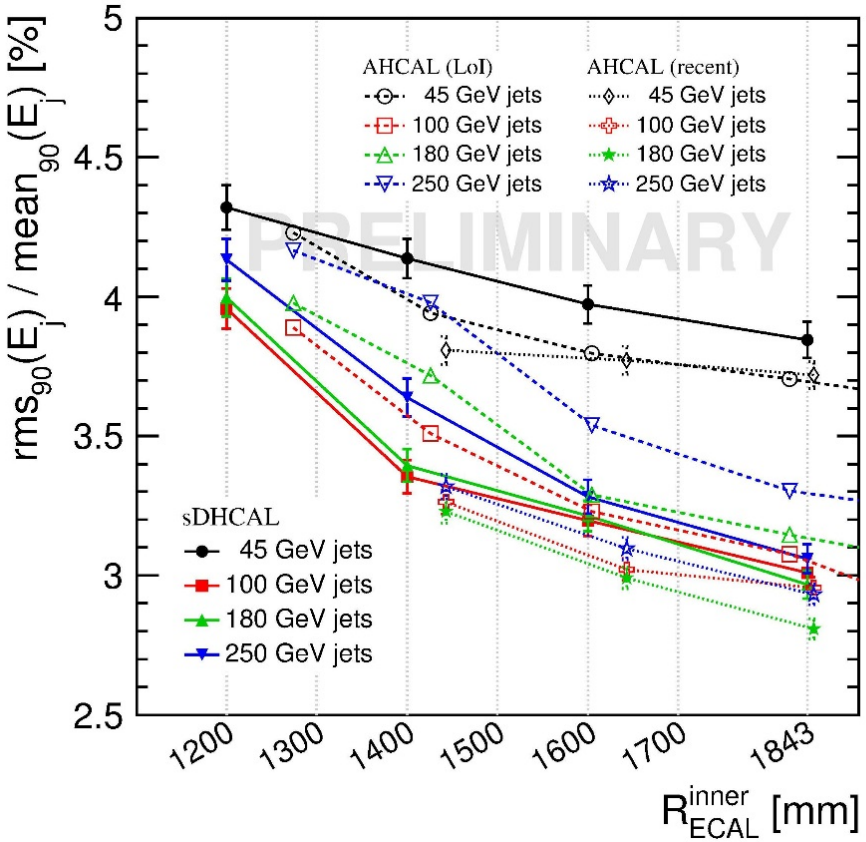
Smaller detector ⇒
smaller cavern, smaller Yoke, smaller return yoke, etc… **COST !!**

CONCLUSION

Small pixels, small radius
OR
Larger pixels (scintillator), larger radius
…
SID , ILD ===== same detector cost




Higgs Recoil Mass spectrum in Hμμ final states
N_evt/0.2MeV
MCTruth
TPC Radius = 1365 mm
R = 1808 (default)
mH_recoil/GeV


rms90(Ej) / mean90(Ej) [%]
AHCAL (LoI)
AHCAL (recent)
45 GeV jets
100 GeV jets
180 GeV jets
250 GeV jets
PRELIMINARY
sDHCAL
R_ECAL^inner [mm]

Detector SLAB (exploded view)