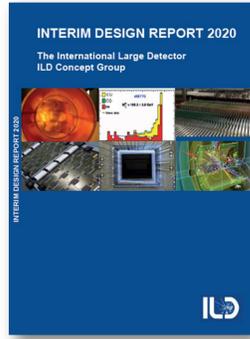


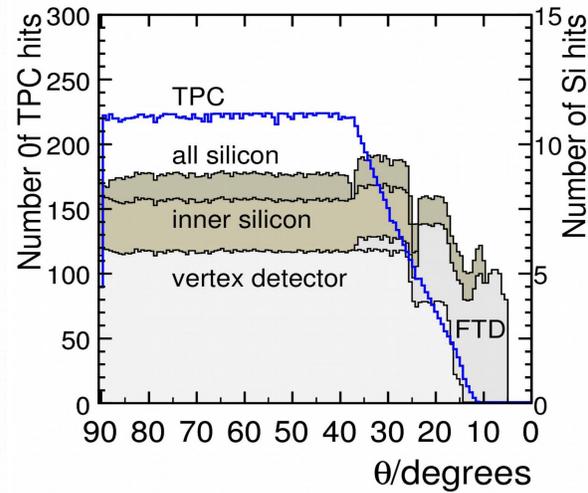
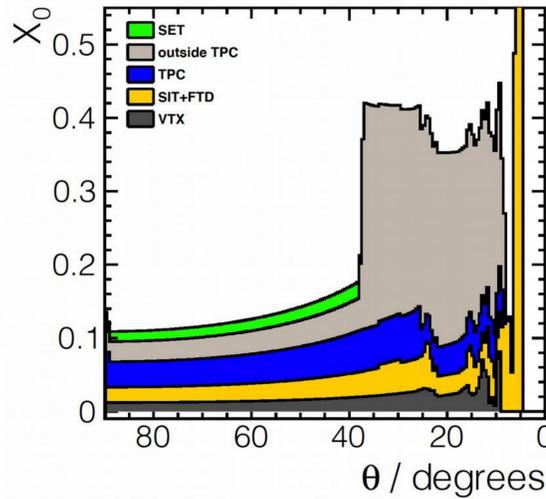
Paul Colas and Maxim Titov, CEA Saclay, Irfu, France (on behalf of the ILD tracking groups)

ILD (Silicon + Gas) Tracking Concept:

- **Vertex: Barrel of 3 double layers of Si-pixels** (e.g. CMOS MAPS, DEPFET, CCD, Sol, ...)
0.3% X₀ / layer, $\sigma_{sp} \lesssim 3 \mu\text{m}$
- **Intermediate Si-tracker (SIT, SET, FTD)**
 - SIT/FTD: silicon pixel sensors (e.g. CMOS)
 - SET: silicon strip sensors
- **Time Projection Chamber with MPGDs**
 - High hit redundancy (200 hits / track)
 - 3D tracking / pattern recognition;
 - dE/dx (dN/dx) information for PID



Most recent paper on ILD: ILD interim design report arXiv: 2003.01116



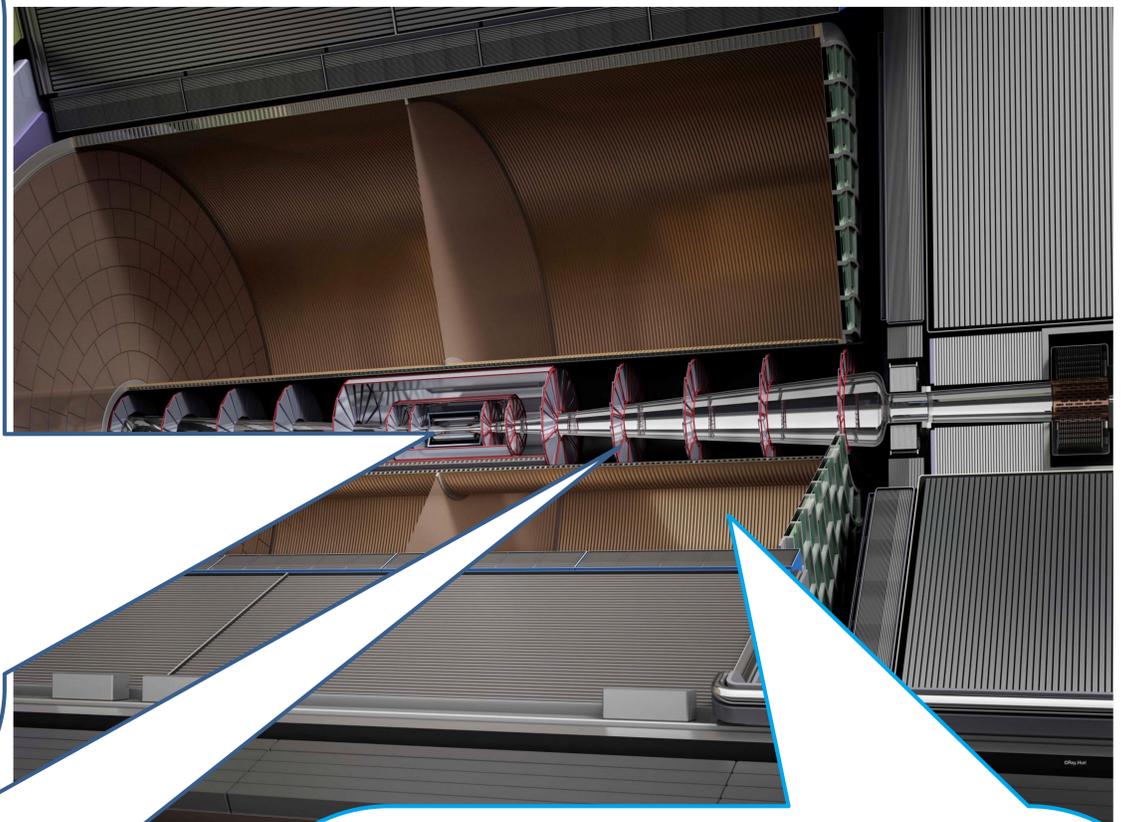
ILD Vertex Technologies:

- Exploiting the ILC low duty cycle 0(10⁻³): triggerless readout, power-pulsing
- **Readout strategies:**
 - continuous during the train with power cycling → mechanic. stress from Lorentz forces in B-field
 - delayed after the train → either ~5μm pitch for occupancy or in-pixel time-stamping

Physics driven requirements	Running constraints	Sensor specifications
$\sigma_{sp} \sim 2.8 \mu\text{m}$	→ Air cooling	Small pixel $\sim 16 \mu\text{m}$
Material budget $0.15\% X_0/\text{layer}$	→ beam-related background	Thinning to $50 \mu\text{m}$
r of Inner most layer 16mm	→ radiation damage	low power $50 \text{ mW}/\text{cm}^2$
		fast readout $\sim 1 \mu\text{s}$
		radiation tolerance $\leq 3.4 \text{ Mrad}/\text{year}$
		$\leq 6.2 \times 10^{12} n_{eq}/(\text{cm}^2 \text{ year})$

Technology	FPCCD	DEPFET	SOI	CMOS	ILGAD
Added value (example)	Very granular	Low material budget	2 tier process (high density μcircuits)	Industry evolution	PID

CMOS (CPS): continuous readout, stitching (STAR)
 DEPFET: continuous readout, 75 / 50 μm thick (Belle II)
 Fine pixel CCD: delayed readout, 5 μm pitch, 50 μm thickness
 SOI: delayed / continuous readout, suited for 3D integration
 Sol-based 3D integration: rely on high-density in-pixel circuitry, with double-tier "3D" in CMOS TJ 180nm process



Examples of recent CMOS – MAPS developments:

	ULTIMATE	ALPIDE	MIMOSIS	PSIRA proposal
Data taking	2014-2016	>2021-2022	>2021	>2030
Technology	AMS-opto 0.35 μm	→ 0.18 μm	0.18 μm	0.18 μm (conservative) < 0.18 μm ?
Architecture	4M	HR, V _{DD} ~6V Deep P-well	HR, Deep P-well	Asynchronous r.o. In pixel disci.
Pitch (μm ²) / Sp. Res.	20.7 x 20.7 / 3.7	27 x 29 / 5	22 x 33 / <5	~ 22 / ~ 4
Time resolution (μs)	~185	→ 5-10	5	1-4
Data Flow		~10 ¹² part/cm ² /s Peak data rate ~ 0.9 Gbits/s	peak hit rate 7 x 10 ¹¹ /mm ² /s → 6 Gbits/s output (20 inside chip)	~375 Gbits/s (instantaneous) ~1.6 Gbits/s (average)
Radiation	O(50 krad)/year	2x10 ¹² n _{eq} /cm ² 300 kRad	3x10 ¹¹ n _{eq} /cm ² /yr & 3 MRad/yr	O(100 krad)/year & O(1x10 ¹¹ n _{eq} (1MeV)/yr
Power (mW/cm ²)	< 150 mW/cm ²	→ < 35 mW/cm ²	< 200 mW/cm ²	~ 50-100 mW/cm ² + Power Pulsing
Surface	2 layers, 400 sensors, 360x10 ³ pixels, 0.15 m ²	→ 7 layers, 25x10 ³ sensors	4 stations Fixed target	3 double layers 10 ³ sensors (4cm ²) 10 ³ pixels ~0.33 m ²
Mat. Budget	~ 0.39 % X ₀ (1st layer)	→ 0.3% X ₀ / layer		~ 0.15-0.2 % X ₀ / layer
Remarks	1 st CPS in colliding exp.	(with CERN)	Vacuum operation Elastic buffer	Evolving requirements

ALICE-ITS3 upgrade drives important R&Ds:

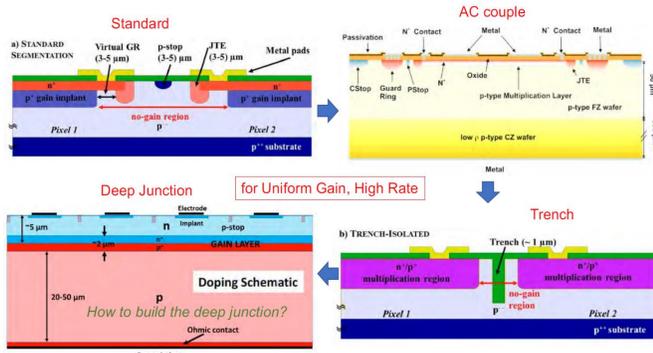
- ✓ Bending thin (50 μm) Si-layers (MAPS): truly cylindrical, supportless CPS (65 nm)
- ✓ Industrial stitching & large surfaces for low-mass detectors

Intermediate Silicon Tracker:

Baseline solution: **silicon-microstrip tracker**; also some enabling technologies (e.g. based on LGAD concept)

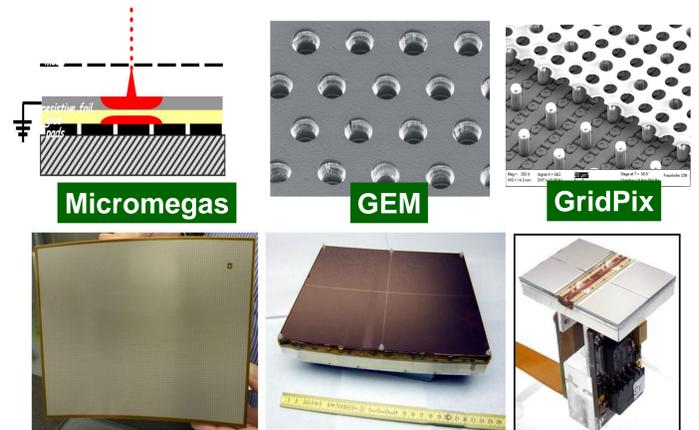
Timing Detectors open up 4D (and 5D) tracking:

- ✓ High-precision tracking → a few μm per layer
- ✓ High-precision timing → tens of ps per layer
- ✓ Optimal geometrical acc. (large fill-factor).
- ✓ Low material (50 μm thickness per plane).

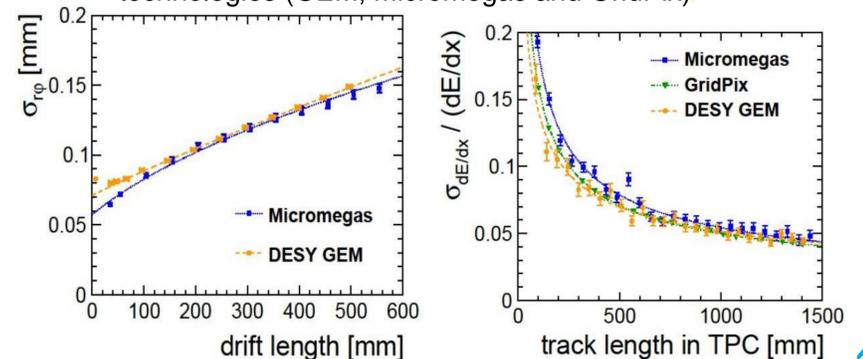


TPC (10 m² endcaps) with MPGD Readout: Ionization for PID and continuous tracking

Baseline technologies: GEMs, Micromegas, GridPix



Target requirement of a spatial resolution of 100 μm in transverse plane and dE/dx resolution < 5% have been reached with all technologies (GEM, Micromegas and GridPix)



STRATEGICAL ISSUES related to adaptation of ILD to other colliders than ILC. Work plan:

- ✓ Optimize acceptance in the forward region, taking into account specific background conditions
- ✓ Bunch and train time structure : revise power management and heat removal to adapt to almost continuous beams
- ✓ Explore how an ILD-like TPC can perform under these high-ionization and high space charge conditions.
- ✓ Adapt calibration and alignment strategies to these conditions