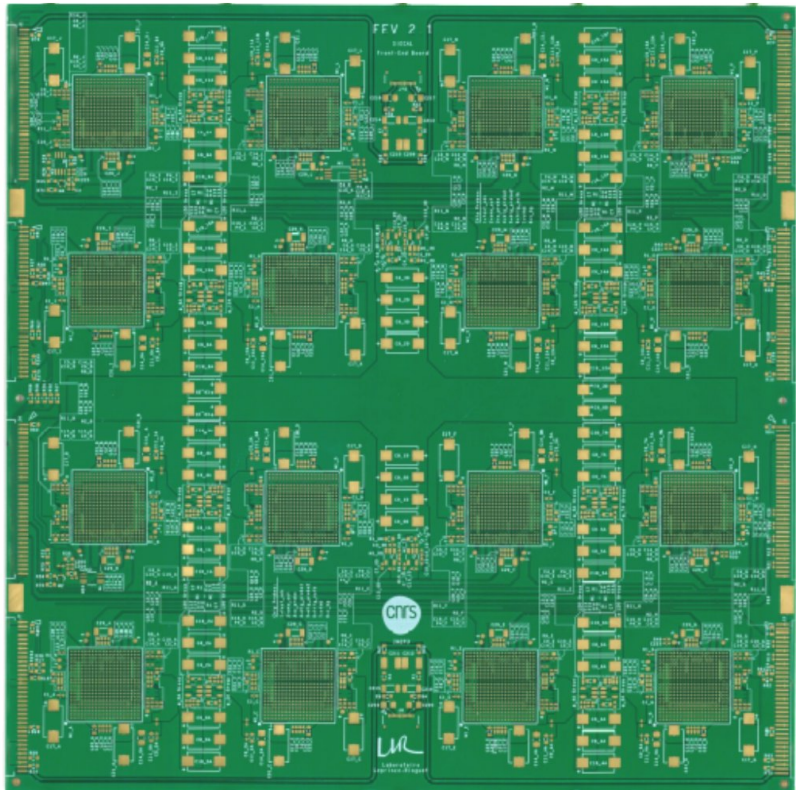
The FEV2.1 and a first glimpse at SK2a full batch testing

V. Boudry, S. Callier, M. Louzir, J. Nanni*

Institut Polytechnique de Paris

CALICE meeting
29/03/2023, Göttingen

New FEV2.1 (ultimate version)



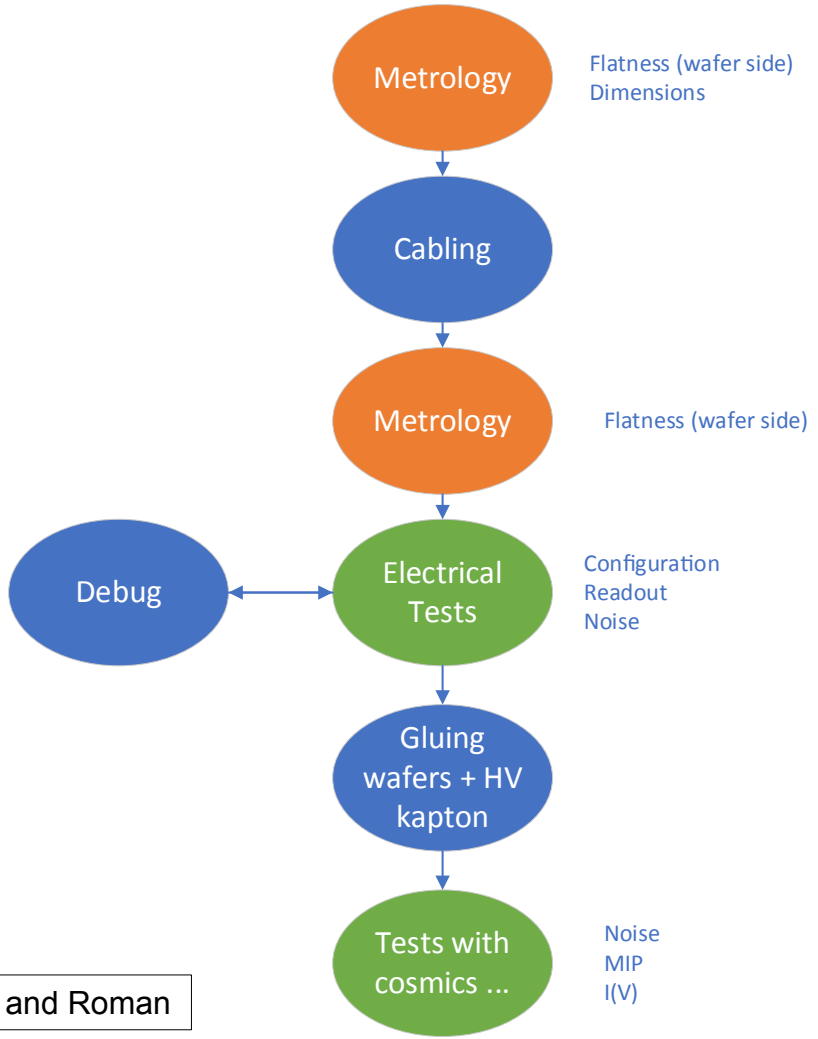
- Add identification component:
  - BQ2023: unique ID, measure current & voltage
- New production CSI company
  - Respect flatness recommendation (<150µm)
  - To confirm with our method
- Before cabling all SKIROC 2A chips are fully tested with Omega software
  - 3 validation levels: OK, OK without minor defaults, KO

J. Nanni, M. Louzir, R. Guillaumat, D. Breton, J. Jeglot, S. Callier, ...

Assembly process

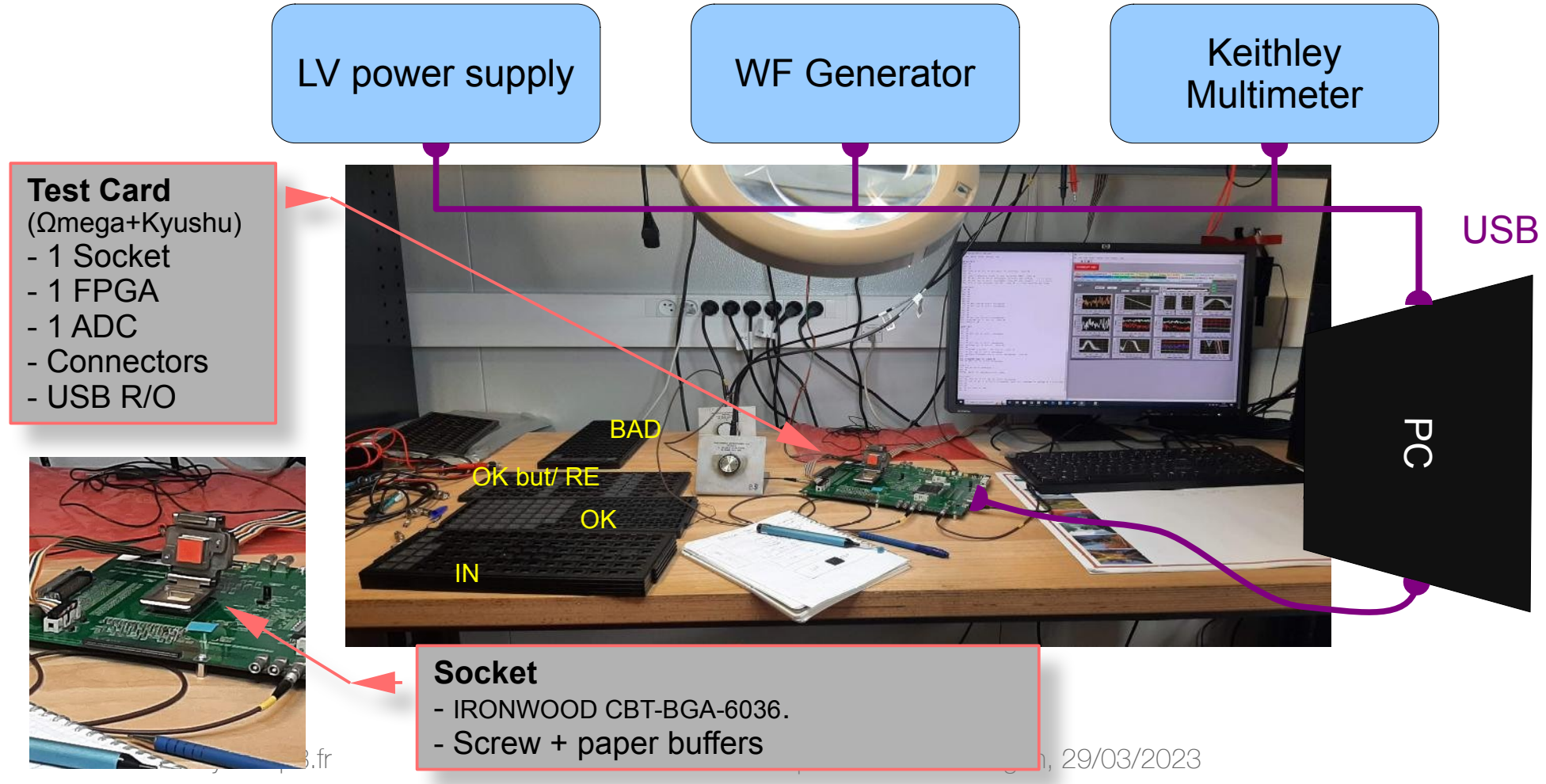
- First batch of 4 boards for electrical test and debug
- Start assembly process of 10 boards with caution:
  - Use gloves
  - Clean board surface before gluing wafers (cold plasma)
  - Store boards in dry cabinet

→ GOAL: LONG SLAB of 8 boards fully equipped of wafers before end of 2023

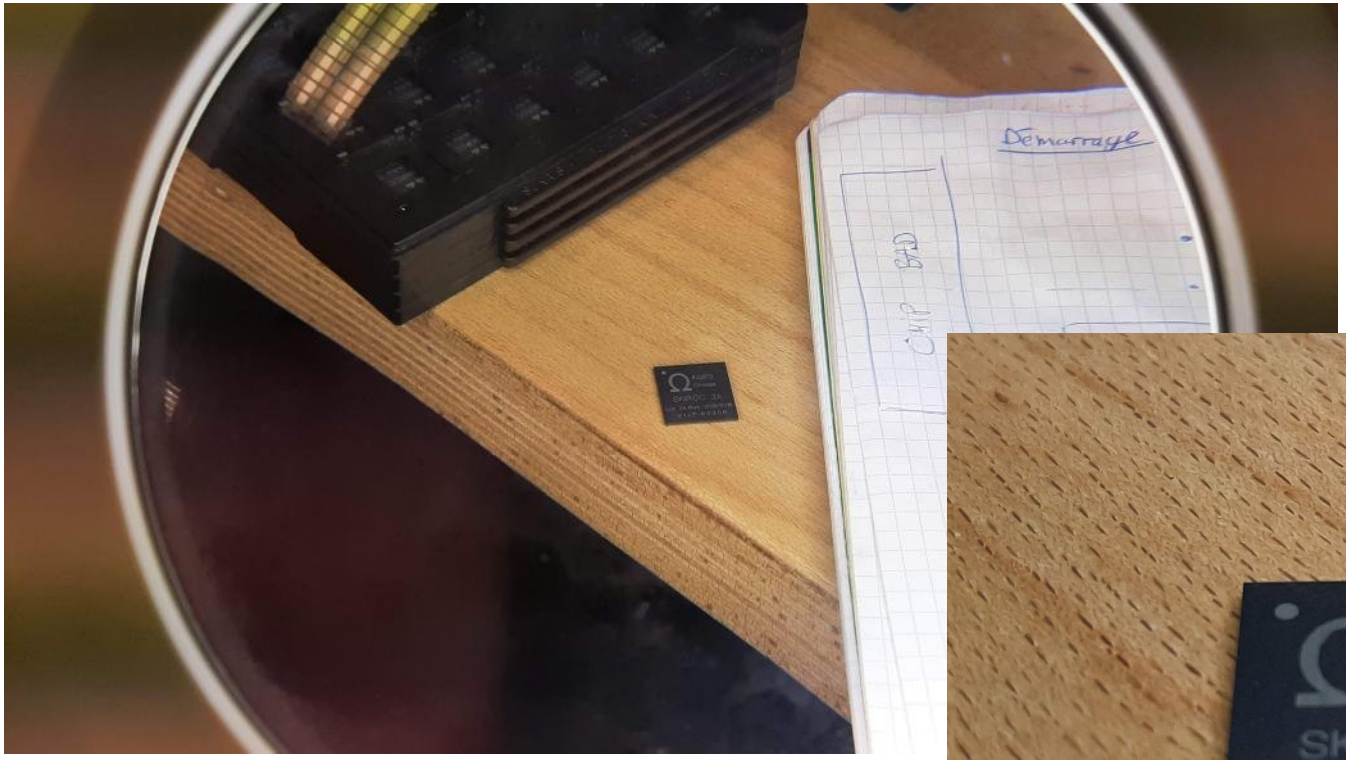


More details in pres of Adrián and Roman

SKIROC2 test bench at Ωmega



NCAP packaging



- 460 pieces; 400 remaining
- Thinner
- Labelled

Measurements

LabView testing SW : Digital & Analogue probing 9 mins per ASIC (optim) © S. Callier

Powering

Fine Thr Adjust /ch

VDC Pre-Amp /ch

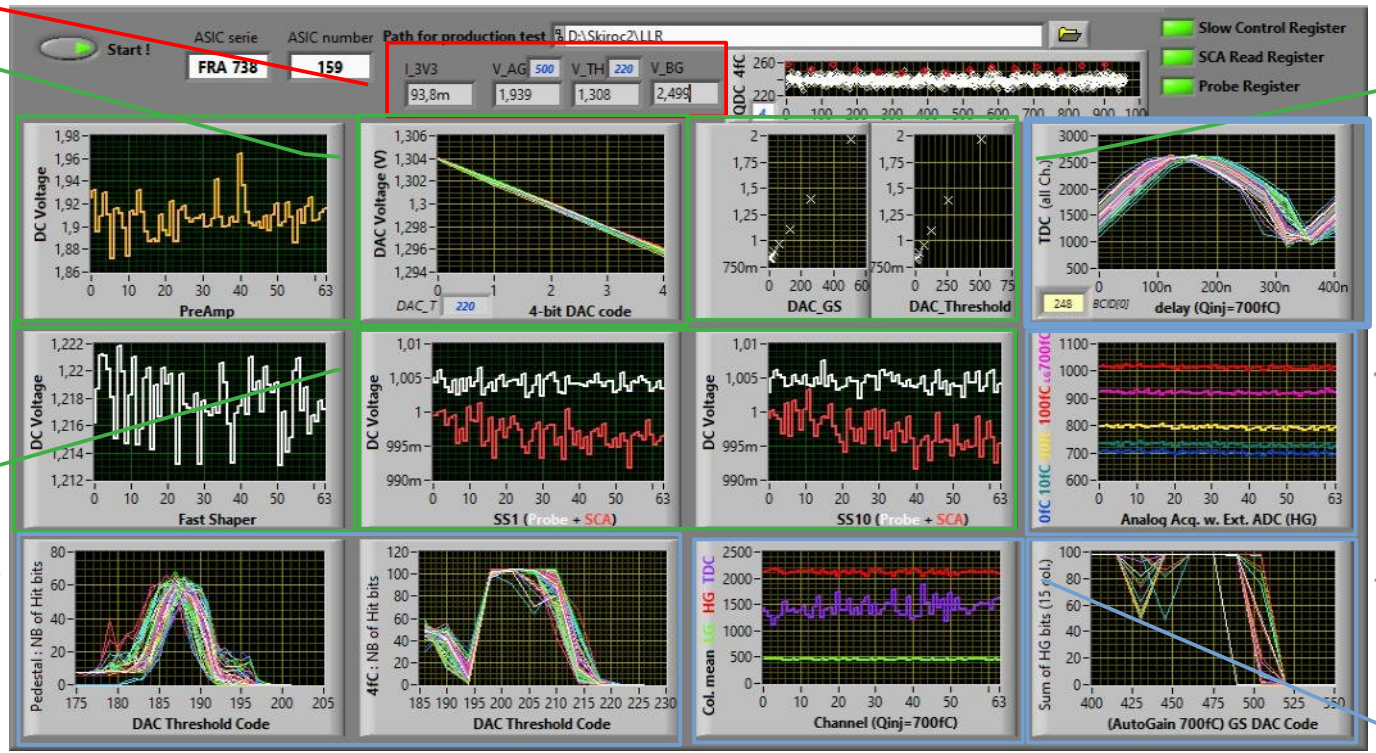
VDC Fast Shaper /ch

VDC Slow-Shaper /ch

- G1, G10
- Probe & SCA

DAC Thr scan / ch

- Pedestal
- MIP (4fC)



DAC Scan with probe:

- auto-gain (GS)
- Global Thr.

TDC Delay scan /ch

Analog Readout/ch

AutoTrigger delayed by FPGA

- HG : 0, 10, 30, 100 fC
- LG: 700 fC

AutoGain efficiency

(SCA 0–14) Qinj = 700fC

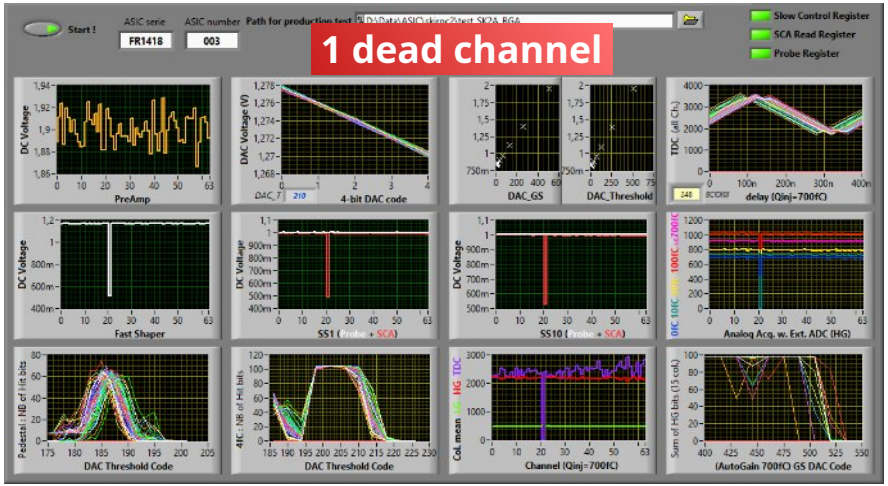
Eff. per Ch. vs Gain code

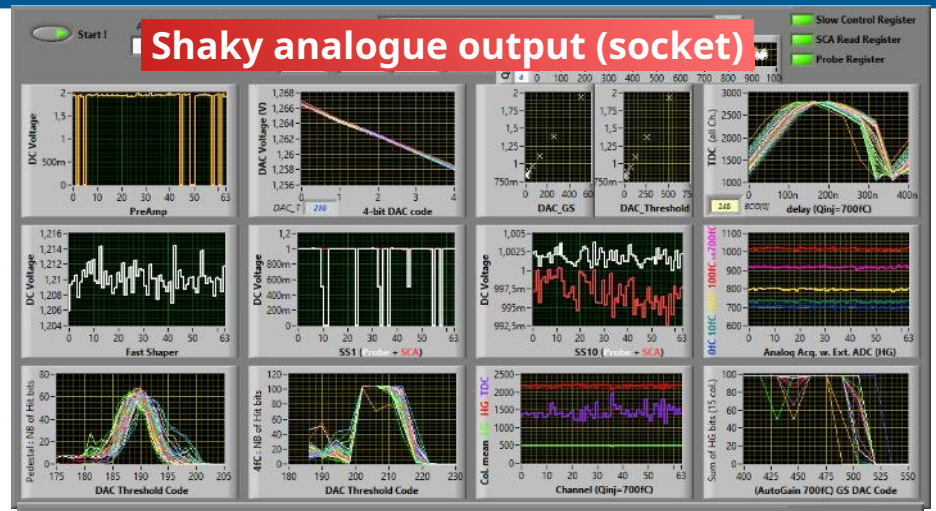
ADC ⟨SCA0–14⟩/ch

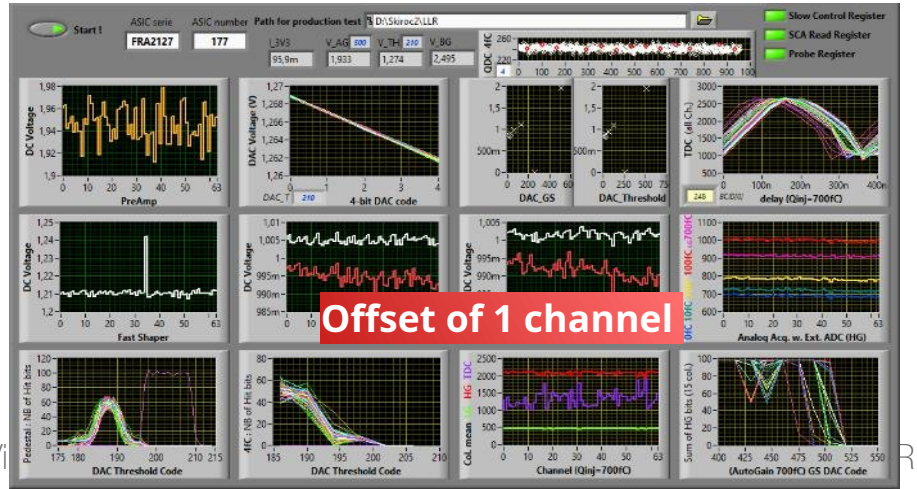
Qinj = 700fC

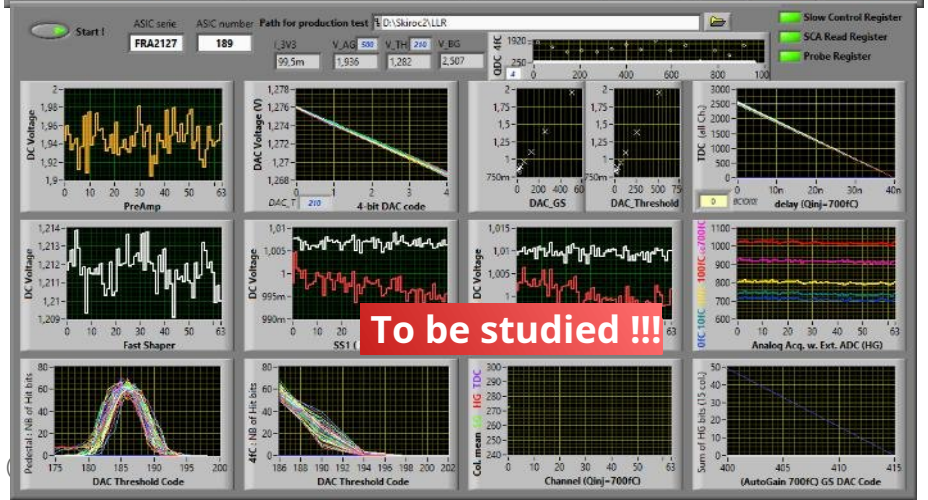
- HG, LG, TDC(SCA0)

Examples of errors









Novapac

46 chips tested

	Data	
Statut	Count - Statut	Count - Statut
BAD	8	17 %
OK	35	76 %
OK but	3	7 %
Total Result	**46**	**100 %**

Count - Rems	Statut			
Remarks	BAD	OK	OK but	**Total Result**
1 channel 60 (61e) with abnormal pedestal		1		**1**
Noisy (ERREUR alim 6.3V et -7V off)			2	**2**
Thr DAC not working	1			**1**
fine scan of DAC_GS not working		1		**1**
multi problems	2			**2**
no digital data (ADC); 23e voie off	1			**1**
No probe register V_BG = 1.873; I_3V3 = 695m !!!	1			**1**
pb preamp	2			**2**
pb probes; internals OK			1	**1**
pbm de probe reg. court circuit FS ? Conso 160mA; pbm SCA 8 ?	1			**1**
(empty)				
Total Result	**8**	**2**	**3**	**13**

400 ASICs

- 105 tested

	Data	
Statut	Count - Statut	Count - Statut
BAD	3	3 %
OK	85	81 %
OK but	11	10 %
RE	6	6 %
Total Result	**105**	**100 %**

Count - Rems	Statut			
Rems	BAD	OK	OK but	RE
8mA de consommation		1		
Multiple problems; a étudier		1		
issue with DAC_GS ?			1	
Noisy (alim OFF so… normal) --> A re tester				4
low pedestal (~176)			1	
No analogue output		10		
OK mais pas de sortie analogique (alim OFF donc normal) --> A re tester				2
No digital output		1		
pas de TDC ni de sortie analogique (peut être problème de cablage de l'injection)			1	
problème injection + TDC voie 29			1	
problem ch 41			1	
problem ch 62			1	
problem ch 49			1	
quelques étrangeté sur la sortie analogique		1		
voie 12 plus bruyante (thr+20); Faire vérifier par Steph			1	
voie 36 avec un offset de 30mV à corriger avec le DAC 4bits		1		
voie 36 pb SS1; no auto gain; no injection			1	
voie 47 mauvaise valeur LG avec injection 700fC			1	
voie 6 pb shaper			1	
(empty)				
Total Result	**3**	**12**	**11**	**6**

Conclusions

FEV2.1 PCBs ready for measures (then cabling)

- All component for cabling now available

ASIC testing :

- **Previously** : only basic configuration and simple readout test were performed, WITHOUT any quality check ~ response to DAQ ✓
- **Now**: Quality control is performed on all stages for all channels ! Even on non used stages for analogue readout. We are ensuring that the response of each channel is identical.
- 1st learning phase
  - Socket: Mechanically hard to handle

SKIROC2a 1st Analogue Batch Tests : ~ 1/3 of available stock (~450).

- 2 packaging
  - NOVAPAC: 75% GOOD, but 15% BAD. Includes some already tested (only on config-data)
  - NPAC: 80% GOOD, but 3% BAD, some specific dysfunctions
    - Most errors affect only single channels
- Preliminary STAT, **worse** than reality.
  - standard settings ➡ adjusments (e.g. thr.) possible
  - “OKbut” ASICs will be retested with tuned settings
  - requires better classification

Full Analysis (started)

Data has been recorded

- text format
- Example of paaremeters to be extracted

Granularity	Parameters	Rem
Set of ASIC's		
ASIC-wise	Temperature	optimal stabilisation time to be measured
	Power ×2 (VDD, VDD_PA)	V*I during measurement
	LG ADC Ped, σ	
	HG ADC pedestal, σ	
	⟨Ped⟩_thr, ⟨sigma⟩_thr	from channels
Channel-wise	Low Gain ADC Ped, Sigma	From non-triggered channels, from external triggers ?
	High Gain ADC Ped, Sigma	From non-triggered channels, from external triggers ?
	Trigger Ped, sigma adcc, σ	From S-Curve : single or two-sided ?
	Relative LG ADC linearity (adcc, σ vs Ampl)*n	From charge injection
	Relative HG ADC linearity (adcc, σ vs Ampl)*n	From charge injection
	TDC linearity (adcc, σ vs ns)*n	From charge injection ≠ Amplitudes ?
	Low Gain Mip response (adcc)	From Sensors
	High Gain Mip response (adcc)	From Sensors
	Threshold linearity (adcc vs DAC)	Threshold scan