Commissioning and noise study of the ultra-thin chip-on-board PCB for the CALICE SiW-ECAL prototype

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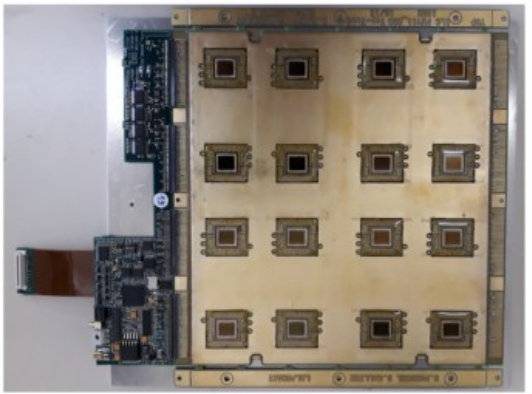
- In recent years the SiW ECAL has developed and used several PCB variants
  - To make sure that you don't get lost, here comes an introduction

FEV10-12

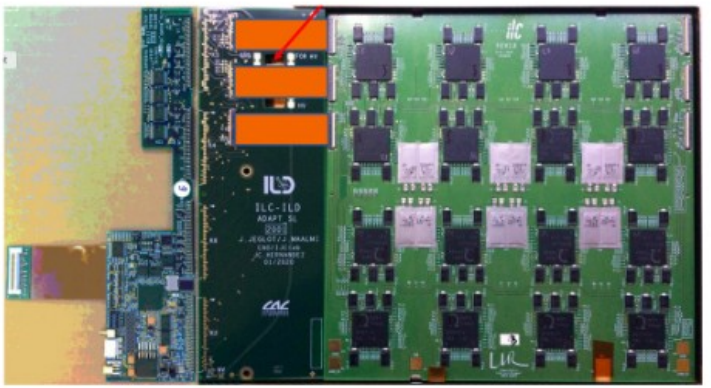
- ASICs in BGA Package
- Incremental modifications From v10 -> v12
- Main "Working horses" since 2014

FEV_COB



- ASICs wirebonded in cavities
  - COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

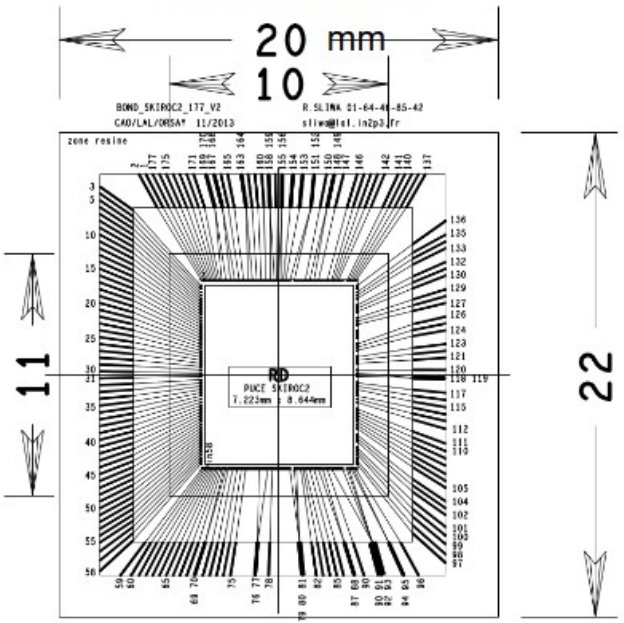
FEV13



- Also based on BGA packaging
- Different routing than FEV10-12
- Different external connectivity

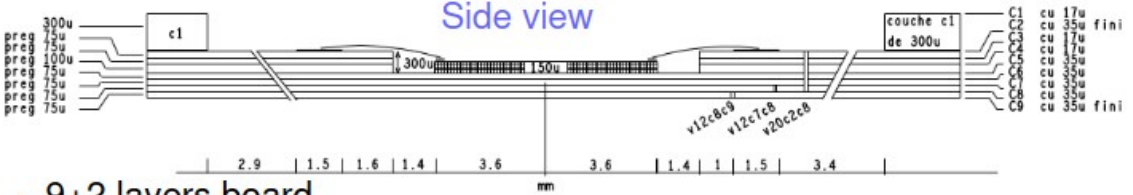
Current prototype (see later) is equipped with all of these PCBs

Bonding scheme

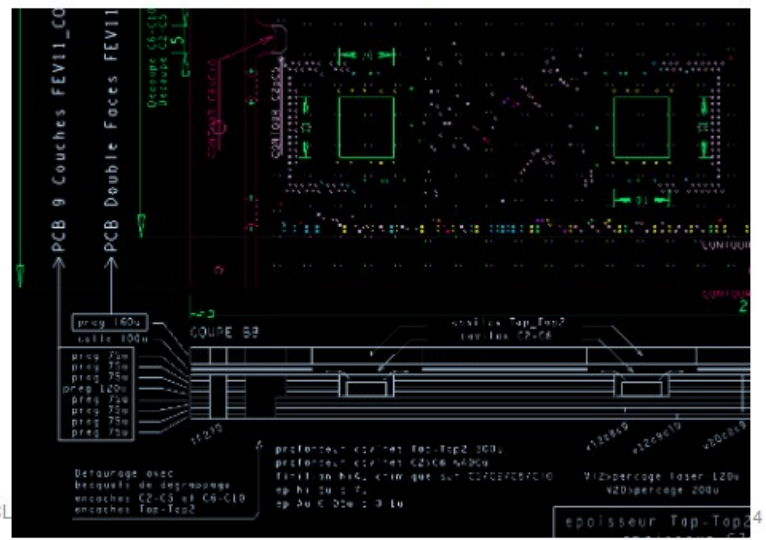


- ~177 Bonding wires
- Bonding by CERN Bondlab
- Regular exchange allowed to iron out early shortcomings

Side view



- 9+2 layers board
- Overall height ~1.2mm
- ASICs buried in cavities to ensure overall flatness
  - Need to make sure that bonding wires don't pass board surface



- More info in https://agenda.linearcollider.org/event/9076/contributions/51356/attachments/38450/60438/SC_FEV11_COB_20221012.pdf

Today

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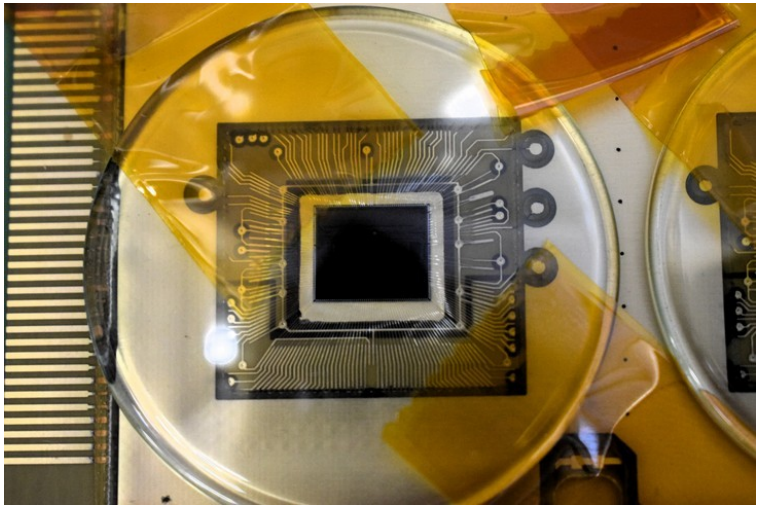
Abstract

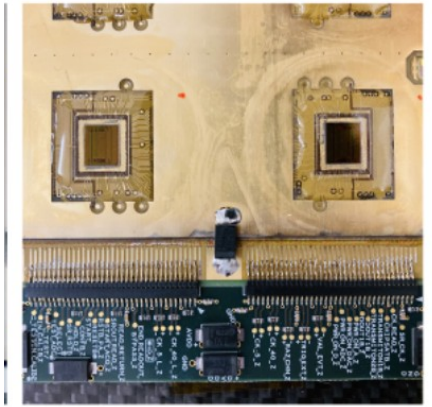
Most future high energy e^+e^- colliders, *a.k.a. Higgs Factories* proposals consider using high granular calorimeters in their detectors concepts. One of such high granular calorimeters proposals silicon-tungsten electromagnetic calorimeter (SiW-ECAL) designed and constructed by the CALICE Collaboration. Its key features are: unprecedented high granularity and compactness featuring very low power consumption. This document reports on the development of an alternative for the basic unit of detection (Active Signal Unit) of the SiW-ECAL. This alternative consists of an ultra-thin PCB called Chip-on-Board (COB) which is equipped with wirebonded ASICs and pixelated silicon wafers. These COB boards feature an unprecedented low thickness of 1.2 mm considering the internal complexity of the boards which allows a more compact design of the full calorimeter. This is to be compared with the 3-3.5 mm of the default solution variant using ASICs in BGA packaging. The design, production, equipment and test of such boards in beam tests (DESY, CERN) is reported in this document and compared with other PCB designs with less aggressive thickness requirements.

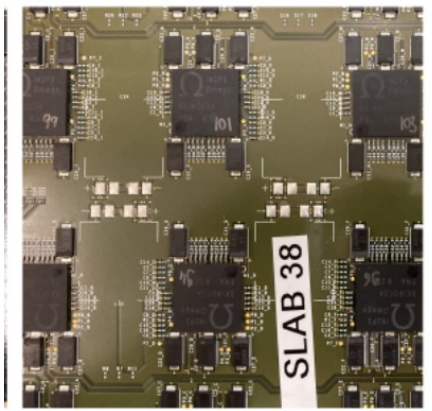
Keywords: Calorimeter methods, calorimeters, Si and pad detectors



- **Technical paper in preparation**
  - Analysis at MIP level
- Well advanced draft
- Using DESY 2022 and CERN 2022 data

Part of the FEV zoo at DESY and CERN





Part of the FEV zoo at DESY and CERN

- In this study, we only consider 6 FEVs (equipped all with 500um)

Pos.	Id	ASU type	An. PS. Dec.	Dig. PS. Dec.
5th	slab 38	FEV13	$(1nF \times 32)$ & $(10nF \times 32)$ & $(100nF \times 32)$ & $(1\mu F \times 32)$ & $(68\mu F \times 32)$ PA : $(1nF \times 32)$ & $(10nF \times 32)$ & $(100nF \times 32)$ & $(1\mu F \times 32)$ & $(120\mu F \times 32)$	$(100nF \times 33)$ & $(33\mu F \times 16)$
6th	slab 39	FEV13	$(1nF \times 32)$ & $(10nF \times 32)$ & $(100nF \times 32)$ & $(1\mu F \times 32)$ & $(68\mu F \times 32)$ $(PA$:$)(1nF \times 32)$ & $(10nF \times 32)$ & $(100nF \times 32)$ & $(1\mu F \times 32)$ & $(120\mu F \times 32)$	$(100nF \times 33)$ & $(33\mu F \times 16)$
7th	slab 29	COB	$(100nF \times 12)$ & $(150\mu F \times 2)$& $(330\mu F \times 5)$	$(100nF \times 14)$ & $(330\mu F \times 5)$
8th	slab 30	FEV12	$120\mu F \times 16$	$120\mu F \times 16$
9th	slab 33	COB	$(100nF \times 8)$ & $(150\mu F \times 2)$& $(330\mu F \times 5)$	$(100nF \times 8)$ & $(330\mu F \times 5)$
10th	slab 31	FEV12	$120\mu F \times 16$	$120\mu F \times 16$

Table 1: Summary of devices under study and their main properties. Column by column: Position in the 15 layer stack; ID; ASU type; amount of decoupling capacitors (with their value) for the Analogue Power Supplies and the Digital Power Supplies. Notice that for the FEV13, the preamplifier analogue power supplies (PA) are separated from the other analogue power suplies.

Commissioning: pedestal and noise

channel i is:

$$\sigma_i^2 = \sigma_{I_i}^2 + \sum_{j=1}^{N_c} \sigma_{C_i^j}^2 \quad (1)$$

The covariance matrix element from the two channels i and k is expressed by:

$$cov(i,k) = \delta_{ik}\sigma_{I_i}\sigma_{I_k} + \sum_{j=1}^{N_c} \sigma_{C_i^j}\sigma_{C_k^j} \quad (2)$$

where:

$$\delta_{ik} = \begin{cases} 1 & \text{if } i = k \\ 0 & \text{if } i \neq k \end{cases} \quad (3)$$

The covariance matrix element can also be determined from the data:

$$cov_{Data}(i,k) = \frac{\sum_{n=1}^{N_{event}} (A_i(n) - \mu_{A_i})(A_k(n) - \mu_{A_k})}{N_{event}} \quad (4)$$

Measured amplitude if no hit

Pedestal position → calculated as simple histogram Mean

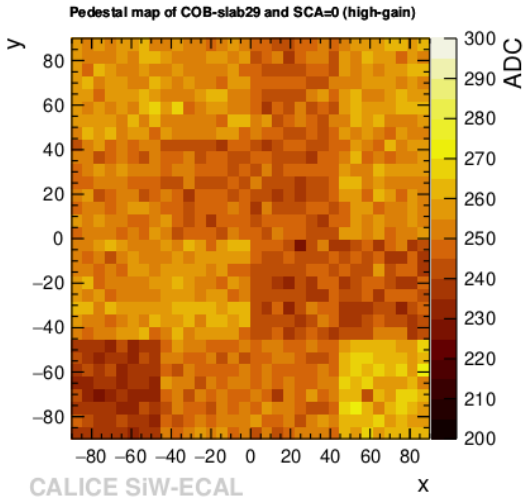
CALICE

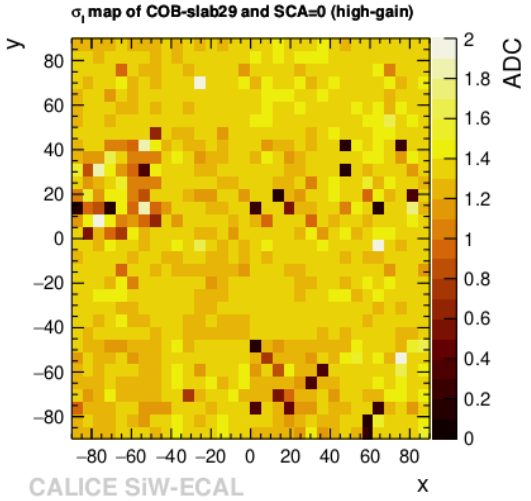
Commissioning: pedestal and noise

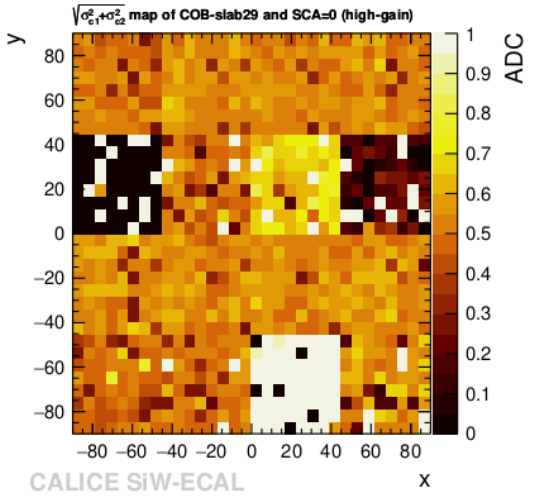
- For the calculation of the pedestal position for each readout channel and each SCA, the following procedure was followed (at DESY and CERN)
  - 1. Use the default trigger thresholds of ~ 0.5 MIP
  - 2. Mask all readout channels except channel 0
  - 3. Set-up the injection system to inject 15 signals of between 0.75-1.5 MIP 2 in channel 0. These signals were separated by 100μs each.
  - 4. Make sure that all ASICs from all modules in the stack were recording 15 injected signals.
  - 5. Record 10000 readout cycles of 2ms each.
  - 6. Repeat the process 3 times more but using channels 9, 18 or 27 instead of 0

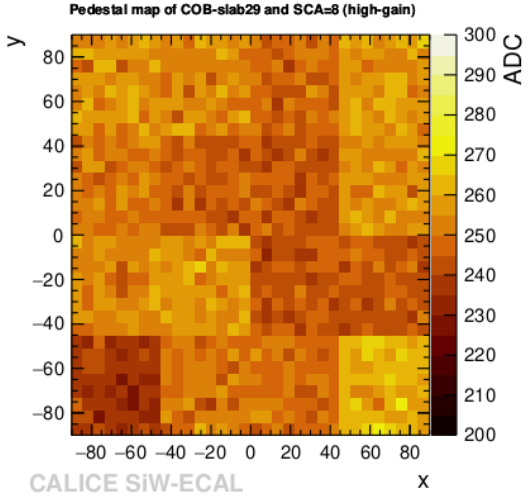
- **The analysis is done, chip-wise (treating all chips independently!)**

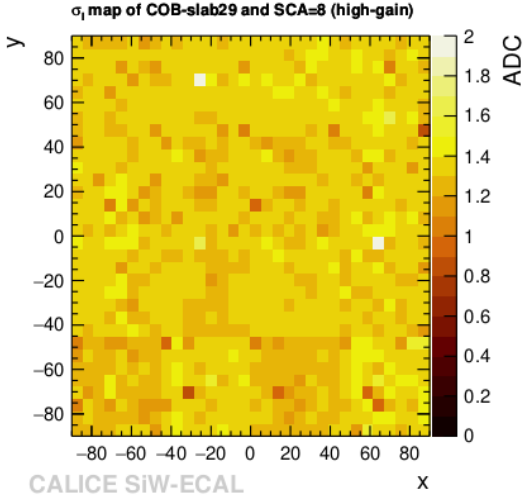
Pedestal and noise, COB -slab29

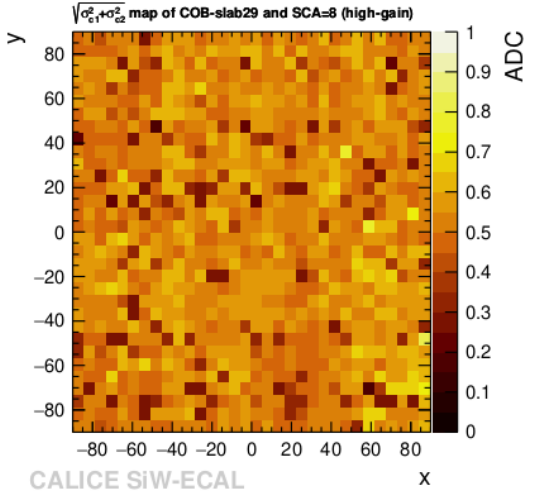




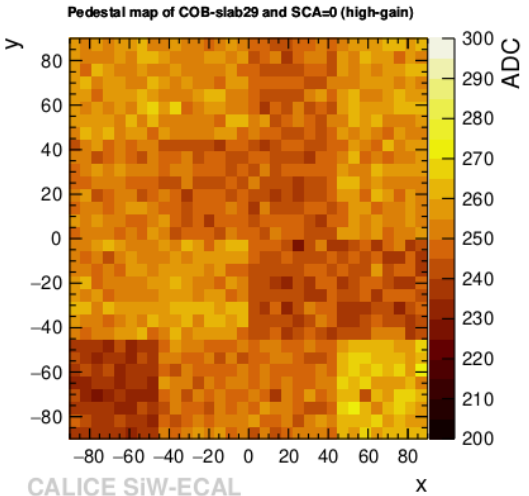


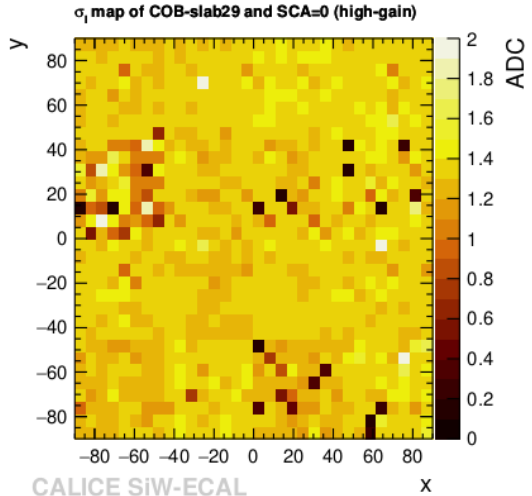


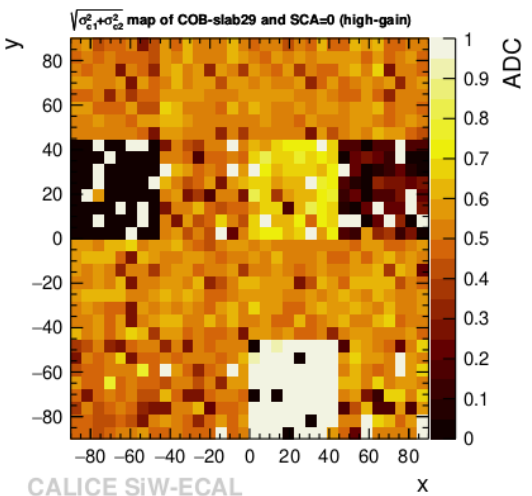




Pedestal and noise, COB -slab29

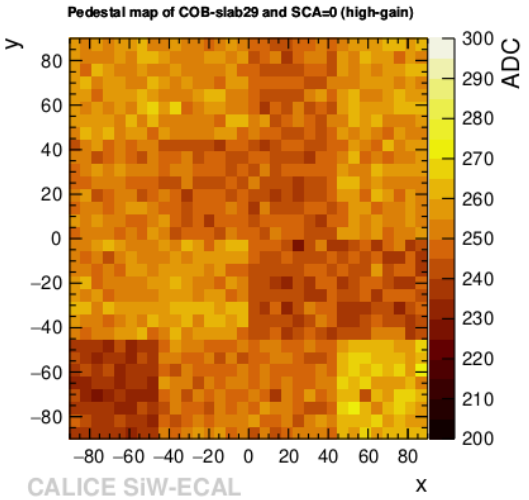


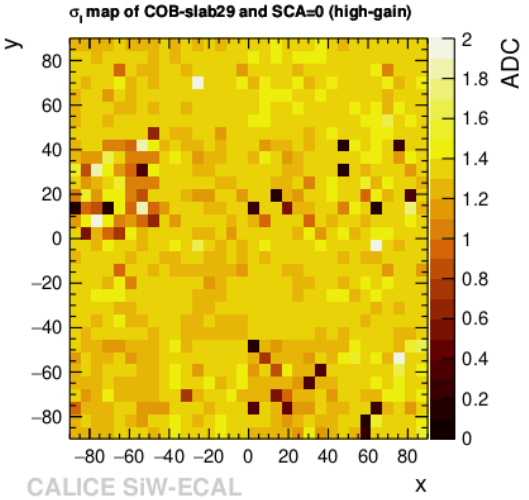


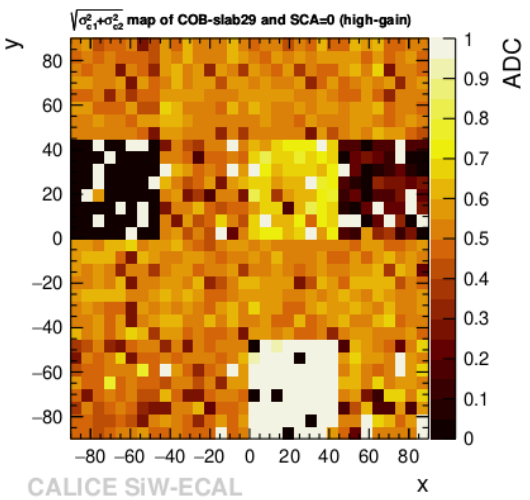


- For the SCA 0, large variations are observed, specially in the ASICs situated in the second and fourth row.
- These rows are in the area of the PCB where most of the routing lines associated to digital signals are located.
  - These variations are associated to large coherent noises that appear at the beginning of the acquisition due to instabilities on the ASIC power supplies.
  - → voltage drops (?) which are translated into pedestal shifts, observed in the data as double pedestal peaks.

Pedestal and noise, COB -slab29







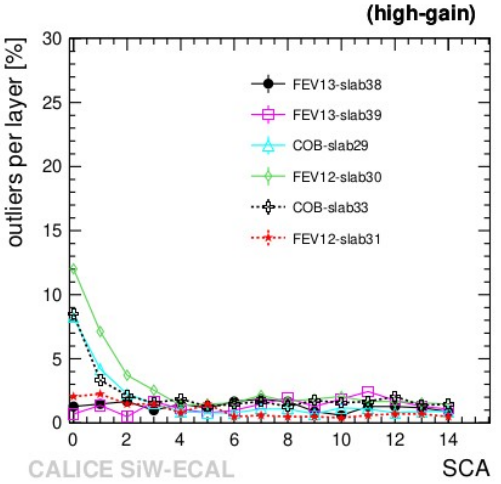
- We define a set of “outliers”
  - Channels that are at more than 3 sigmas of the average noise (incoherent + coherent in quadrature) of the chip
  - Process done iteratively : first we remove the 5sigma outliers for the recalculation of the average

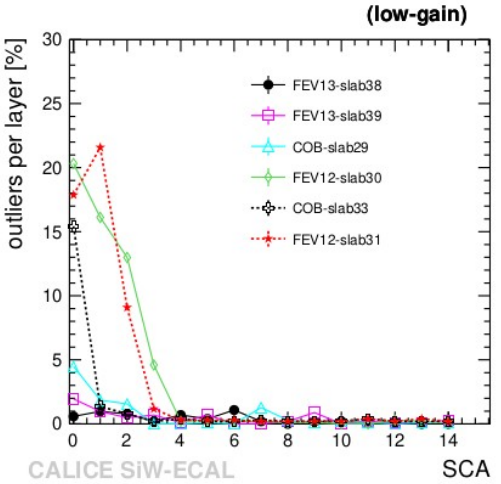
Outliers per PCB

- For the high gain:
  - FEV12 -slab 30 is slightly worst than the COBS
  - COBs are worst than all the others

- For the low gain,
  - FEV 12s seem to behave a bit worst
  - COBs have a very competitive behaviour, wrt the FEV13s
  - 33 is worst than 29 (and has less decoupling capacitances)

- FEV 12 have much less decoupling capacitances than FEV13
  - And COB less than all others





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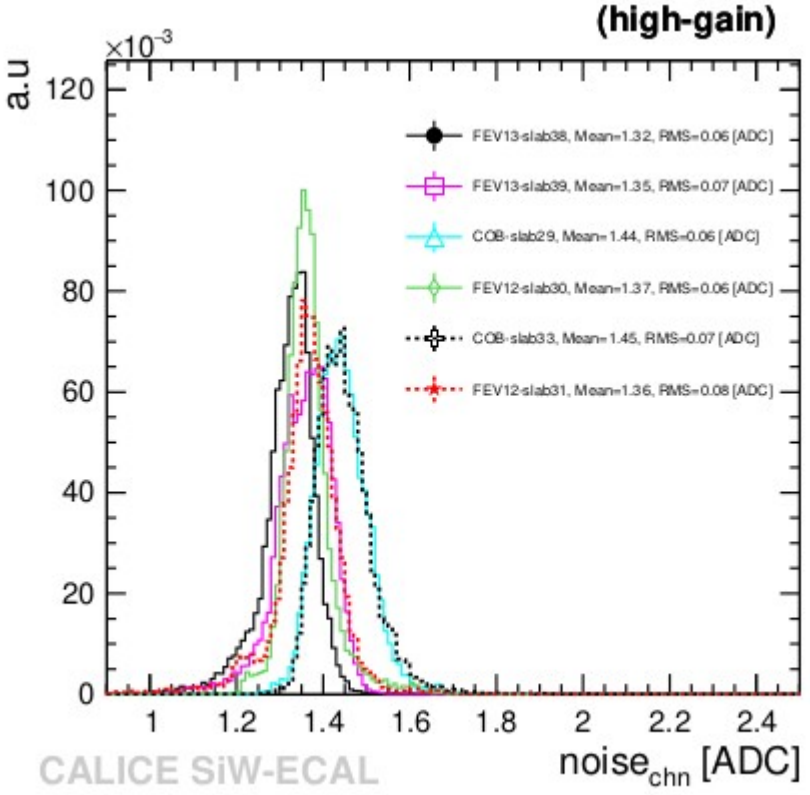
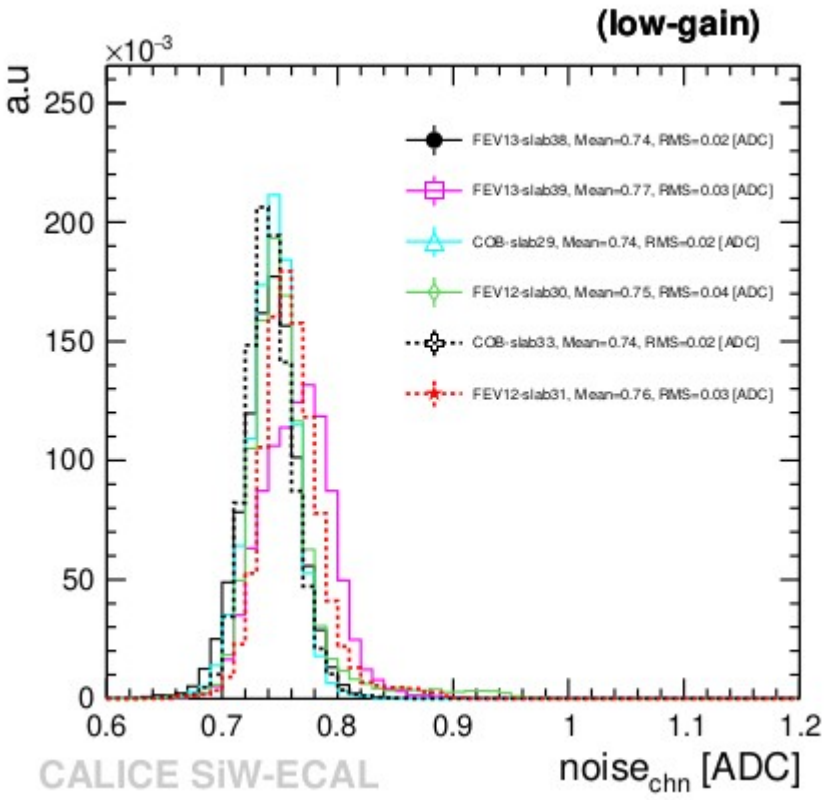
Important remark: before adding the decoupling capacitances to the COBs, making the pedestal studies was simply not possible, at least for the first SCAs

Noise (excluding outliers)





Contribution of the coherent noise

$$R_{C1}(chn) = 1 - \frac{\sqrt{\sigma_I^2(chn) + \sigma_{C2}^2(chn)}}{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn) + \sigma_{C2}^2(chn)}} \quad (2)$$

$$R_{C2}(chn) = 1 - \frac{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn)}}{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn) + \sigma_{C2}^2(chn)}} \quad (3)$$

Contribution of the coherent noise

$$R_{C1}(chn) = 1 - \frac{\sqrt{\sigma_I^2(chn) + \sigma_{C2}^2(chn)}}{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn) + \sigma_{C2}^2(chn)}} \quad (2)$$

$$R_{C2}(chn) = 1 - \frac{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn)}}{\sqrt{\sigma_I^2(chn) + \sigma_{C1}^2(chn) + \sigma_{C2}^2(chn)}} \quad (3)$$

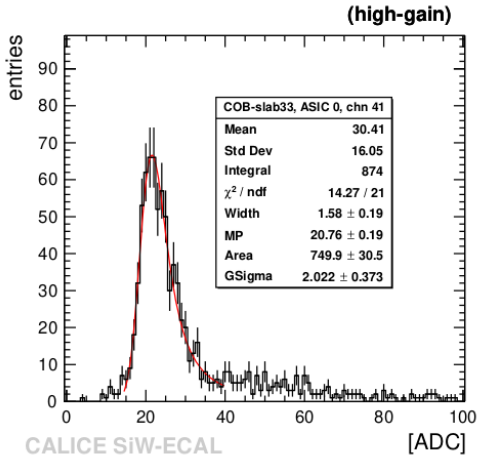
Id	ASU type	$< noise >_{HG}$ [ADC]	$< noise >_{LG}$ [ADC]	$< R_{C1,HG} >$ [%]	$< R_{C2,HG} >$ [%]	$< R_{C1,LG} >$ [%]	$< R_{C2,LG} >$ [%]
slab 38	FEV13	1.32 ± 0.06	0.74 ± 0.02	4 ± 1	2 ± 1	7 ± 1	$\leq 1 \pm 1$
slab 39	FEV13	1.35 ± 0.07	0.77 ± 0.03	5 ± 1	2 ± 1	9 ± 1	$\leq 1 \pm 1$
slab 29	COB	1.44 ± 0.06	0.74 ± 0.02	5 ± 2	2 ± 1	6 ± 1	$\leq 1 \pm 1$
slab 30	FEV12	1.37 ± 0.06	0.75 ± 0.04	5 ± 1	3 ± 1	8 ± 2	$\leq 1 \pm 2$
slab 33	COB	1.45 ± 0.09	0.74 ± 0.02	6 ± 2	2 ± 1	6 ± 1	$\leq 1 \pm 1$
slab 31	FEV12	1.36 ± 0.08	0.76 ± 0.03	5 ± 2	2 ± 1	8 ± 2	$\leq 1 \pm 1$

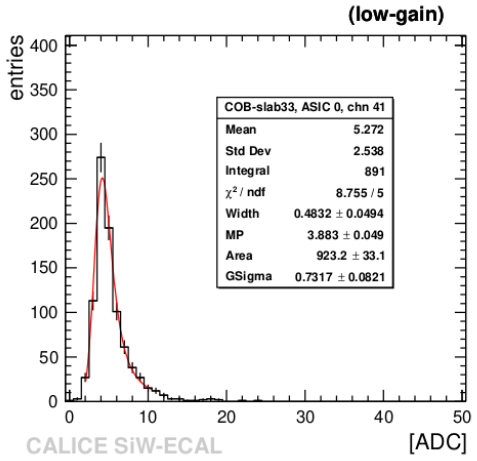
Table 2: Summary of devices under study and their noise parameters. Column by column: ID; ASU type; average measured noise values for the *high-gain* and *low-gain* branches; the relative contribution of the coherent noise sources 1 and 2.

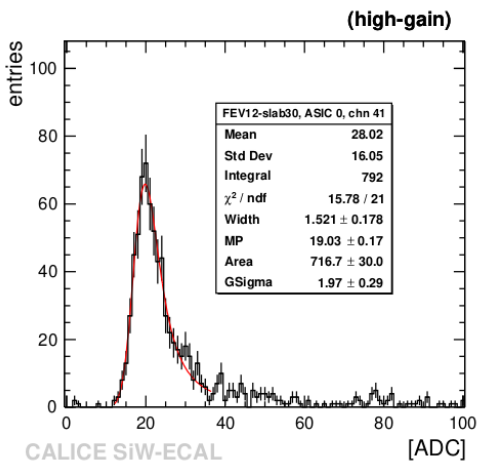
Masked channels

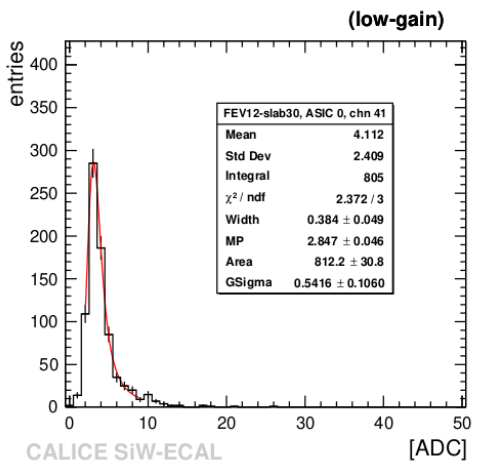
- Iterative process using 0.5 MIP thresholds as goal and requiring the noise not competing with cosmic signals
- FEV12s:
  - 3% of channels always masked (37 + few channels in near the digital line connectors)
  - Less than 1% of random channels
- FEV13s:
  - ~1.5% of channels always masked (37 + few channels in near the digital line connectors)
  - Less than 1% of random channels
- COBs:
  - 6-7% of channels systematically masked (not the 37!, all in the digital-lines rows)
  - Less than 1% of random channels

MIPs









Id	ASU type	$< MIP_{HG} >$ [ADC]	$< MIP_{LG} >$ [ADC]
slab 38	FEV13	16.9 ± 1.3	2.7 ± 0.8
slab 39	FEV13	17.3 ± 1.3	2.8 ± 0.8
slab 29	COB	19.0 ± 1.1	3.2 ± 0.9
slab 30	FEV12	17.9 ± 1.0	2.9 ± 0.9
slab 33	COB	18.9 ± 1.6	3.0 ± 0.9
slab 31	FEV12	18.5 ± 1.1	2.9 ± 0.9

Table 3: Summary of devices under study and their average single cell MIP calibration values.

Summary

- Noise levels of the COB are similar to the other solutions.
  - Amount of decoupling capacitances seems crucial
- The systematically masked channels is larger
  - For all the PCBs, the digital sectors seem critic. More decoupling capacitances are needed.
- A systematic study of noise vs decoupling capacitances would require delicate (possibly destructive) actions...