上海交通大學
SHANGHAI JIAO TONG UNIVERSITY

SJTU

Time-based electronics for T-SDHCAL

Yongqi Tan, Weihao Wu

On behalf of SJTU SDHCAL Group

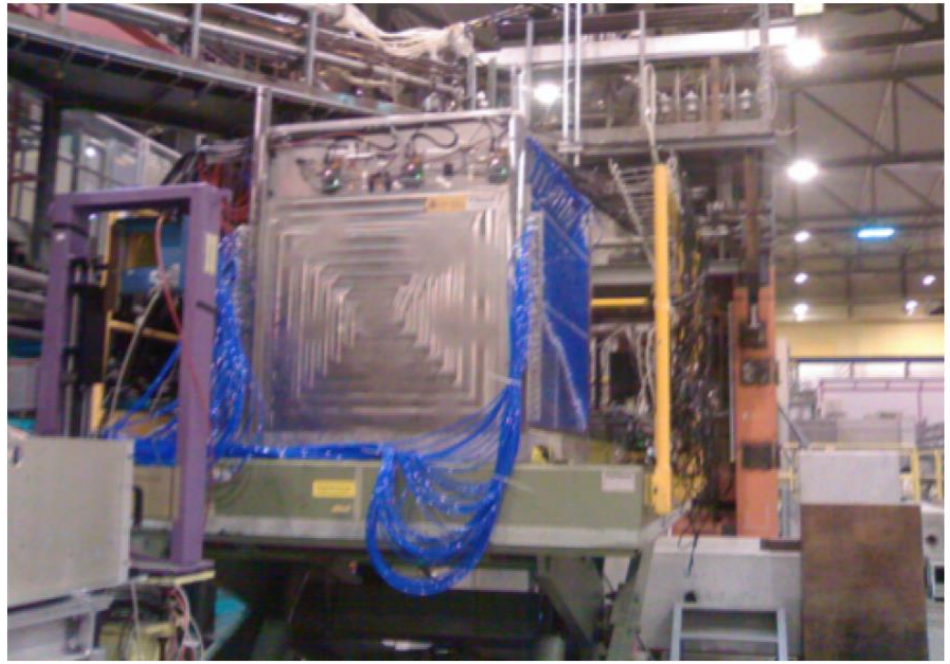
Shanghai Jiao Tong University

30/03/2023

饮 水 思 源 • 爱 国 荣 校

Introduction of timing electronics

- Purpose: Identifying the charged and neutral hadrons
- Method: Adding some MRPC layers in the SDHCAL
- Front-End Electronics for MRPC readout
  - Charge and time measurement
  - **High resolution time measurement**

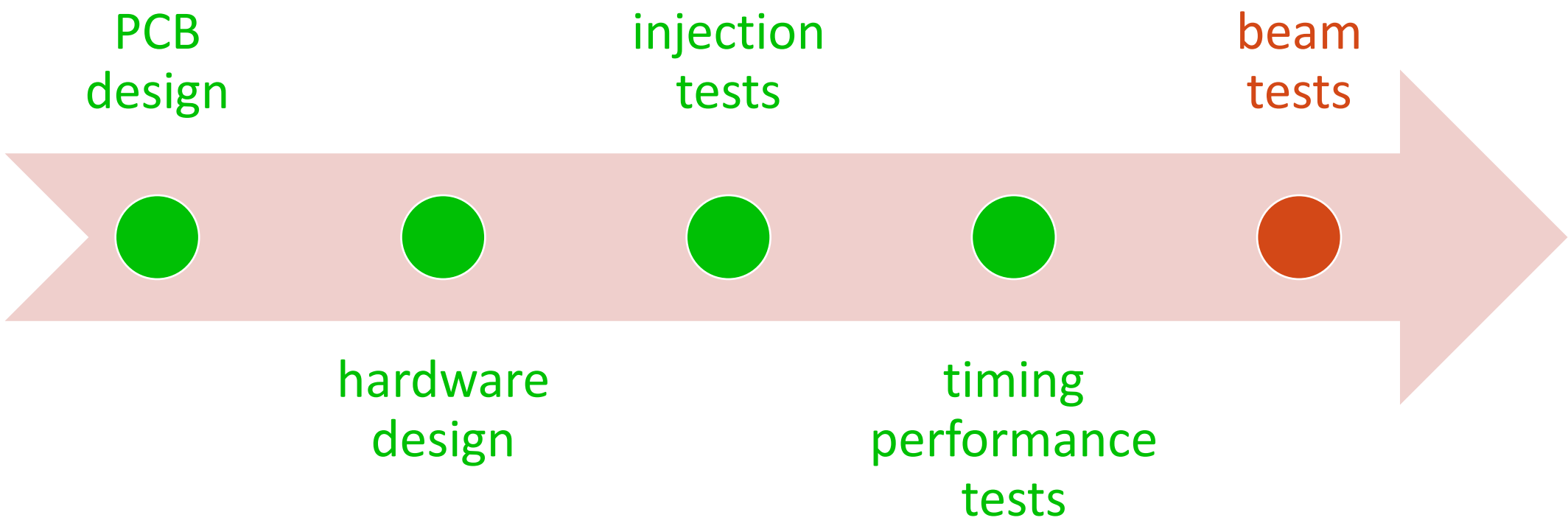


- Road map:
  - Design a FEB prototype with 2 petiroc2B
    - Configure Petiroc2B
    - Accurate time measurement
    - Validation
  - Build larger front-end board module

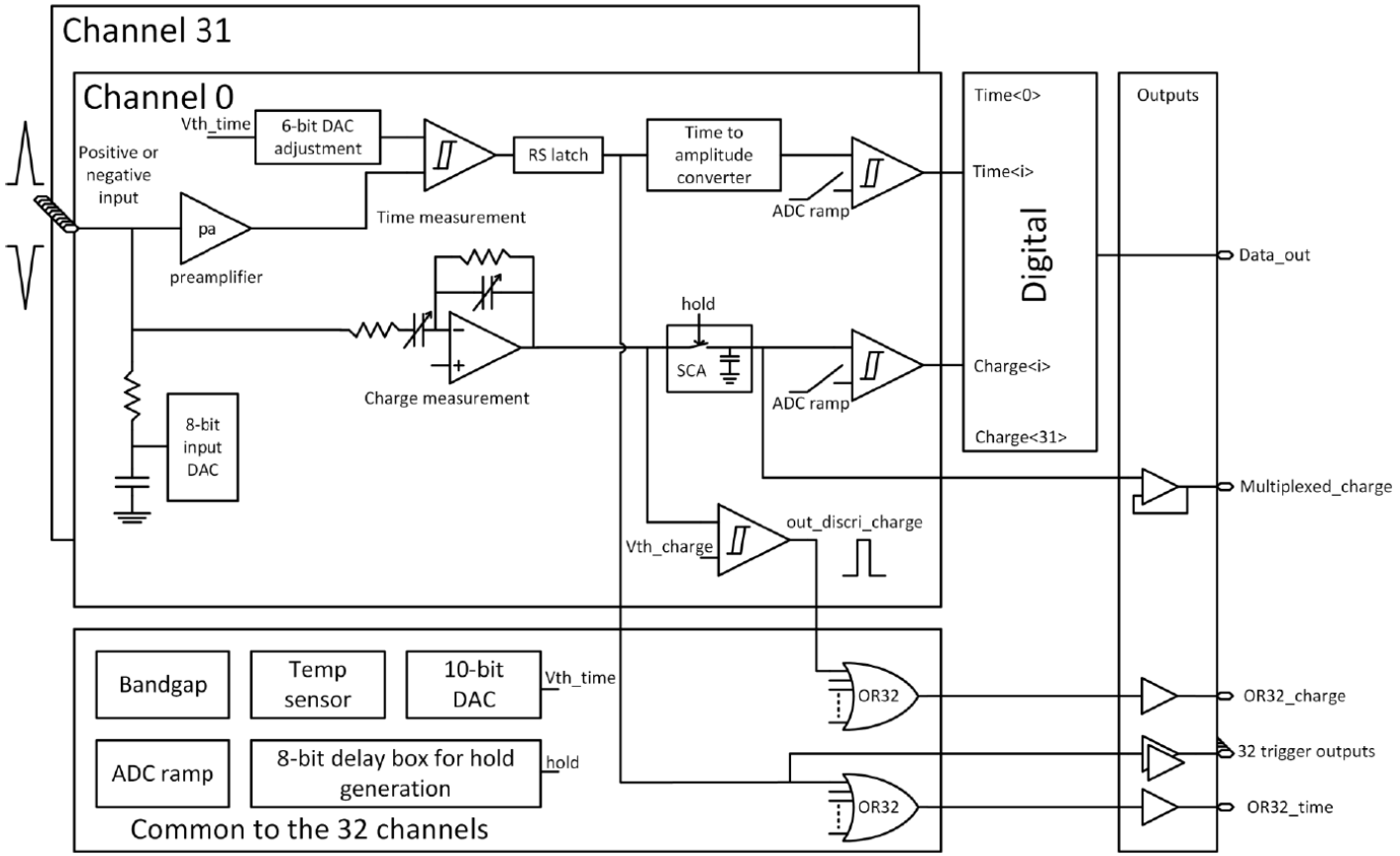
Front-End-Board (FEB) prototype

Timeline of the prototype
Petiroc2B ASIC
Overview
System and setup

Timeline of the prototype



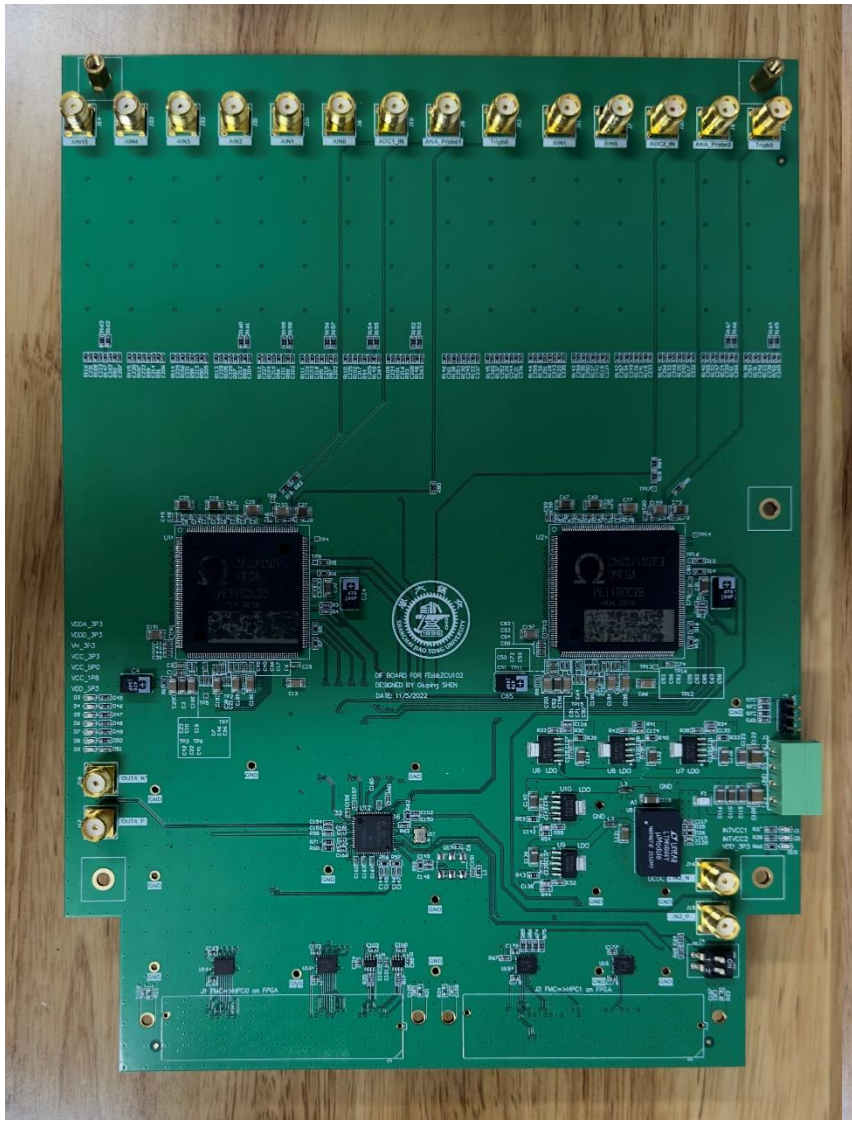
Petiroc2B ASIC

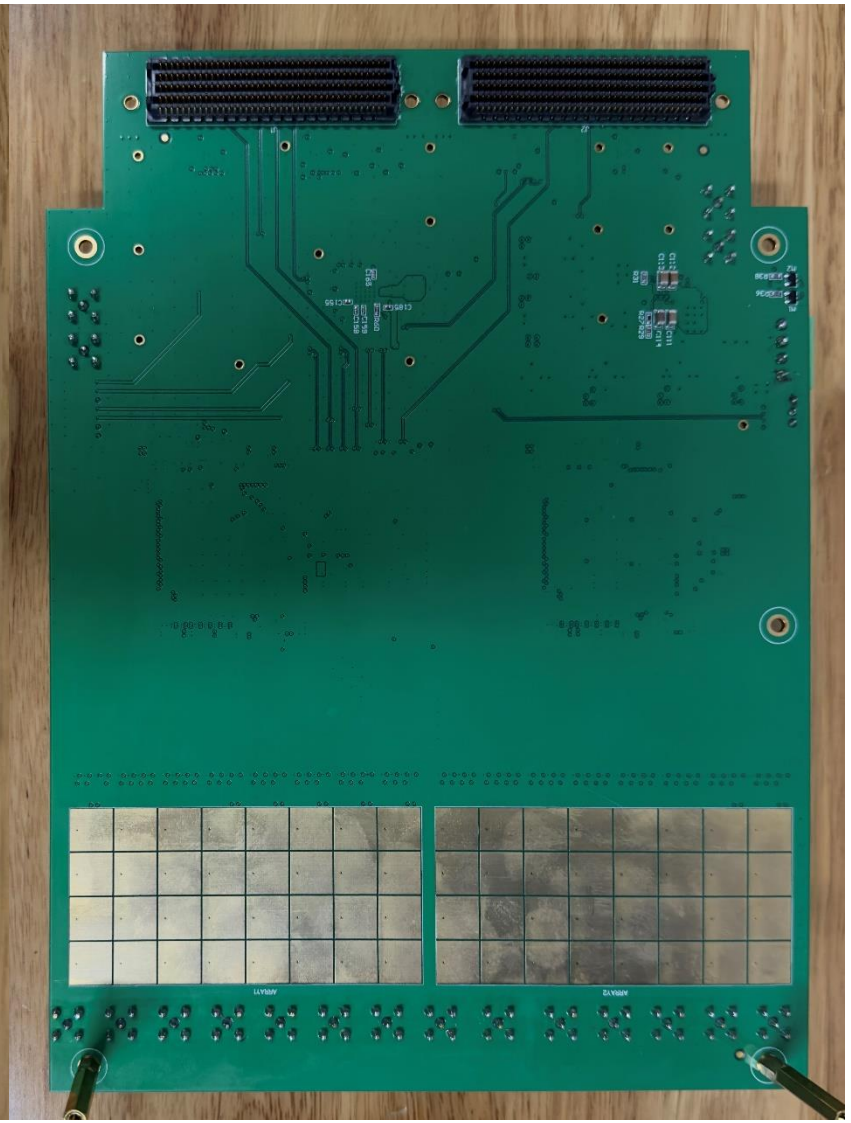


*from Petiroc datasheet v2.5a

- A 32-channel front-end ASIC designed to readout SiPMs (mRPCs as well).
- Combines a very fast and low-jitter trigger with accurate charge and **time** measurements (on-chip TDC).
- timing resolution of on-chip TDC is 37ps.

Overview

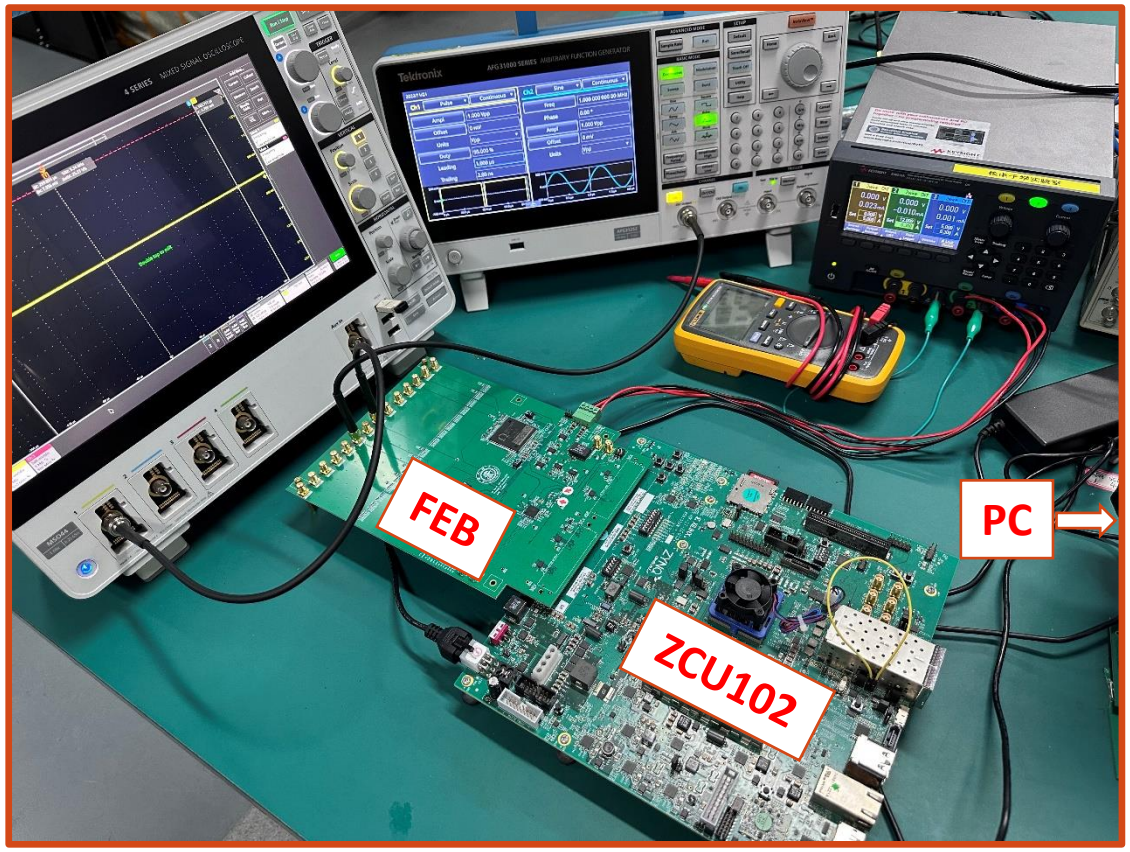


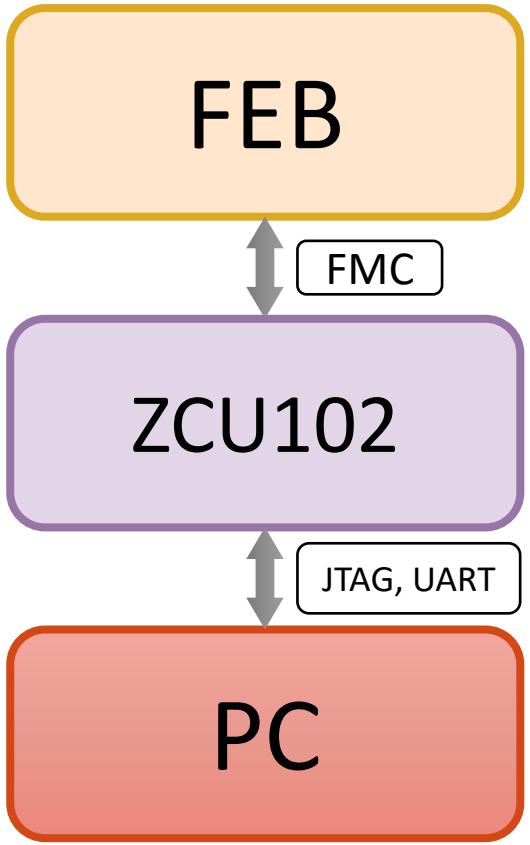


- 2 Petirocs on-board
- 64-channel inputs
- SMAs to inject signals
- 2 FMAs to connect with ZCU102 evaluation board (with ZYNQ-XCZU9EG)
- Power: LTM4644
- Clock: Si5345

✓ Power rail tests have been completed.

System and setup





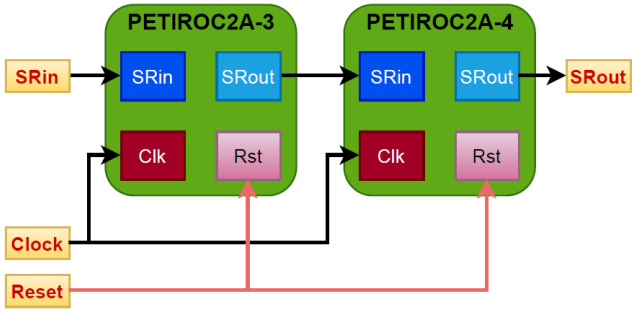
Configurations

Petiroc2B configuration

Validation

configuration of Petiroc2B

- Two chips can be configured through daisy chain.



validation

reference voltages

- After configuration, check all the reference voltages to see if they match the datasheet and Petiroc evaluation boards

threshold tests

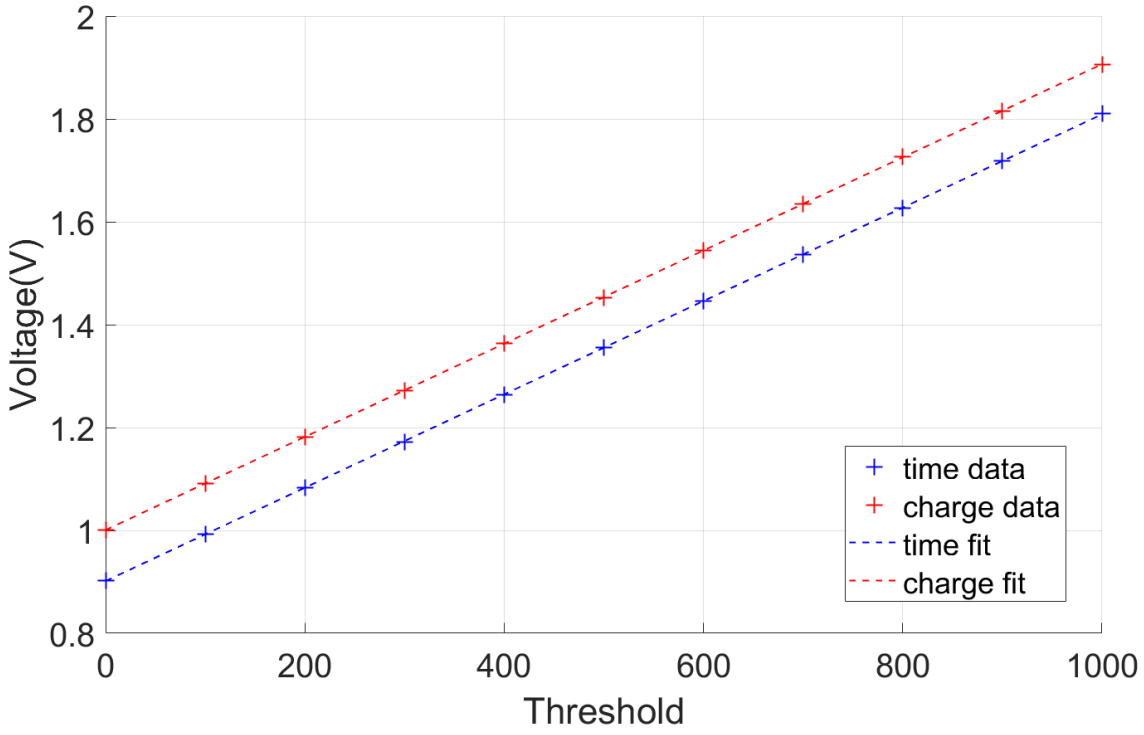
- Set different time and charge thresholds through 10-bit DAC configuration
- Use a voltage meter to measure the analog output of thresholds
- Linear regression and compare with the datasheet

Petiroc2B reference voltage tests

pin #	pin name	test board	FEB	pin #	pin name	test board	FEB	pin #	pin name	test board	FEB
64	vbg	2.521	2.488	73	ib_adc	2.253	2.285	177	ibi_discri_charge	0.789	0.794
49	vref_time	1.684	2.192	74	vcasc1_tdc_pad	1.207	1.2	179	ibo_charge	0.811	0.812
50	vcasc_time	2.225	2.199	75	adc_ramp	1.964	0.966	181	ibi_charge	0.816	0.809
51	vcasc_discri	2.315	2.286	76	vref_adc	0.978	0.964	182	ibo_inpdac	0.8	0.8
52	vslope_tdc	0.345	0.342	78	vslope_adc	0.311	0.307	184	ibm_inpdac	0.53	0.531
54	vth_Time	1.889	1.354	80	ibi_cs_adc	2.486	2.51	186	ibi_inpdac	2.509	2.53
56	vref_inpdac	1.01	0.99	91	ibi_delay	2.355	2.382	189	ibi_tdc	2.358	2.377
58	vref_10bdac	1.442	0.912	93	ibi_rx	2.064	2.063	191	ibo_tdc	0.8	0.804
59	iref_10bdac	2.263	2.231	95	ibo_rx	1.266	1.154	193	ibo_cs_tdc	2.311	2.341
60	vcasc1_tdc	1.215	1.205	96	ibi_tx	0.622	0.622	195	ibm_cs_tdc	2.315	2.338
65	vcasc2_tdc	1.704	1.683	97	vcm_tx	1.185	1.15	197	ibi_cs_tdc	2.478	2.501
67	vcasc_time_pad	2.207	2.185	166	vref_charge	1.018	0.981	200	ib_6bdac	0.587	0.582
69	vth_discri_charge	1.291	1.272	170	ibo_discri_adc	2.245	2.281	204	ibo_discri	1.36	1.343
70	vref_tdc	0.139	0.986	174	ibo_discri_charge	2.255	2.279	206	ibi_discri	0.803	0.805
71	vref_time_pad	1.678	2.192	175	ib_sca	0.863	0.871	207	ibo_time	1.264	1.266
72	vslope_delay	0.249	0.247	176	iref_inpdac	0.389	0.383	208	ibi_time	1.269	1.274

✓ All the reference voltages matched

Petiroc2B threshold tests



Test Results of ours:

$$V_{time} = 0.0009 * threshold + 0.9016$$
$$V_{charge} = 0.0009 * threshold + 1.0008$$

Test Results from datasheet v2.5a:

$$V_{time} = 0.0009 * threshold + 0.8941$$
$$V_{charge} = 0.0009 * threshold + 1.0131$$

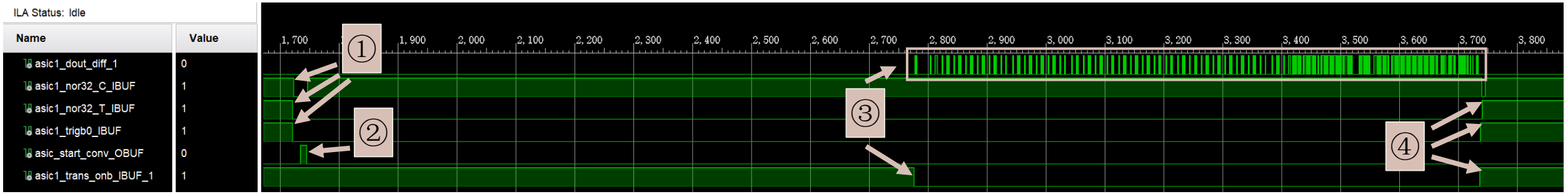
- ✓ The analog output of time and charge thresholds matched input DAC.
- ✓ The configuration of Petiroc2B is valid.

Data readout system

Digital readout timing diagram

Data composition

Digital readout timing diagram



① When the signal is injected, *trigb*, *nor32_T* and *nor32_C* will be triggered (low active).

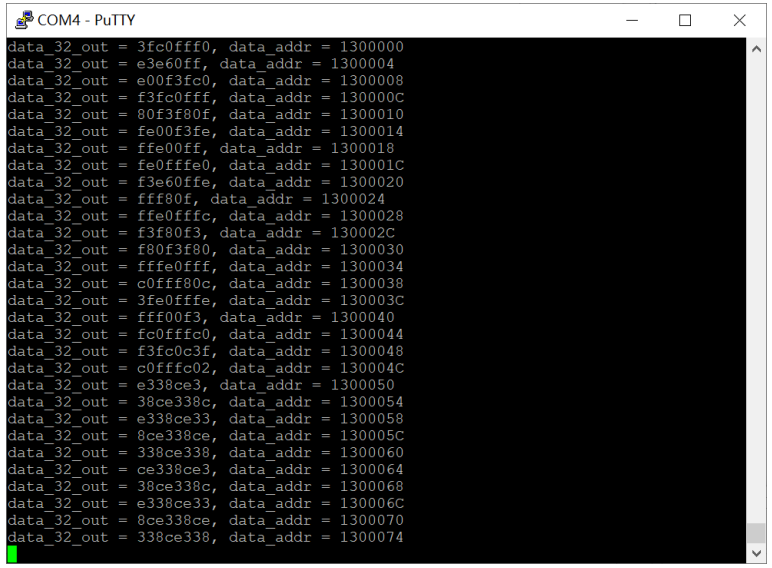
② Pull up *start_conv* signal for at least 100ns (controlled by hardware), to command Petiroc2B to start internal ADC and generate digital data.

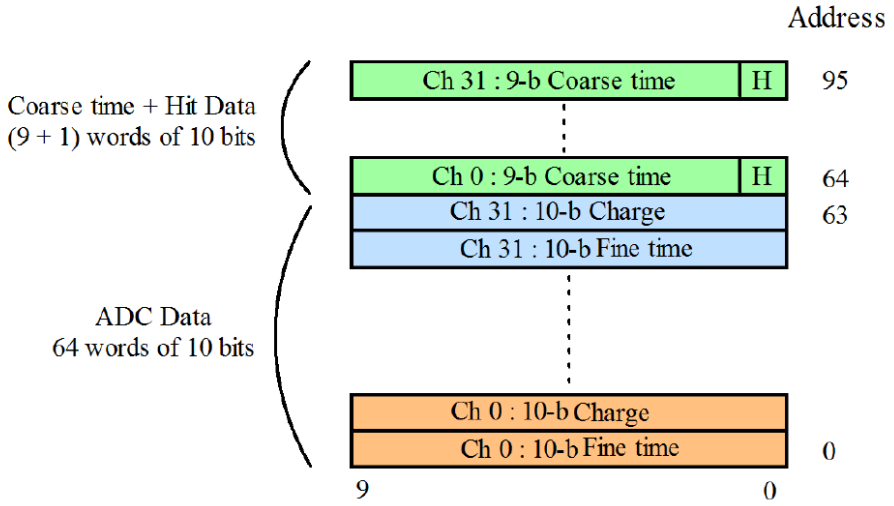
③ Wait till the internal ADC finished converting, *trans_onb* signal will be driven low by Petiroc2B and spontaneously start the data flow (960-bit data stream).

④ After the transfer is finished, all trigger signals will be pulled up by Petiroc2B, and be ready for the next hit.

Data composition

- The data is acquired by UART or JTAG (through ILA)
- 960-bit data is coded in Gray format
- After decoding, we will get 4 data: **coarse_time(9bits)**, **fine_time(10bits)**, charge(10bits) and if_hit(1bit).





*from Petiroc datasheet v2.5a

$$\text{Absolute Timing} = (\text{Coarse time} + 1) \times (\text{ck\_40 period}) - (\text{Fine time})$$

$(25ns)$ $(\times 37ps)$

Injection tests

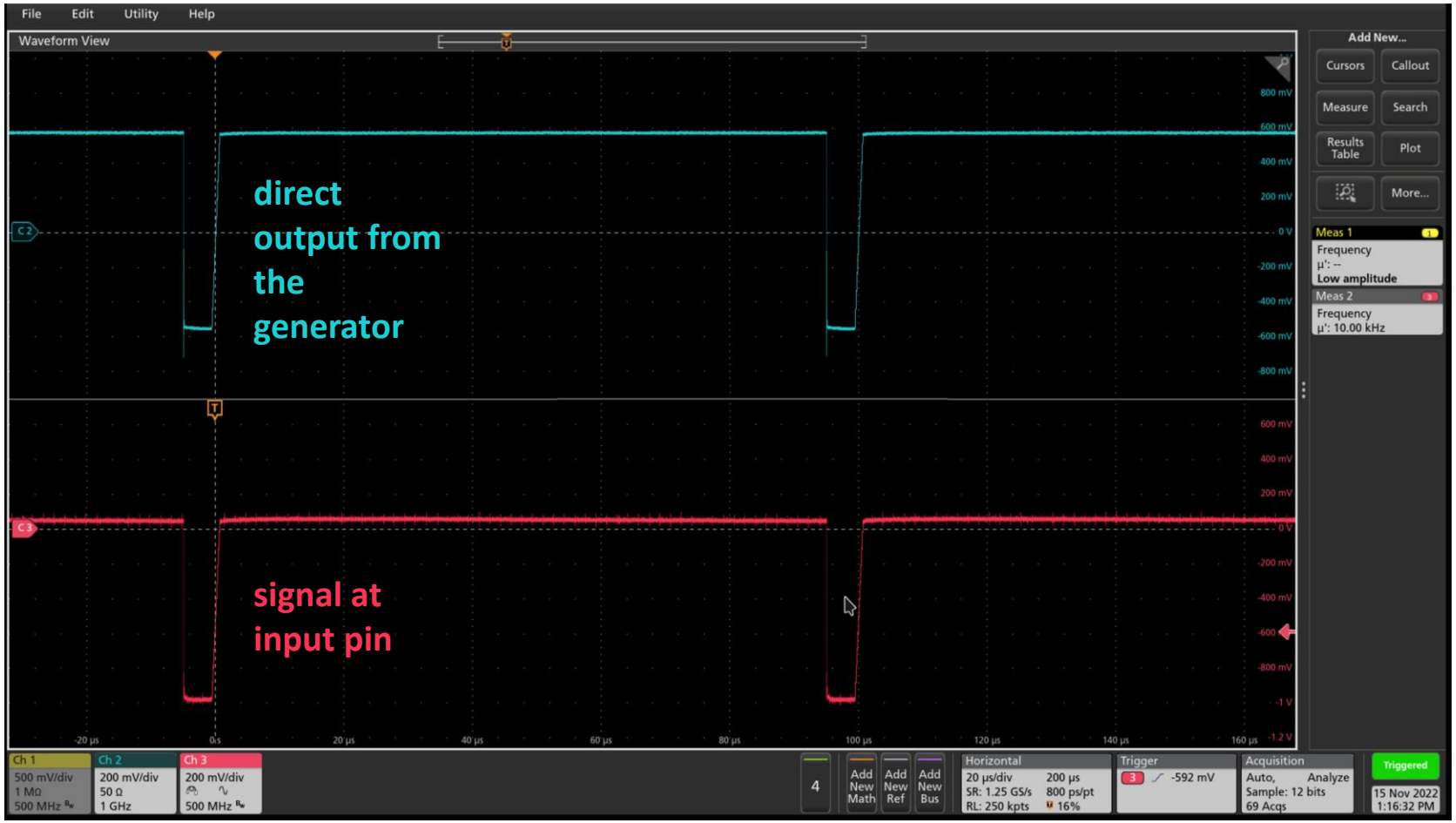
Injected signal profiles

Single injection tests

Timing performance tests

Injected signal profiles

- Negative pulse
- *freq*: 10kHz (period of 100 μs) or 25kHz (period of 40μs)
- 95% duty
- 1Vpp amplitude
- leading of 1us
- trailing of 2ns



Single injection tests

- To test if the new version of FEB has clean signals without crosstalk, we first did some single injection tests:
  1. Inject the signal to one of the 32 channels of one of the Petiroc2B chips.
  2. readout the 960-bit data.
  3. check 'if_hit' data to see if any hits are recorded except for the injected channel.
- All the masks are disabled during the tests.

✓ No crosstalk in the FEB

inject channel

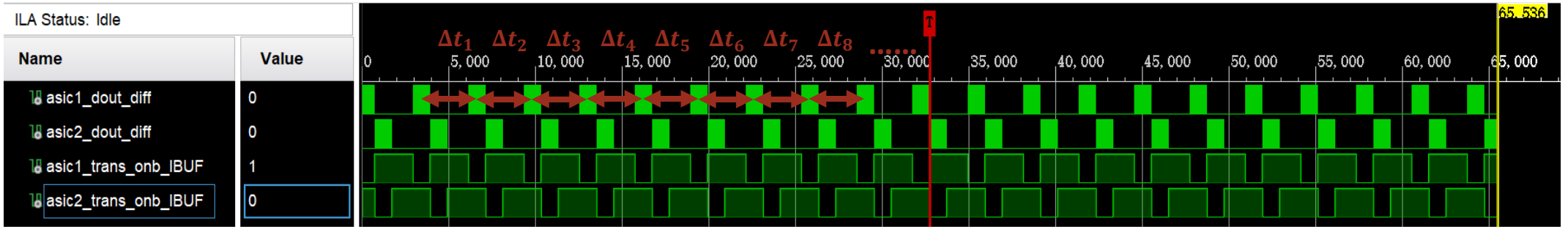
if_hit data

chip1	chn0	chn4	chn8	chn12	chn16	chn29	chip2	chn0	chn4
chn0	1	0	0	0	0	0	chn0	1	0
chn1	0	0	0	0	0	0	chn1	0	0
chn2	0	0	0	0	0	0	chn2	0	0
chn3	0	0	0	0	0	0	chn3	0	0
chn4	0	1	0	0	0	0	chn4	0	1
chn5	0	0	0	0	0	0	chn5	0	0
chn6	0	0	0	0	0	0	chn6	0	0
chn7	0	0	0	0	0	0	chn7	0	0
chn8	0	0	1	0	0	0	chn8	0	0
chn9	0	0	0	0	0	0	chn9	0	0
chn10	0	0	0	0	0	0	chn10	0	0
chn11	0	0	0	0	0	0	chn11	0	0
chn12	0	0	0	1	0	0	chn12	0	0
chn13	0	0	0	0	0	0	chn13	0	0
chn14	0	0	0	0	0	0	chn14	0	0
chn15	0	0	0	0	0	0	chn15	0	0
chn16	0	0	0	0	1	0	chn16	0	0
chn17	0	0	0	0	0	0	chn17	0	0
chn18	0	0	0	0	0	0	chn18	0	0
chn19	0	0	0	0	0	0	chn19	0	0
chn20	0	0	0	0	0	0	chn20	0	0
chn21	0	0	0	0	0	0	chn21	0	0
chn22	0	0	0	0	0	0	chn22	0	0
chn23	0	0	0	0	0	0	chn23	0	0
chn24	0	0	0	0	0	0	chn24	0	0
chn25	0	0	0	0	0	0	chn25	0	0
chn26	0	0	0	0	0	0	chn26	0	0
chn27	0	0	0	0	0	0	chn27	0	0
chn28	0	0	0	0	0	0	chn28	0	0
chn29	0	0	0	0	0	1	chn29	0	0
chn30	0	0	0	0	0	0	chn30	0	0
chn31	0	0	0	0	0	0	chn31	0	0

Timing performance tests

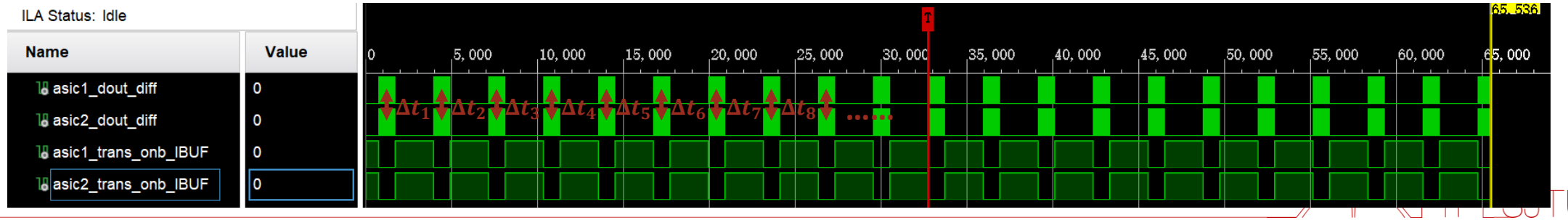
- To test the timing performance, two experiments are implemented:
  - timing tests for single chip, between neighbor hits

    If Petiroc2B is working properly, every two neighbor hits should have the same time gap (when inject signal is uniform). So analyzing the time gaps can get us the timing performance.

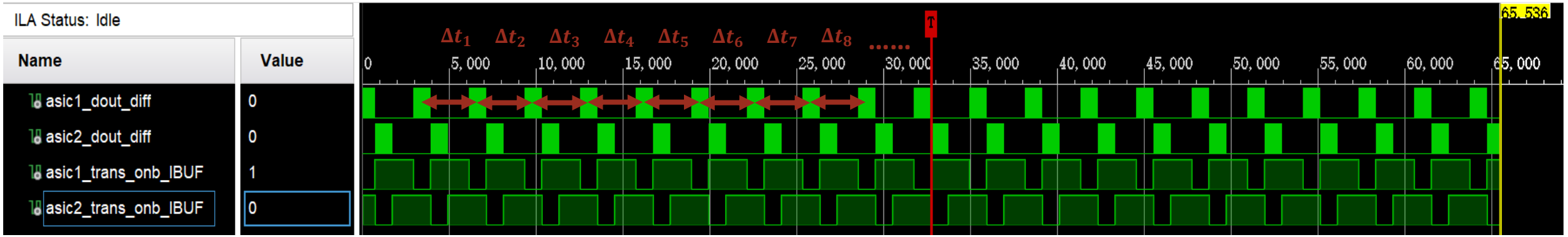


  - timing tests for single hit, between two chips

    Because two chips share one clock source, the phase difference should be fixed, which means that for the same single hit, the time gap between two chips should be fixed.



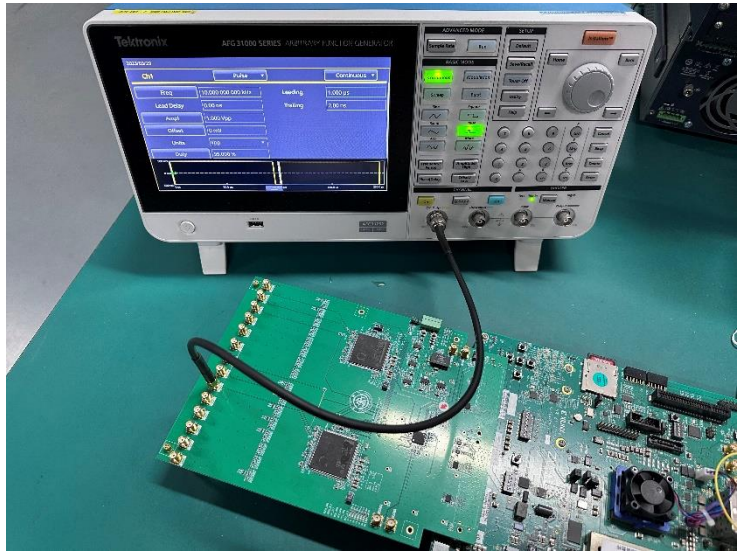
Multiple hits experiments: neighbor hits timing ——process



- Inject signal into one chip.
- Calculate the timing differences (**Δt**) between every two neighbor hits.
- Single variable statistical analysis is done for the calculated **Δt**s.
- If the timing function works well, **Δt** should be fixed for each Petiroc2B chip, and should match the period of the signal.

Check:

- ☐ **Δt** is fixed
- ☐ **Δt** matches the period



Multiple hits experiments: neighbor hits timing ——results

ASIC1	$\overline{\Delta t}(\mu s)$	std$(\Delta t)(ps)$	$f_{sig}(kHz)$	num_of_test
CHN0	**10.3998**	46.4400	10	70 (7*10)
CHN0	**1.5999**	45.3646	25	95 (19*5)
CHN4	**1.5999**	46.5751	25	95 (19*5)
CHN29	**1.5999**	41.4256	25	95 (19*5)
ASIC2	$\overline{\Delta t}(\mu s)$	std$(\Delta t)(ps)$	$f_{sig}(kHz)$	num_of_test
CHN0	**10.3997**	50.7754	10	70 (7*10)
CHN0	**1.5999**	45.4254	25	95 (19*5)
CHN4	**1.5999**	45.6677	25	95 (19*5)

*8 hits recorded in ILA in one experiment, getting 7 Δts. And the experiment is repeated 10 times

- ✓ One bit change of fine time will cause 37ps difference in absolute time.
- ✓ The standard deviation of single chip timing is 32ps $(\overline{std(\Delta t)}/\sqrt{2})$.

- ✓ Δt is fixed. But can it match our signal periods? ($100\mu s$ for $10kHz$ and $40\mu s$ for $25kHz$)

Multiple hits experiments: neighbor hits timing ——analysis

We want to check if the Δt is correct, so certain conversion should be implemented:

- Absolute timing can be calculated from

  Absolute Timing = (Coarse time + 1) x (ck_40 period) – (Fine time)

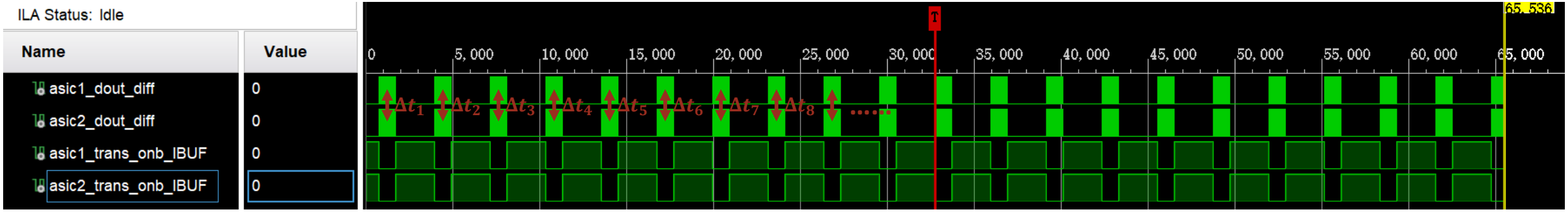
- 9-bit coarse time can count from 0 to 511: $coarse\ time\ (9\ bit) \in [0, 511]$
- so that **(Coarse time + 1) x (ck_40 period)** $\in [1, 512] * \frac{1}{40}\mu s$
- and $\boldsymbol{coarse\ time\ loop\ period} = 512 * \frac{1}{40} = \mathbf{12.8}\mu s$
- for 10kHz signals, $signal\ period = 100\mu s = 7 * \mathbf{12.8} + \mathbf{10.40}\mu s$

  or $100\mu s\ \mathbf{mod}\ 12.8\mu s = \mathbf{10.40}\mu s$
- for 25kHz signals, $signal\ period = 40\mu s = 3 * \mathbf{12.8} + \mathbf{1.60}\mu s$

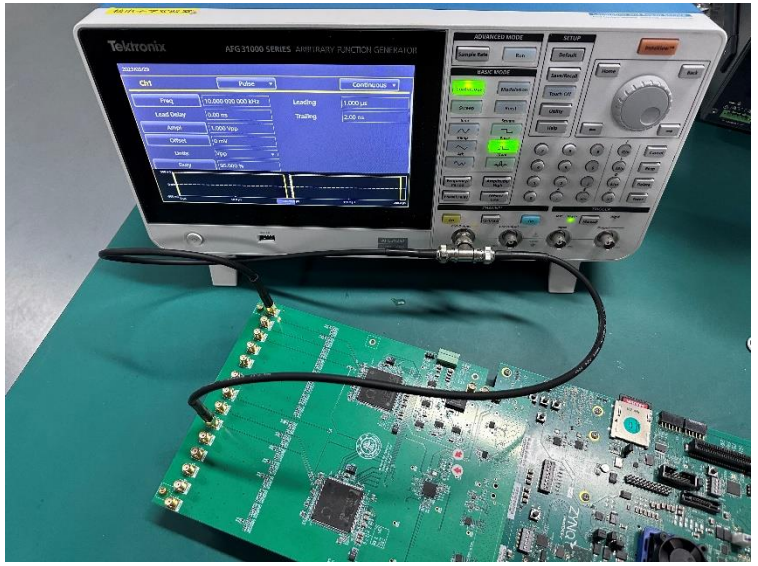
  or $40\mu s\ \mathbf{mod}\ 12.8\mu s = \mathbf{1.60}\mu s$

✓ Δt matches the signal period

Multiple hits experiments: two chips timing ——process



- Inject the same signal into two chips (with a double-pass).
- Calculate the **Δt** between two Petiroc2B chips of each hit.
- Single variable statistical analysis is done for the calculated **Δt**s.
- Because two chips share one clock source, the phase difference should be fixed, which means **Δt** should be fixed.



Multiple hits experiments: two chips timing ——results

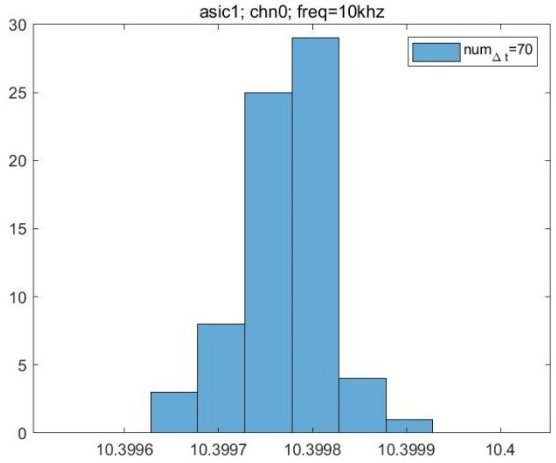
$\overline{\Delta t_{12}}(\mu s)$	$\mathrm{std}(\Delta t_1)(ps)$	$\mathrm{std}(\Delta t_2)(ps)$	$\mathrm{std}(\Delta t_{12})(ps)$	$f_{sig}(kHz)$	num_of_test
5.8000	41.0912	49.5356	73.5276	25	100 (20*5)
5.7999	48.6895	51.9453	78.4336	10	80 (8*10)

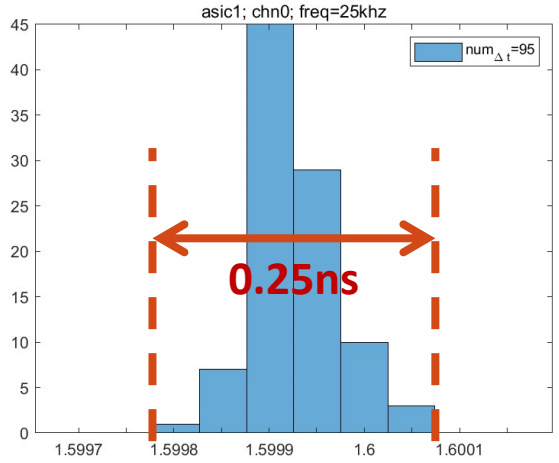
*20 hits recorded in ILA in one experiment, getting 20 Δts. And the experiment is repeated 5 times

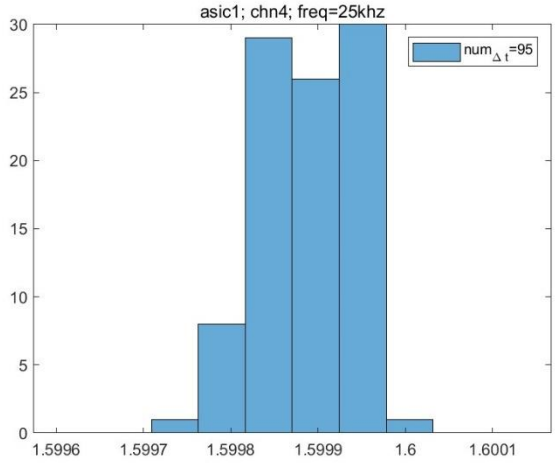
- ✓ $\mathbf{\Delta t_{12}}$ is fixed as expected.
- ✓ $\mathbf{\Delta t_{12}}$ between two chips of one hit is larger than $\mathbf{\Delta t_1}$ or $\mathbf{\Delta t_2}$ between neighbor hits in one chip.
- ✓ The standard deviation of timing between two chips is 54ps ($\overline{std(\Delta t)}/\sqrt{2}$).

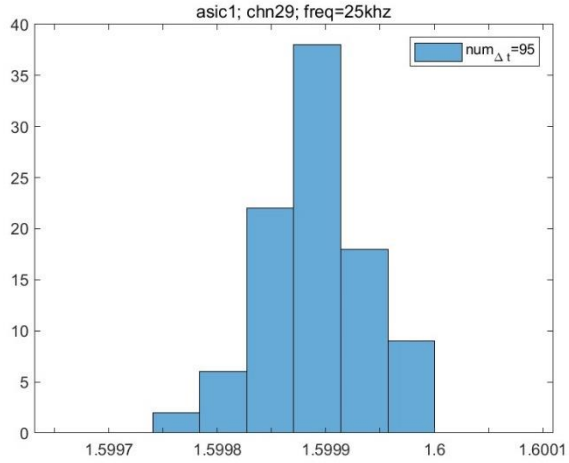
Multiple hits experiments

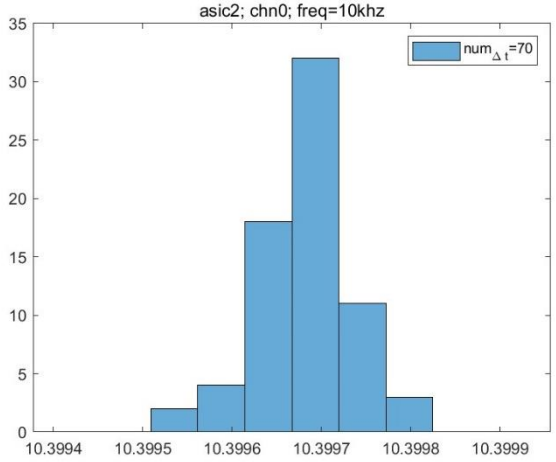
——histogram

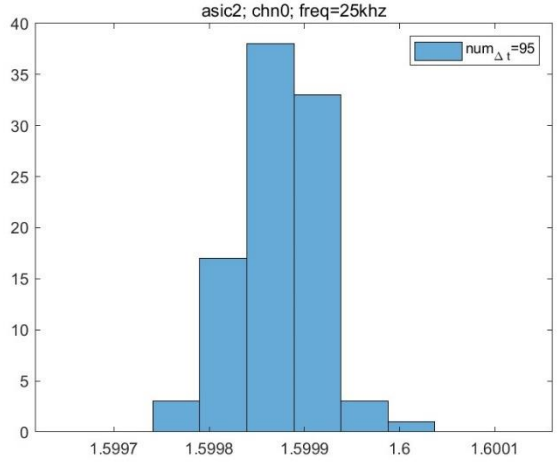


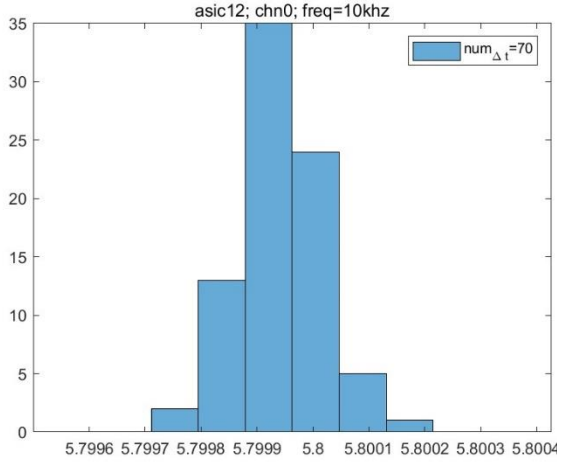


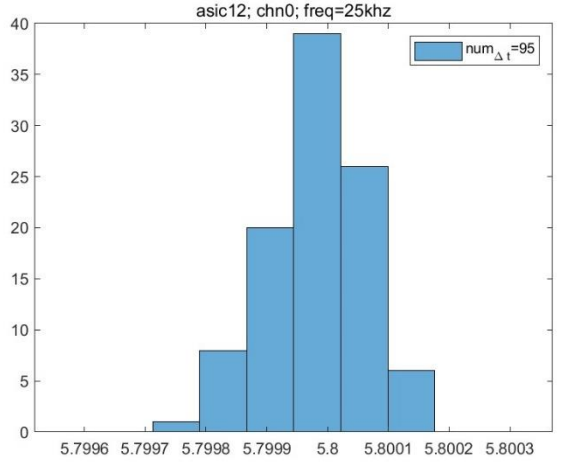












Conclusion

- ✓ FEB is configured correctly
- ✓ No crosstalk in the FEB
- ✓ Timing resolution is $\sim 10^{1} ps$

Next step plans

- Use Ethernet to replace UART protocol to realize high speed data transfer from FEB to PC
- Test the FEB with MRPCs to validate the design (beam tests)
- Build full-sized module

上海交通大學
SHANGHAI JIAO TONG UNIVERSITY

SJTU

Thank you for your attention

Q&A